AML 6213A A/V Processor User's Guide

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Revision History

Revision Number	Revised Date	By	Changes
0.1	2007/05/05	MY	Initial release
0.2	2007/05/14	MY	Updated pin diagram and table

1 Introduction

The AML6213A A/V processor is a complete integrated system targeting the digital picture frame market. The device combines a super fast JPEG/MPEG decoder, all analog LCD drivers/TCON signals, USB and card-reader I/Os and a 32-bit host CPU in a small 144 pins package.

The embedded 32-bits core CPU handles all system related application software. It executes AVOS, the base operating system for AML6213A. All applications and drivers run on top of AVOS. Drivers including USB drivers, card-reader hardware driver, and video and other hardware related programming interfaces are provided by AVOS. Applications include graphical user interfaces and file system sub-system are also included. Developers can add additional applications to customize for each platform.

The core CPU interfaces to the video and audio processing hardware. It performs advanced digital audio decoding. It provides support for all existing audio formats and it also has enough flexibility to accommodate new audio standards. Popular audio formats like MPEG Layer I/II/III, LPCM, MP3, WMA, AAC and WAV can be supported.

MPEG1/2/4 and JPEG/M-JPEG streams are processed by dedicated video/picture decoding hardware and the flexible Video AMRISC™ engine. The hardware and microcode combination is capable of decoding home video from digital cameras, and JPEG pictures with no limits in picture resolution. Once decoded, the output pictures are passed to a sophisticated video sub-system that performs video/image analysis, enhancement and scaling functions. Contrast enhancement, hue adjustment, video scaling, video interpolation, and zoom are also supported. The high-resolution scalar supports both up-scaling and down-scaling of images and video. The scalar can also mix in multiple graphics and OSD layers for the final display. The integrated video encoder supports all analog LCD panel resolutions thru the on-chip triple panel DACs. In addition, a programmable analog LCD TCON is included for the AML6213A to interface to analog LCD panels directly.

The AML6213A also integrated a USB 2.0 High Speed OTG controller/PHY and card-reader controller. The card-reader controller can support SD/SDHC, MS/MS-Pro/MS-Duo/MS-Pro Duo, MMC, xD and CF cards. FAT and FAT32 file systems are supported. The USB controller can be connected to USB hard disk, FLASH drive, digital cameras and MP3 players. The AVOS drivers and applications for AML6213A firmware includes the basic USB device driver, USB protocol stacks to support bulk and INTR transfer, Hub, Mass-Storage (MS) class and Picture Transfer Protocol (PTP). The AVOS USB firmware also supports multiple file systems and includes flexible file transfer functions between USB devices.

AML6213A A/V processor has a set of very flexible clocking circuits that implement the adaptive AMPOWER-II power reduction algorithms. The chip works in conjunction with the AVOS software to reduce total power consumption based on processing load, type of media streams being processed and the output requirements. With AMPOWER-II, the system can reduce power consumption for portable applications and helps consumer electronics to achieve the Energy Star rating. In addition, AMPOWER-II also provides higher performance within smaller, thermally constrained environments.

2 Features

The AML6213A chip is very flexible and most of the capabilities are under firmware control. The following list of features may or may not be included in the firmware library or binary, depending on the actual application and platform.

- **High Integration**
  - Embedded 32-bits core RISC processor for system control
  - Complete JPEG/MPEG decoding logic and video scaling logic
  - Complete audio decoding and stereo audio DACs
  - Integrated analog LCD panel DAC and TCON
  - Integrated USB 2.0 High Speed OTG port
  - Integrated card reader controllers
  - Integrated NAND FLASH controller

- **JPEG/M-JPEG Decoding**
  - Super fast hardware decoding of JPEG picture
  - Unlimited pixel resolution (currently test with 16M pixel pictures)
  - Supports scaling (zoom in or out), rotation and transition effects
  - Automatic image analysis and enhancement
  - M-JPEG engine supports up to full frame rate (30 fps) VGA quality movies

- **MPEG 1/2 Decoding**
  - MPEG video engine controlled by a dedicated Video AMRISC™ processor
  - MPEG-2 ML/MP conforming to ISO-13818
  - MPEG-1 ML/MP conforming to ISO-11172
  - Sub-picture and highlight decoding and display
  - Advanced error detection, concealment, and recovery scheme
  - *.mpg, *.mpeg, *.dat, and *.avi file formats can be handled by AVOS and CPU subsystems

- **MPEG 4 Decoding**
  - MPEG-4 ASP and XVID compliant
  - Multiple language and multiple formats DivX sub-title support
  - *.avi and *.mov file formats can be handled by AVOS and CPU subsystems

- **Other Images/Pictures Decoding**
  - Decodes BMP, PNG, GIF, TIFF and other popular picture formats
  - Supports zoom in and out, rotation and transition effects

- **Special Trick Modes:**
  - Pause
  - Reverse playback
  - Multiple steps fast forward/backward

- **Video Processing**
  - Variable steps video zooming (up to 8x)
  - On-Screen-Display (OSD) capable of supporting 4/16/256 colors or True-Color
  - OSD alpha-blending over video display

- **TV Encoder / TCON**
  - Triple panel DAC designed especially for analog LCD panels
  - Programmable tint, brightness and other TV enhancements
  - Integrated programmable timing controller (TCON) for analog LCD panels

- **Graphics**

- Graphics can be scaled independently of the video output
- Unified MPEG video and graphics memory architecture for maximum flexibility and system cost savings

➢ **Audio Decoding**
- Full MPEG audio layers I, II and III
- Capable of decoding popular audio formats including: MP3, WMA and WAV

➢ **Audio Post Processing and Output**
- Integrated a 2-channel audio DACs
- Muting, volume control, etc.

➢ **USB Interface**
- Integrated OTG 2.0 High Speed controller and PHY
- Backward compatible with USB 1.1 devices
- USB OTG port can be configured as USB device, host or OTG port
- DMA support for data movement for BULK, INTR and ISO transfer
- USB device driver, native USB protocol stack supported in AVOS firmware
- Integrated support for Mass-storage class (MS-Class) and Picture Transfer Protocol (PTP)
- USB Hub support
- Video, audio and image decoding from USB attached MS-Class or PTP devices
- Connecting to PCs or Apple computers as USB MS-Class devices

➢ **Card Reader Interfaces and Controllers**
- Support MS, SD/SDHC, MMC, xD and CF memory card formats
- Supports reading and play back of audio and picture multimedia files
- AVOS software supports all file operations via file system on each memory card

➢ **Core CPU Sub-system**
- 32-bit core CPU dedicated for user applications
- Embedded debug interface using ICE/JTAG
- Shared MPEG SDRAM as run time data storage for minimal system cost
- Integrated interrupt controller
- Integrated general purpose timers and counters
- Integrated general purpose DMA controllers
- Supports up to 8M bytes of 8-bit FLASH chip
- Supports single SDRAM interface (m1_*). The SDRAM interface can support 8M or 16M bytes of SDRAM.

➢ **System, Peripherals and Misc. Interfaces**
- One 27 MHz crystal oscillator for A/V system
- AMPOWER-II power reduction algorithm for portable devices
- Numerous programmable GPIO pins for system control and interrupts
- Integrated i2c master controllers, remote control input circuitry, quad PWM output pins
- 1.2 volt and 3.3 volt power supplies
- 3.3 volt I/O support
- 144 pins PQFP RoHS package

3 External Interfaces

3.1 Global Configurations

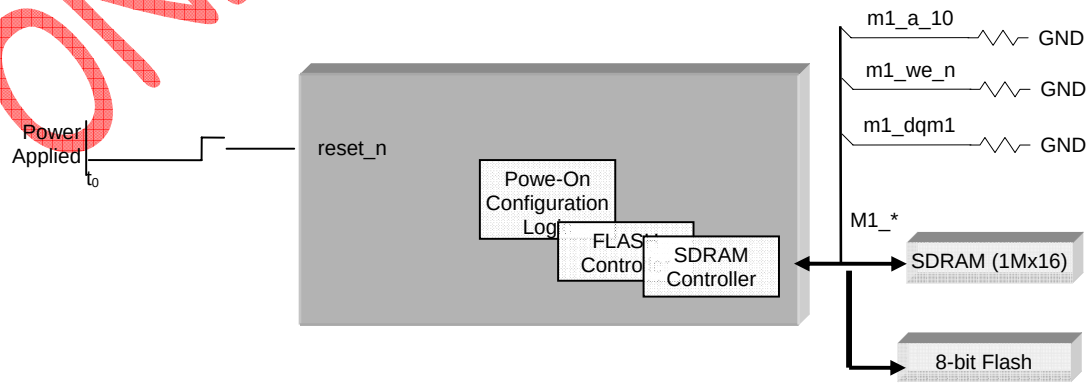
3.1.1 Powe-On Configuration

The chip has a common active-low reset signal called *reset_n*. This signal puts the entire chip into a known state by resetting internal registers and state-machines to their default states. Typically this signal is held low for at least 100 msec after the power and crystal clock is stabilized. The reset process also plays a role in configuring certain functions within the chip. Using the state of the configuration pins and the rising edge of the *reset_n* signal, the user can dictate the configuration of the JTAG pins and the boot device. The configuration pins should be pulled up or down using 10K resistors to either 3.3v or ground.

PIN	Function
m1_a_10	This pin controls the **JTAG** configuration after RESET: ➢ Tie to 3.3v with 10k resistor for JTAG debugging ➢ Tie to ground with a 10k resistor to use the JTAG pins as GPIO
m1_we_n	This pin controls the **Boot Option** after RESET: ➢ Tie to 3.3v with 10k resistor if the boot device is NAND FLASH ➢ Tie to ground with a 10k resistor if the boot device is NOR FLASH
m1_dqm1	This pin controls the **FLASH Data Wide** after RESET: ➢ Tie to 3.3v with 10k resistor for 16-bit FLASH device ➢ Tie to ground with a 10k resistor for 8-bit FLASH device
m1_cas_n	This pin controls the **NAND Page Size** after RESET (only for NAND flash): ➢ Tie to 3.3v with 10k resistor for 512 bytes page size ➢ Tie to ground with a 10k resistor for 2048 bytes page size
m1_ras_n	This pin controls the **NAND Flash Size** after RESET. The pin controls the number of ALE pulses that are issued to set the ROW address. ➢ Tie to 3.3v with 10k resistor for large size NAND flash device that needs 3 ALE pulses ➢ Tie to ground with a 10k resistor for small size NAND device that needs 2 ALE pulses

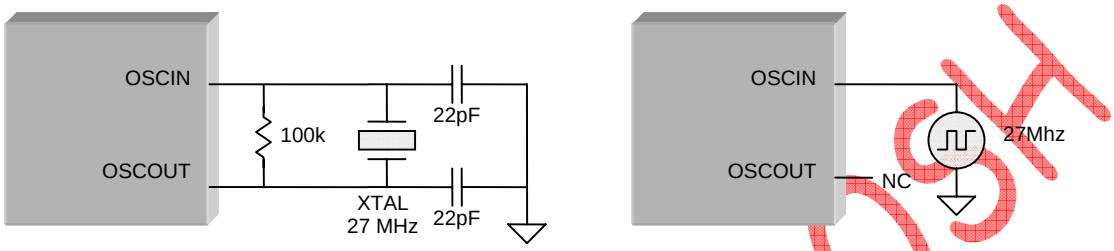
Example:

The following example illustrates a start-up configuration for a single 2M Bytes SDRAM and 8-bit FLASH memory during a production environment (i.e. no JTAG debugging). M1_a_10 is tied to GND to disable JTAG debugging; m1_we_n is tied to GND to boot from NOR FLASH; and m1_dqm1 is tied to GND for 8-bits NOR FLASH device.



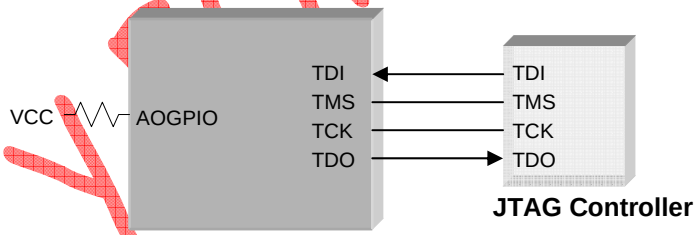
3.1.2 Clocks

The AML6213A has multiple internal clock domains, but all the internal clock domains are derived from a single external reference: *OSC*. As illustrated below, the crystal/oscillator pin pairs (OSCIN/OSCOUT) can be connected to a crystal or driven from an external oscillator. In the typical A/V application, a 27 MHz crystal is connected to the *OSC* pins. The following diagram depicts a typical crystal circuit; the actual values of the components depend on the type of crystal used in the application.



3.1.3 JTAG for Software Development

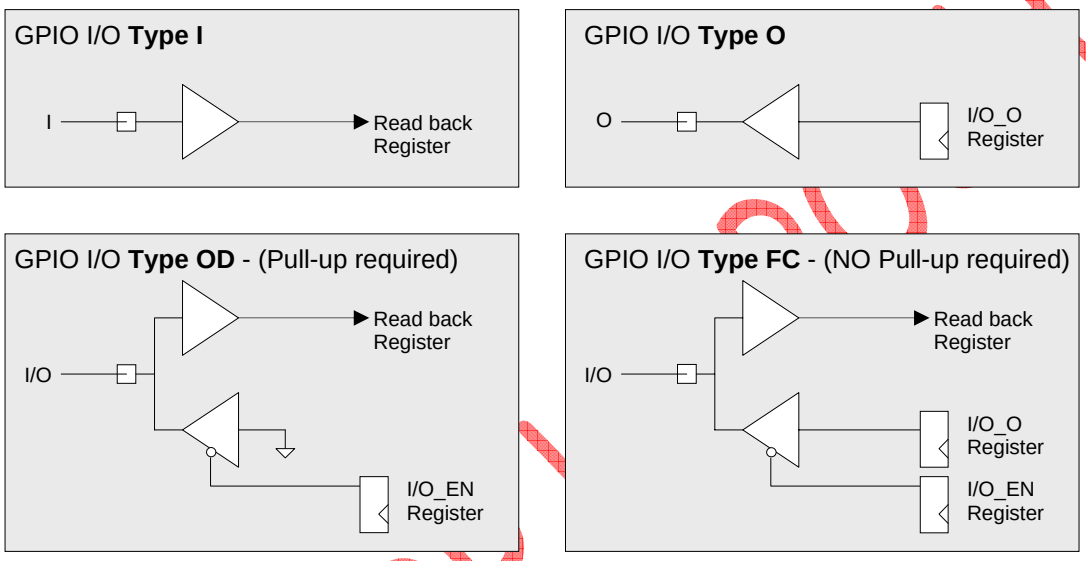
The embedded core processor can be controlled through its JTAG port using the embedded ICE interface. The embedded ICE interface allows the developer to download code/data to the SDRAM memory, probe registers on the AML6213A chip, execute and debug the RISC code using a user friendly development environment. The JTAG interface is enabled by tying m1_a_10 high high as illustrated below.



3.1.4 GPIOs

Configurable hardware controllers (e.g. i2c, card-reader, etc.) and DMAs are integrated into the AML6213A device to speed up the common operations and relieve the core RISC for user-level applications. Since hardware controllers and state-machines cannot cover all possible external devices or system-level signals, numerous general-purpose I/O pins are available on the chip for purpose like Portable Media Player keypads. Each GPIO pin can be independently configured to be an input or an output. As indicated in the diagram, there are various I/O types.

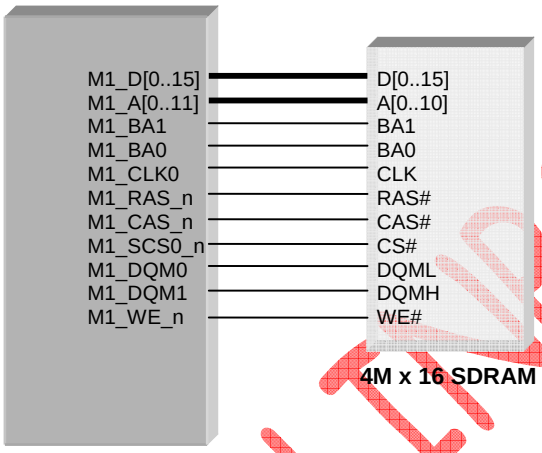
GPIO PAD TYPES



3.2 Memory Interfaces

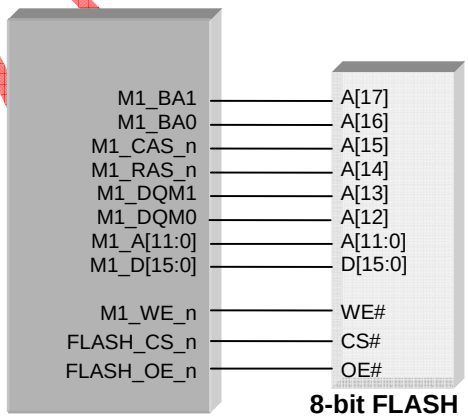
3.2.1 SDRAM Interfaces

The AML6213A device uses external SDRAM for data storage and code execution. The SDRAM1 interface is labeled as *m1_** interface. The SDRAM interface can access up to 16M bytes of memory. Depending on the application, 166MHz 4Mx16 or 8Mx16 SDRAM chips can be used. The following example depicts a system with 8M bytes of SDRAM on m1_* interface.



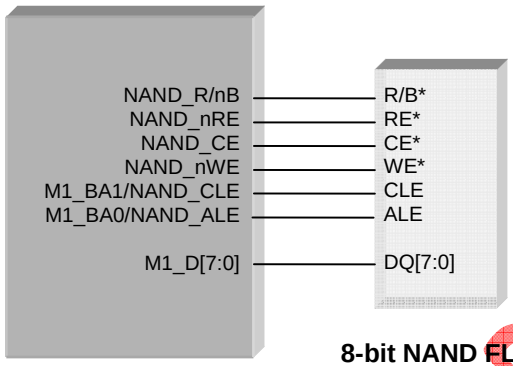
3.2.2 FLASH Interface

The FLASH interface can accommodate an 8-bits FLASH device. Due to the limited number of I/O pins, the FLASH interface is shared with the SDRAM (m1_*) interface. Up to 8M bytes of FLASH is accessible with the 8-bits wide FLASH interface design. The FLASH should be connected as indicated in the following diagram:



3.2.3 NAND FLASH Interface

The NAND FLASH interface can accommodate an 8-bits or 16-bits NAND FLASH device. Due to the limited number of I/O pins, the FLASH interface is shared with the SDRAM (m1_*) interface. NAND FLASH has a very large capacity that ranges from 32MB to more than 1GB. The NAND FLASH should be connected as indicated in the following diagram:

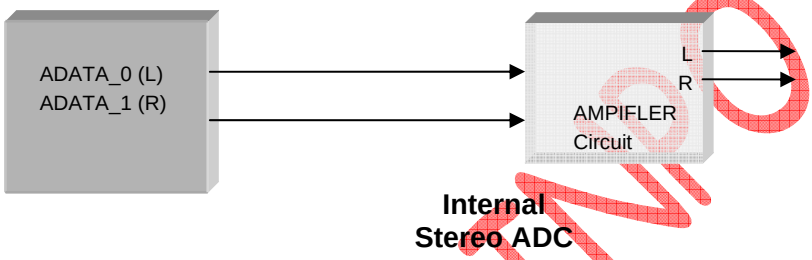


8-bit NAND FLASH

3.3 Audio Interfaces

A pair of audio DACs is provided in the AML6213A device. The audio DACs are designed for connecting to small speaker inside the photo frame or ear buds for external listening. A simple external amplifier is needed. Please see the following sample circuit diagram.

Internally, the delta-sigma algorithm is used to improve the performance and ensure high SNR output. The implementation includes a multi-tap interpolation filter which increases the sample rate of the audio channels to the modulator rate. Then the audio stream is passed through a sigma-delta modulator that generates the serial PWM data stream. An internal analog filter is then used for out-of-band noise filtering and analog signal reconstruction. External amplifier is needed to provide the necessary current to drive the speakers or head phones.



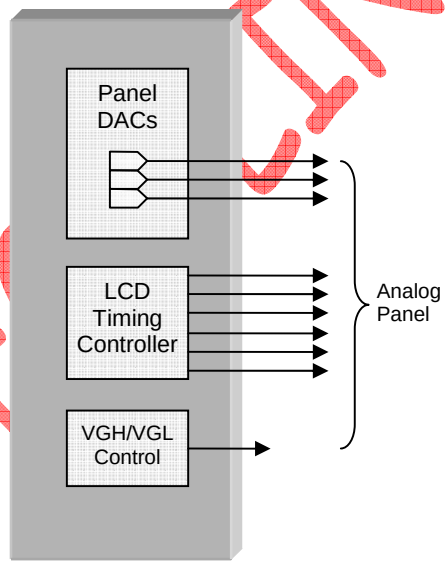
3.4 Video Output Interfaces

3.4.1 Analog Video Output

The AML6213A integrated internal LCD video scalar and encoder and high resolution triple panel DACs (PDAC) for direct connection to analog LCD panels. The LCD scale and encoder convert the video images to the LCD resolution and prepare the image to be displayed on the LCD panel. The Panel DACs are internally calibrated by the firmware to work with all analog LCD panels, no amplification stage is needed.

3.4.2 LCD Timing Controller

The AML6213A AV processor has a built-in LCD timing controller (TCON) that works in conjunction with the video encoder to drive analog LCD panels. The integrated TCON improves the picture quality and lower the total system cost since the external analog conversion stage is eliminated. The TCON is programmable and can be used in any small to medium size analog LCD panels. The LCD TCON also includes a dedicated VGH/VGL pulse generator for the LCD panel voltage generator. Together with some simple passive components, VGH/VGL can be generated



3.5 Peripherals

3.5.1 Card-Reader Interface

The AML6213A have an integrated hardware controller for SD/MS/MMC/xD card-reader operations. The hardware controller is capable of executing the low-level card interface protocols, computing the CRC or checksum, and transferring data to/from SDRAM. The hardware provides interface for the necessary signals (e.g. SD_CLK, SD_CMD, SD_D0-3 for SD cards) but signals like card detect and write-protect are provided using GPIO only.

3.5.2 USB Interface

AM6213A AV processor has integrated one high speed USB 2.0 OTG controller and PHY into the chip. The output USB signal (DP/DM) can drive the external USB controller (e.g. Hub, FLASH drive, camera, PC, Mac, etc.) directly. The OTG controller can acts as a high speed USB Host or USB Device or a try OTG controller.

4 Operating Conditions

4.1 DC Characteristics

Table 4-1 DC Characteristics

V_{DD} = 3.3 +/- 0.3V, T_A = 0 to 75°C

Symbol	Parameters	Condition	Min	Typ	Max	Unit
V_{IH}	High Level Input		2.0		3.3	V
V_{IL}	Low Level Input		-0.3		0.8	V
VT+	Schmitt trigger, positive going Threshold			1.5		V
VT-	Schmitt trigger, negative going threshold			0.93		
Voh	High-level output voltage	Ioh = -2.0mA to 24mA	2.4			V
Vol	Low-level output voltage	Iol = 2.0 mA to 24mA			0.4	V
I_{IH}	High-level input current	Vin = V_{DD}		10nA	1	uA
I_{IL}	Low-level input current			10nA	1	
Ioz	Tri-state output leakage current			10nA	1	
P_D	Power Dissipation	Vin = V_{DD}			0.8	W

4.2 Absolute Maximum Ratings

The table below gives the absolute maximum ratings. Exposure to stresses beyond those listed in this table may result in permanent device damage, unreliability or both.

Table 4-2 Absolute Maximum Ratings

Characteristic	Value	Unit
1.2V Core Supply Voltage	1.3	V
3.3V Pads Supply Voltage	3.8	V
Input voltage, V_I	-0.5 ~ 4.6	V
Output voltage, V_O	-0.5 ~ 4.6	V
Operating Temperature	70	°C

4.3 Recommended Operating Conditions

Table 4-3 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max	Unit
$V_{DD(CORE)}$	1.2V Core Supply Voltage	1.00	1.2	1.5	V
$V_{DD(PADS)}$	3.3V Pads Supply Voltage	3.0	3.3	3.6	V
T_J	Junction Temperature	0		125	°C

5 Pin-out

5.1 Pin-out information

The AML6213A A/V processor pin-out is described in the following table.

Abbreviations:

- I == Input digital pin, O == Output digital pin, I/O == Input/Output pin
- AI == Analog input pin, AO == Analog output pin, AIO == Analog input/output pin
- P == Power pin, AP == Analog power pin, NC == No connection

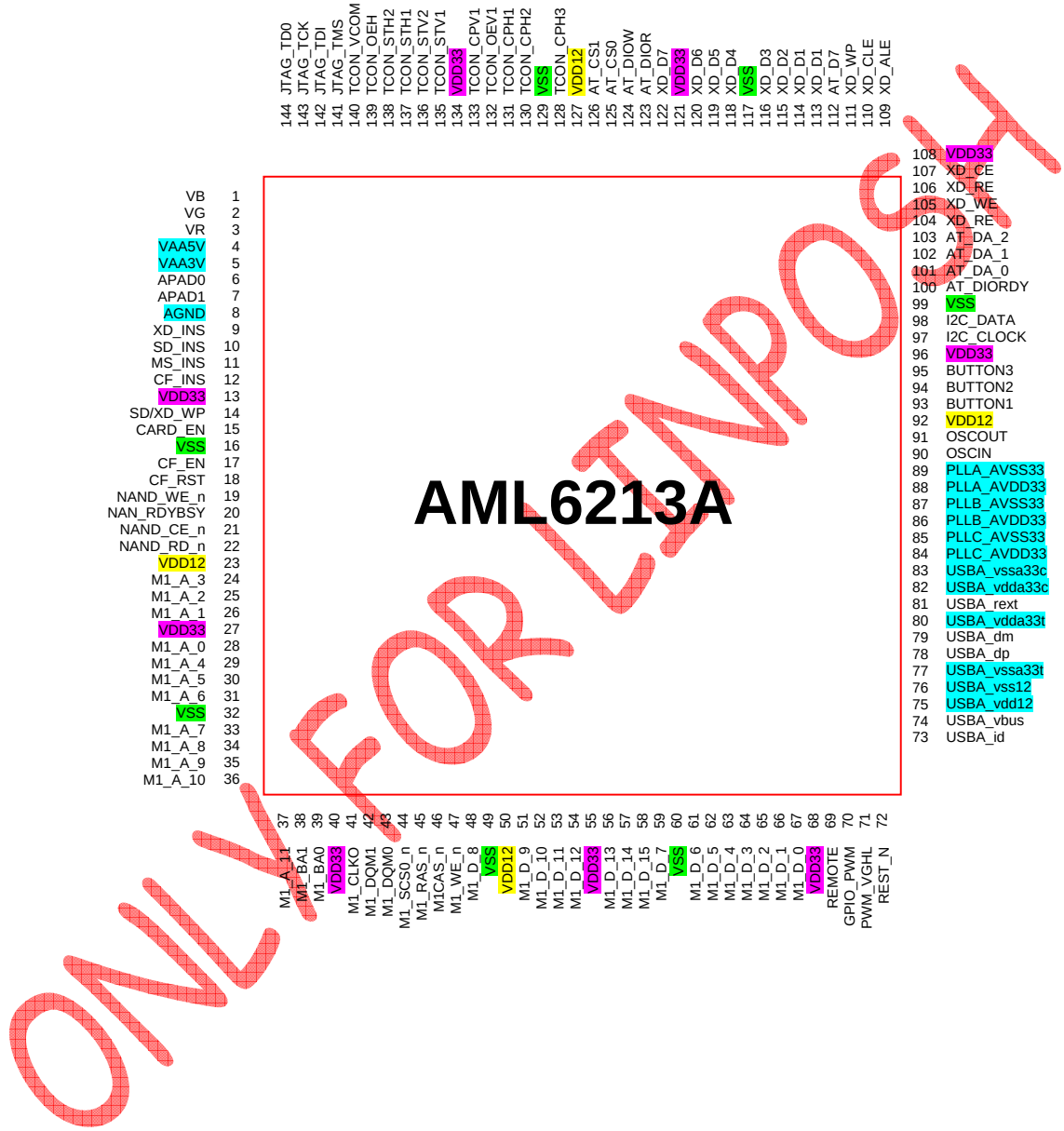
Pin #	Pin Name	Description	Alternate Usage / Comments	Type
1	VB	VDAC-B	Panel DAC for blue signal	AO
2	VG	VDAC-G	Panel DAC for Green signal	AO
3	VR	VDAC-R	Panel DAC for Red signal	AO
4	VAA5V	Analog power	5V analog power	AP
5	VAA3V	Analog power	3.3V analog power	AP
6	AL	Audio output	Audio output – LEFT	AO
7	AR	Audio output	Audio output – RIGHT	AO
8	AGND	Analog ground	Analog ground	AP
9	XD_INS	Card Reader I/O	Card Reader I/F or GPIO	I/O
10	SD_INS	Card Reader I/O	Card Reader I/F or GPIO	I/O
11	MS_INS	Card Reader I/O	Card Reader I/F or GPIO	I/O
12	CF_INS	Card Reader I/O	Card Reader I/F or GPIO	I/O
13	VDD33	Digital I/O Power	Digital I/O 3.3V power	P
14	SD/XD_WP	GPIO	GPIO	I/O
15	CARD_EN	GPIO	GPIO	I/O
16	VSS33	Digital Ground	Digital ground	P
17	CF_EN	GPIO	GPIO	I/O
18	CF_RST	GPIO	GPIO	I/O
19	NAND_WE_n	NAND Interface	NAND Interface WE or GPIO	I/O
20	NAND_RDYBSY	NAND Interface	NAND Interface RDYBSY or GPIO	I/O
21	NAND_CE_n	NAND Interface	NAND Interface CE or NOR Interface	I/O
22	NAND_RD_n	NAND Interface	NAND Interface RD or NOR Interface	I/O
23	VDD12	Digital Core Power	Digital core 1.2V power	P
24	M1_A_3	M1_A_3	SDRAM1 and/or FLASH	I/O
25	M1_A_2	M1_A_2	SDRAM1 and/or FLASH	I/O
26	M1_A_1	M1_A_1	SDRAM1 and/or FLASH	I/O
27	VDD33	Digital I/O Power	Digital I/O 3.3V power	P
28	M1_A_0	M1_A_0	SDRAM1 and/or FLASH	I/O
29	M1_A_4	M1_A_4	SDRAM1 and/or FLASH	I/O
30	M1_A_5	M1_A_5	SDRAM1 and/or FLASH	I/O
31	M1_A_6	M1_A_6	SDRAM1 and/or FLASH	I/O
32	VSS	Digital Ground	Digital ground	P
33	M1_A_7	M1_A_7	SDRAM1 and/or FLASH	I/O
34	M1_A_8	M1_A_8	SDRAM1 and/or FLASH	I/O
35	M1_A_9	M1_A_9	SDRAM1 and/or FLASH	I/O
36	M1_A_10	M1_A_10	SDRAM1 and/or FLASH	I/O

Pin	Pin name	Description	Comments / Alternate usage	Type
37	M1_A_11	M1_A_11	SDRAM1 and/or FLASH	O
38	M1_BA1	M1_BA1	SDRAM1 and/or FLASH	O
39	M1_BA0	M1_BA0	SDRAM1 and/or FLASH	O
40	VDD33	I/O Power 3.3V	Digital I/O power 3.3V	P
41	M1_CLKO	M1_CLKO	SDRAM1 and/or FLASH	O
42	M1_DQM1	M1_DQM1	SDRAM1 and/or FLASH	O
43	M1_DQM0	M1_DQM0	SDRAM1 and/or FLASH	O
44	M1_SCS0_n	M1_SCS0_n	SDRAM1 and/or FLASH	O
45	M1_RAS_n	M1_RAS_n	SDRAM1 and/or FLASH	O
46	M1_CAS_n	M1_CAS_n	SDRAM1 and/or FLASH	O
47	M1_WE_n	M1_WE_n	SDRAM1 and/or FLASH	O
48	M1_D_8	M1_D_8	SDRAM1 and/or FLASH	I/O
49	VSS	VSS	Digital ground	P
50	VDD12	Digital Core Power 1.2V	Digital core power 1.2V	P
51	M1_D_9	M1_D_9	SDRAM1 and/or FLASH	I/O
52	M1_D_10	M1_D_10	SDRAM1 and/or FLASH	I/O
53	M1_D_11	M1_D_11	SDRAM1 and/or FLASH	I/O
54	M1_D_12	M1_D_12	SDRAM1 and/or FLASH	I/O
55	VDD33	I/O Power 3.3V	Digital I/O power 3.3V	P
56	M1_D_13	M1_D_13	SDRAM1 and/or FLASH	I/O
57	M1_D_14	M1_D_14	SDRAM1 and/or FLASH	I/O
58	M1_D_15	M1_D_15	SDRAM1 and/or FLASH	I/O
59	M1_D_7	M1_D_7	SDRAM1 and/or FLASH	I/O
60	VSS	VSS	Digital ground	P
61	M1_D_6	M1_D_6	SDRAM1 and/or FLASH	I/O
62	M1_D_5	M1_D_5	SDRAM1 and/or FLASH	I/O
63	M1_D_4	M1_D_4	SDRAM1 and/or FLASH	I/O
64	M1_D_3	M1_D_3	SDRAM1 and/or FLASH	I/O
65	M1_D_2	M1_D_2	SDRAM1 and/or FLASH	I/O
66	M1_D_1	M1_D_1	SDRAM1 and/or FLASH	I/O
67	M1_D_0	M1_D_0	SDRAM1 and/or FLASH	I/O
68	VDD33	I/O Power 3.3V	Digital I/O power 3.3V	P
69	REMOTE	REMOTE	REMOTE	I/O
70	GPIO_PWM	GPIO	GPIO or PWM signal	I/O
71	PWM_VGHL	PWM_VGHL	PWM signal for generation VGH/VGL or GPO	O
72	RESET_N	RESET	Reset signal	I

Pin	Pin name	Description	Comments / Alternate usage	Type
73	USBA_id	USBA identifier	USB Mini-receptacle Identifier between mini-A/mini-B plug	AI
74	USBA_vbus	USBA mini VBUS	USB power supply pin **(5 volt)**. An off-chip charge pump is used to provide power to the VBUS pin.	AP
75	USBA_vdd12	USBA Digital 1.2V Power	Digital 1.2V power for USB-A	AP
76	USBA_vss12	USBA Digital Ground	Digital ground for USB-A	AP
77	USBA_vssa33t	USBA ground	Analog ground for USB-A transceiver	AP
78	USBA_dp	USBA D+	D+ analog signal from the USB cable	A
79	USBA_dm	USSA D-	D- analog signal from the USB cable	A
80	USBA_vdda33t	USBA 3.3V power	Analog 3.3V power for USB-A transceiver	AP
81	USBA_rext	USBA Ext Ref resistor	External resistor that controls the bias current for USB	AP
82	USBA_vdda33c	USBA 3.3V power	Analog 3.3V power for USB-A core	AP
83	USBA_vssa33c	USBA ground	Analog ground for USB-A core	AP
84	PLLC_AVDD33	PLL VDD	PLL power	AP
85	PLLC_AVSS33	PLL Ground	PLL ground	AP
86	PLLB_AVDD33	PLL VDD	PLL power	AP
87	PLLB_AVSS33	PLL Ground	PLL ground	AP
88	PLLA_AVDD33	PLL VDD	PLL power	AP
89	PLLA_AVSS33	PLL Ground	PLL ground	AP
90	OSCIN	OSC Input	27MHz crystal oscillator input	I
91	OSCOUT	OSC Output	27MHz crystal oscillator output	O
92	VDD12	Digital Core Power	Digital core 1.2V power	P
93	BUTTON1	GPIO (Interrupt GPIO)	GPIO and misc	I/O
94	BUTTON2	GPIO (Interrupt GPIO)	GPIO and misc	I/O
95	BUTTON3	GPIO (Interrupt GPIO)	GPIO and misc	I/O
96	VDD33	Digital I/O Power	Digital I/O 3.3V power	P
97	I2C_CLOCK	I2C interface	I2C interface and GPIO and misc	I/O
98	I2C_DATA	I2C interface	I2C interface and GPIO and misc	I/O
99	VSS	Digital Ground	Digital ground	P
100	AT_DIORDY	Card Reader I/O	Card Reader I/F or GPIO	I/O
101	AT_DA_0	Card Reader I/O	Card Reader I/F or GPIO	I/O
102	AT_DA_1	Card Reader I/O	Card Reader I/F or GPIO	I/O
103	AT_DA_2	Card Reader I/O	Card Reader I/F or GPIO	I/O
104	XD_RE	Card Reader I/O	Card Reader I/F or GPIO	I/O
105	XD_WE	Card Reader I/O	Card Reader I/F or GPIO	I/O
106	XD_RB	Card Reader I/O	Card Reader I/F or GPIO	I/O
107	XD_CE	Card Reader I/O	Card Reader I/F or GPIO	I/O
108	VDD33	Digital I/O Power	Digital I/O 3.3V power	P

Pin	Pin name	Description	Comments / Alternate usage	Type
109	XD_ALE	Card Reader I/O	Card Reader I/F or GPIO	I/O
110	XD_CLE	Card Reader I/O	Card Reader I/F or GPIO	I/O
111	XD_WP	Card Reader I/O	Card Reader I/F or GPIO	I/O
112	CARD_EN	Card Reader I/O	Card Reader I/F or GPIO	I/O
113	XD_D0	Card Reader I/O	Card Reader I/F or GPIO	I/O
114	XD_D1	Card Reader I/O	Card Reader I/F or GPIO	I/O
115	XD_D2	Card Reader I/O	Card Reader I/F or GPIO	I/O
116	XD_D3	Card Reader I/O	Card Reader I/F or GPIO	I/O
117	VSS	Digital Ground	Digital ground	P
118	XD_D4	Card Reader I/O	Card Reader I/F or GPIO	I/O
119	XD_D5	Card Reader I/O	Card Reader I/F or GPIO	I/O
120	XD_D6	Card Reader I/O	Card Reader I/F or GPIO	I/O
121	VDD33	Digital I/O Power	Digital I/O 3.3V power	P
122	XD_D7	Card Reader I/O	Card Reader I/F or GPIO	I/O
123	AT_DIOR	Card Reader I/O	Card Reader I/F or GPIO	I/O
124	AT_DIOW	Card Reader I/O	Card Reader I/F or GPIO	I/O
125	AT_CS0	Card Reader I/O	Card Reader I/F or GPIO	I/O
126	AT_CS1	Card Reader I/O	Card Reader I/F or GPIO	I/O
127	VDD12	Digital Core Power	Digital core 1.2V power	P
128	TCON_CPH3	LCD Panel signal	LCD panel clock pulse	I/O
129	VSS	Digital Ground	Digital ground	P
130	TCON_CPH2	LCD Panel signal	LCD panel clock pulse	I/O
131	TCON_CPH1	LCD Panel signal	LCD panel clock pulse	I/O
132	TCON_OEV1	LCD Panel signal	LCD panel clock pulse	I/O
133	TCON_CPV1	LCD Panel signal	LCD panel clock pulse	I/O
134	VDD33	Digital I/O Power	Digital I/O 3.3V power	P
135	TCON_STV1	LCD Panel signal	LCD panel clock pulse	I/O
136	TCON_STV2	LCD Panel signal	LCD panel clock pulse	I/O
137	TCON_STH1	LCD Panel signal	LCD panel clock pulse	I/O
138	TCON_STH2	LCD Panel signal	LCD panel clock pulse	I/O
139	TCON_OEH	LCD Panel signal	LCD panel clock pulse	I/O
140	TCON_VCOM	LCD Panel signal	LCD panel clock pulse	I/O
141	JTAG_TMS	JTAG TMS	JTAG	I/O
142	JTAG_TDI	JTAG TDI	JTAG	I/O
143	JTAG_TCK	JTAG TCK	JTAG	I/O
144	JTAG_TDO	JTAG TDO	JTAG	I/O

5.2 Package pin-out diagram



5.3 Multiple usage pins

Multiple usage pins are used to converse pin consumption for different features. The AML6213A devices can be used in many different applications but each application will not utilize all the on chip features. As a result, some of the features share the same pin. Most of the multiple usage pins can be a GPIO pin also.

The following tables illustrate the applications of the multiple usage pins.

5.3.1 Card Reader interface multi-function pins

Pin#	Package Pin Name	xD	SD/MMC	MS	CF/MD	GPIO
100	AT_DIORDY				AT_DIORDY	AT_GPIO26
101	AT_DA_0				AT_DA_0	AT_GPIO16
102	AT_DA_1				AT_DA_1	AT_GPIO17
103	AT_DA_2				AT_DA_2	AT_GPIO18
104	XD_RE	XD_RE			AT_D0	AT_GPIO0
105	XD_WE	XD_WE			AT_D1	AT_GPIO1
106	XD_READY	XD_READY			AT_D2	AT_GPIO2
107	XD_CE	XD_CE			AT_D3	AT_GPIO3
109	XD_ALE	XD_ALE			AT_D4	AT_GPIO4
110	XD_CLE	XD_CLE			AT_D5	AT_GPIO5
111	XD_WP	XD_WP	SD_WP		AT_D6	AT_GPIO6
112	AT_D7	CARD_EN	CARD_EN	CARD_EN	AT_D7	AT_GPIO7
113	XD_D0	XD_D0			AT_D8	AT_GPIO8
114	XD_D1	XD_D1			AT_D9	AT_GPIO9
115	XD_D2	XD_D2	SD_CMD	MS_STB	AT_D10	AT_GPIO10
116	XD_D3	XD_D3	SD_CLK	MS_CLK	AT_D11	AT_GPIO11
118	XD_D4	XD_D4	SD_D0	MS_D0	AT_D12	AT_GPIO12
119	XD_D5	XD_D5	SD_D1	MS_D1	AT_D13	AT_GPIO13
120	XD_D6	XD_D6	SD_D2	MS_D2	AT_D14	AT_GPIO14
122	XD_D7	XD_D7	SD_D3	MS_D3	AT_D15	AT_GPIO15
123	AT_DIOR				AT_DIOR	AT_GPIO26_INTR
123	AT_DIOW				AT_DIOW	AT_GPIO25_INTR
125	AT_CS0				AT_CS0	AT_GPIO20_INTR
126	AT_CS1				AT_CS1	AT_GPIO21_INTR
9	XD_INS	XD_INS				LCD_GPIO_0_INTR
10	SD_INS		SD_INS			LCD_GPIO_1_INTR
11	MS_INS			MS_INS		LCD_GPIO_2_INTR
12	CF_INS				CF_INS	LCD_GPIO_3_INTR
14	SD/XD_WP	XD_WP	SD_WP			LCD_GPIO_4_INTR
15	CARD_EN	CARD_EN	CARD_EN	CARD_EN		LCD_GPIO_5_INTR
17	CF_EN				CF_EN	LCD_GPIO_6_INTR
18	CF_RST				CF_RST	LCD_GPIO_7_INTR

5.3.2 LCD TCON interface multi-function pins

Pin#	Package Pin Name	LCD TCON	MISC	GPIO
71	PWM_VGHL	PWM_VGHL		LCD_GPIO_20
128	TCON_CPH3	TCON_CPH1/2/3	I2C_MSTR_CLK	LCD_GPIO_21
130	TCON_CPH2	TCON_CPH1/2/3	ISC_MSTR_DATA	LCD_GPIO_22
131	TCON_CPH1	TCON_CPH1/2/3	PWM_VGHL	LCD_GPIO_23
132	TCON_OEV1	TCON_OEV1		LCD_GPIO_24
133	TCON_CPV1	TCON_CPV1		LCD_GPIO_25
135	TCON_STV1	TCON_STV1		LCD_GPIO_26
136	TCON_STV2	TCON_STV2		LCD_GPIO_27
137	TCON_STH1	TCON_STH1		LCD_GPIO_28
138	TCON_STH2	TCON_STH2		LCD_GPIO_29
139	TCON_OEH	TCON_OEH		LCD_GPIO_30
140	TCON_VCOM	TCON_VCOM		LCD_GPIO_31

5.3.3 Misc interface multi-function pins

Pin#	Package Pin Name	Main Function	Other Functions	GPIO
69	REMOTE	IR Remote Input		GPIO_0_INTR
70	GPIO_PWM		PWM_B	GPIO_1_INTR
97	I2C_CLOCK	I2C Master Clock	UART_TX	AT_GPIO23
98	I2C_DATA	I2C Master Data	UART_RX	AT_GPIO22

5.3.4 JTAG interface multi-function pins

Pin#	Package Pin Name	JTAG	MISC	GPIO
141	JTAG_TMS	JTAG_TMS	I2C_MSTR_CLK	JTAG_GPIO_1
142	JTAG_TDI	JTAG_TDI	I2C_MSTR_DATA	JTAG_GPIO_2
143	JTAG_TCK	JTAG_TCK	UART_RX	JTAG_GPIO_0
144	JTAG_TDO	JTAG_TDO	UART_TX	JTAG_GPIO_3

5.3.5 FLASH and m1_* interface multi-function pins

Pin#	Package Pin Name	SDRAM Memory Interface Usage (16bits wide only)	NAND FLASH Usage (8-bits wide or 16-bits wide)	NOR FLASH Usage (8-bits wide, maximum of 8Mbytes)	MISC
19	NAND_WE_n		NAND_WE_n		EGPIO_8
20	NAND_RDYBSY		NAND_RDY_BSY		EGPIO_9
21	NAND_CE_n		NAND_CE_n	FLASH_CS_n	
22	NAND_RD_n		NAND_RD_n	FLASH_OE_n	
24	M1_A_3	M1_A_3		FLASH_A_3	
25	M1_A_2	M1_A_2		FLASH_A_2	
26	M1_A_1	M1_A_1		FLASH_A_1	
28	M1_A_0	M1_A_0		FLASH_A_0	
29	M1_A_4	M1_A_4		FLASH_A_4	
30	M1_A_5	M1_A_5		FLASH_A_5	
31	M1_A_6	M1_A_6		FLASH_A_6	
33	M1_A_7	M1_A_7		FLASH_A_7	
34	M1_A_8	M1_A_8		FLASH_A_8	
35	M1_A_9	M1_A_9		FLASH_A_9	
36	M1_A_10	M1_A_10		FLASH_A_10	
37	M1_A_11	M1_A_11		FLASH_A_11	
38	M1_BA1	M1_BA1			
39	M1_BA0	M1_BA0			
41	M1_CLKO	M1_CLKO			
42	M1_DQM1	M1_DQM1		FLASH_A_21	
43	M1_DQM0	M1_DQM0		FLASH_A_20	
44	M1_SCS0_n	M1_SCS0_n			
45	M1_RAS_n	M1_RAS_n		FLASH_A_22	
46	M1_CAS_n	M1_CAS_n			
47	M1_WE_n	M1_WE_n		FLASH_WE_n	
48	M1_D_8	M1_D_8	NAND_8	FLASH_A_12	
51	M1_D_9	M1_D_9	NAND_9	FLASH_A_13	
52	M1_D_10	M1_D_10	NAND_10	FLASH_A_14	
53	M1_D_11	M1_D_11	NAND_11	FLASH_A_15	
54	M1_D_12	M1_D_12	NAND_12	FLASH_A_16	
56	M1_D_13	M1_D_13	NAND_13	FLASH_A_17	
57	M1_D_14	M1_D_14	NAND_14	FLASH_A_18	
58	M1_D_15	M1_D_15	NAND_15	FLASH_A_19	
59	M1_D_7	M1_D_7	NAND_7	FLASH_D_7	
61	M1_D_6	M1_D_6	NAND_6	FLASH_D_6	
62	M1_D_5	M1_D_5	NAND_5	FLASH_D_5	
63	M1_D_4	M1_D_4	NAND_4	FLASH_D_4	
64	M1_D_3	M1_D_3	NAND_3	FLASH_D_3	
65	M1_D_2	M1_D_2	NAND_2	FLASH_D_2	

66	M1_D_1	M1_D_1	NAND_1	FLASH_D_1	
67	M1_D_0	M1_D_0	NAND_0	FLASH_D_0	

6 Mechanical Specifications

The AML6213A A/V processor is packaged using a 144 pins PQFP package. The mechanical dimensions are given in millimeters as below: