H5TQ2G83BFR

The H5TQ2G43BFR-xxC, H5TQ2G83BFR-xxC and H5TQ2G63BFR-xxC are a 2,147,483,648-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. SK Hynix 2Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

Features

VDD=VDDQ=1.5V +/- 0.075V
Fully differential clock inputs (CK, /CK) operation
Differential Data Strobe (DQS, /DQS)
On chip DLL align DQ, DQS and /DQS transition with CK transition
DM masks write data-in at the both rising and falling edges of the data strobe
All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
Programmable CAS latency 6, 7, 8, 9, 10 and (11) supported
Programmable additive latency 0, CL-1, and CL-2 supported
Programmable CAS Write latency (CWL) = 5, 6, 7, 8
Programmable burst length 4/8 with both nibble sequential and interleave mode
BL switch on the fly
8banks
Average Refresh Cycle (Tcase of 0 °C~ 95 °C)
- .8 μs at 0°C ~ 85 °C
- 3.9 μs at 85°C ~ 95 °C
Auto Self Refresh supported
JEDEC standard 82ball FBGA(x4/x8), 96ball FBGA (x16)
Driver strength selected by EMRS
Dynamic On Die Termination supported
Asynchronous RESET pin supported
ZQ calibration supported
TDQS (Termination Data Strobe) supported (x8 only)

Write Levelization supported

8 bit pre-fetch

This product in compliance with the RoHS directive.

Technical Data Sheet

Part Number	Rev.	Update Date	Remark
H5TQ2G83BFR (/product/filedata/fileDownload.do?seq=2292)	1.1	2010-06-24	

Simulation Model

Part Number	Rev.	Update Date	Remark
IBIS (/product/filedata/fileDownload.do?seq=2293)	1.6	2010-03-05	
Verilog (/product/filedata/fileDownload.do?seq=2294)	1.5	2010-05-13	
HSpice (/product/filedata/fileDownload.do?seq=2295)	1.5	2010-05-13	

Device Operation

Part Number	Update Date
DDR3_device_operation_timing_diagram.pdf (/product/filedata/fileDownload.do?seq=2296)	2010-03-04

Speed

Part Number	Speed
G7	1066 7-7-7
H9	1333 9-9-9
PB	1600 11-11-11
RD	1866 13-13-13