SDR SDRAM

H57V2562GTR

The SK Hynix H57V2562GTR Synchronous DRAM is 268,435,456bit CMOS Synchronous DRAM, ideally suited for the consumer memory applications which requires large memory density and high bandwidth. It is organized as 4banks of 4,194,304 x 16 I/O.

Synchronous DRAM is a type of DRAM which operates in synchronization with input clock. The SK Hynix Synchronous DRAM latch each control signal at the rising edge of a basic input clock (CLK) and input/output data in synchronization with the input clock (CLK).

The address lines are multiplexed with the Data Input/ Output signals on a multiplexed x16 Input/ Output bus.

All the commands are latched in synchronization with the rising edge of CLK.The Synchronous DRAM provides for programmable read or write Burst length of Programmable burst lengths: 1, 2, 4, 8 locations or full page.

An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access. The Synchronous DRAM uses an internal pipelined architecture to achieve high-speed operation.

This architecture is compartible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, randon-access operation.

Read and write accesses to the SK Hynix Synchronous DRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access. All inputs are LVTTL compatible. Devices will have a VDD and VDDQ supply of 3.3V (nominal).

Features

Standard SDRAM Protocol

Internal 4bank operation

Power Supply Voltage : VDD = 3.3V, VDDQ = 3.3V

All device pins are compatible with LVTTL interface

Low Voltage interface to reduce I/O power

8,192 Refresh cycles / 64ms

Programmable CAS latency of 2 or 3

Programmable Burst Length and Burst Type

- 1, 2, 4, 8 or full page for Sequential Burst

- 1, 2, 4 or 8 for Interleave Burst

Commercial Temp : 0oC ~ 70oC Operation\

Package Type : 54_Pin TSOPII

This product is in compliance with the directive pertaining of RoHS.

Technical Data Sheet

Part Number	Rev.	Update Date	Remark
H57V2562GTR (/product/filedata/fileDownload.do?seq=4558)	1.0	2010-12-15	
H57V2562GTR-xI (/product/filedata/fileDownload.do?seq=4559)	1.0	2010-12-15	IT-Part

Simulation Model

Part Number	Rev.	Update Date	Remark
IBIS (/product/filedata/fileDownload.do?seq=4560)	1.0	2009-08-10	
Verilog (/product/filedata/fileDownload.do?seq=4561)	1.0	2009-08-10	
HSpice (/product/filedata/fileDownload.do?seq=4562)	1.0	2009-08-10	

Speed

Part Number	Speed
60	166MHz, 3-3-3
70	133MHz, 3-3-3