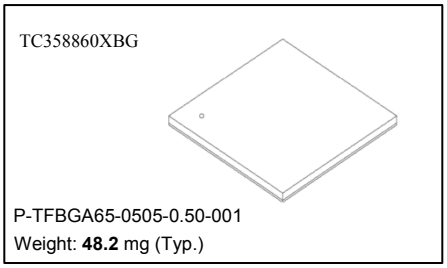
CMOS Digital Integrated Circuit Silicon Monolithic

TC358860XBG

Mobile Peripheral Devices



P-TFBGA65-0505-0.50-001
Weight: **48.2** mg (Typ.)

Overview

TC358860XBG converts an Embedded Display Port (eDP™) video stream into an MIPI® DSI stream. There are four eDP main link lanes in TC358860XBG, they can toggle at either 1.62, 2.16, 2.43, 2.7, 3.24, 4.32, 4.86 or 5.4 Gbps/link to receive up to 17.28 Gbps (5.4 Gbps * 0.8 * 4) of video stream. The 4-data lanes dual link DSI Tx can transmit up to 8 Gbps (1 Gbps * 4 * 2) of video stream.

For input video stream with bandwidth (BW) < 4 Gbps, TC358860XBG can output the video data either with a single DSI link or performs left-right line split to output the video data stream with dual DSI links. For input video stream with BW requirements between 4 Gbps and 8 Gbps, left-right line split and dual DSI links usage is necessary.

TC358860XBG provides a compression engine which compress video data with 2-to-1 ratio. This enables TC358860XBG to receive 4K @60fps video streams at eDP Rx, compress and send out to a dual DSI link 4K panel for display. A de-compress engine is expected in the DSI panel.

Host/eDPTx controls/configures TC358860XBG chip by using its AUX channel (I^2C over AUX). TC358860XBG provides mail box register/command queue for host to control/configure/command DSI panels, too. After host writes to the command queue, TC358860XBG starts DSI "command packets" to communicate with the DSI panels.

Alternatively, an external I^2C master can configure TC358860XBG via I^2C bus. Command queue address can also be access via I^2C bus, which means Host can use I^2C to access command queue, which in turn, controls DSI panel parameters.

Please note that host can not use both AUX ch. and I^2C bus for register setting simultaneously.

Features

● TC358860XBG follows the following standards:
- ✧ MIPI Alliance Specification for Display Serial Interface (DSI) version 1.1, Nov 22 2011
- ✧ MIPI Alliance Specification for D-PHY Version 1.1, Nov 7 2011
- ✧ VESA DisplayPort Standard version 1.2a, May 23 2012.
- ✧ VESA Embedded DisplayPort Standard version 1.4 Feb. 28 2013

● eDP Sink (Receiver)
- ✧ Bit Rate @ 1.62, 2.16, 2.43, 2.7, 3.24, 4.32, 4.86 or 5.4Gbps, Voltage Swing @0.2 to 1.2 V, Pre-Emphasis Level @3.5dB.
- ✧ There are four lanes available in eDP main Link, which can operate in 1-, 2- or 4-lane configuration.
- ✧ Support Single-Stream Transport (SST), not multi-Stream Transport (MST)
- ✧ Capable of Full and Fast Link Training
- ✧ AUX channel with nominal bit rate at 1 Mbps.
- ✧ Video input data formats supported: RGB666 and RGB888
- ✧ Absolute maximum pixel rate is 600 Mpixel/s.
- ✧ Support Alternate Scrambler Seed Reset (ASSR) is used for content protection, Does not support HDCP encryption.
  - System designer can connect ASSR_Disable Pad to GND, which prevents eDPTx (Source device) to disable ASSR mode TC358860XBG.
  - In order words, when ASSR_Disable Pad is grounded, the Source device cannot clear the ALTERNATE_SCRAMBER_RESET_ENABLE bit of the eDP_CONFIGURATION_SET register (DPCD Address 0010Ah, bit 0) to 0.
- ✧ No audio SDP, Multi-touch and Backlight DPCD registers support
- ✧ Support REFCLK from 24 MHz to 40 MHz with 1.0 MHz step.

● DSI Transmitter
- ✧ Dual 4-Data Lane DSI Links with Bi-direction support at Data Lane 0. Each link can be used in 1-, 2-, 3- or 4-data lane configuration. Maximum speed at 1.0 Gbps/lane.
- ✧ No deep color support, Video input data formats: RGB666 and RGB888

- TC358860XBG performs dithering for RGB888 video stream to RGB666 panel
- TC358860XBG appends MSB bits of RGB666 video stream (RGB[5:0] ➔ {RGB[5:0], RGB[5:4]) to RGB888 panel

✧ Interlaced video mode is not supported.

✧ Dual links with Left-Right split: DSI0 carries the left half data of eDP Rx video stream and DSI1 carries the right one

- DSI0 can be assigned/programmed to either DSITx port.
- The maximum length of each half is limited to 2048-pixel plus up to 32-pixel overlap.
- The skew (DSI1 delay w.r.t. to DSI0) between DSI0 and DSI1 can be programmed by register

✧ Provide path for eDP host/transmitter to control TC358860XBG and its attached panel.

✧ Built in Color Bar Generator to verify Dual DSI link without eDPRx input.

✧ DSITx operates in video mode when video stream is continuously received at eDPRx port.

● Video function

✧ Compression engine : 2 to 1 compression for 4k2k resolution

✧ Magic square

✧ Color bar output for debug

● I^2C Slave Port

✧ Support for normal (100 kHz), fast (400 kHz or 1 MHz, if SysClk is running at 25 MHz) modes.

✧ External I^2C master can access TC358860XBG internal and DPCD registers and read/write DSI panel register (via DSI link).

✧ Address auto increment is supported.

✧ TC358860XBG Slave Port address is 0x68, (binary 1101_000x) where x = 1 for read and x = 0 for write. The slave address can be changed to 0x0E (binary 0001_110x) by a weak pull up to pin HPD during boot time.

● Power Supply

✧ MIPI D-PHY 1.2 V

✧ Core, MIPI D-PHY and eDP-PHY 1.1 V

✧ eDP-PHY: 1.8 V

✧ I/O: 1.8 V or 3.3 V (all IO pins must be same power level)

✧ HPD Output Pad 1.8 V or 3.3 V

● Power Consumption (Typical Condition)

✧ 130 mW

- Condition: Input 5.4 Gbps eDP 1 lane, Output DSI port 4 data lane, Full HD@60fps resolution,24 bpp

● Packaging

✧ 65-pin FBGA Package with 0.5 mm ball pitch

✧ 5 x 5 mm^2

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This Notice of Disclaimer applies to all DSI input and processing paths related descriptions throughout this document.

REFERENCES

1. MIPI D-PHY, “MIPI Alliance Specification for D-PHY Version 1.00.00 14-May-2009"
2. MIPI Alliance Standard for DSI Version 1.02.00 – 28 June 2010
3. VESA DisplayPort Standard (Version 1, Revision 2a May 23, 2012)
4. VESA Embedded DisplayPort (eDP) Standard (Version 1.4 February 28, 2013)
5. I^2C bus specification, version 2.1, January 2000, Philips Semiconductor

1. Introduction

This Functional Specification defines operation of TC358860XBG chip, which converts an Embedded Display Port (eDP) video stream into an MIPI DSI stream. There are four eDP main link lanes in TC358860XBG, they can toggle at either 1.62, 2.16, 2.43, 2.7, 3.24, 4.32, 4.86 or 5.4 Gbps/link to receive up to 17.28 Gbps (5.4 Gbps * 0.8 * 4) of video stream. The 4-data lanes dual link DSI Tx can transmit up to 8 Gbps (1 Gbps * 4 * 2) of video stream.

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Please note that host can not use both AUX ch. and I^2C bus for register setting simultaneously.

The target system diagram and TC358860XBG block diagram are shown in Figure 1.1 and Figure 1.2, respectively.

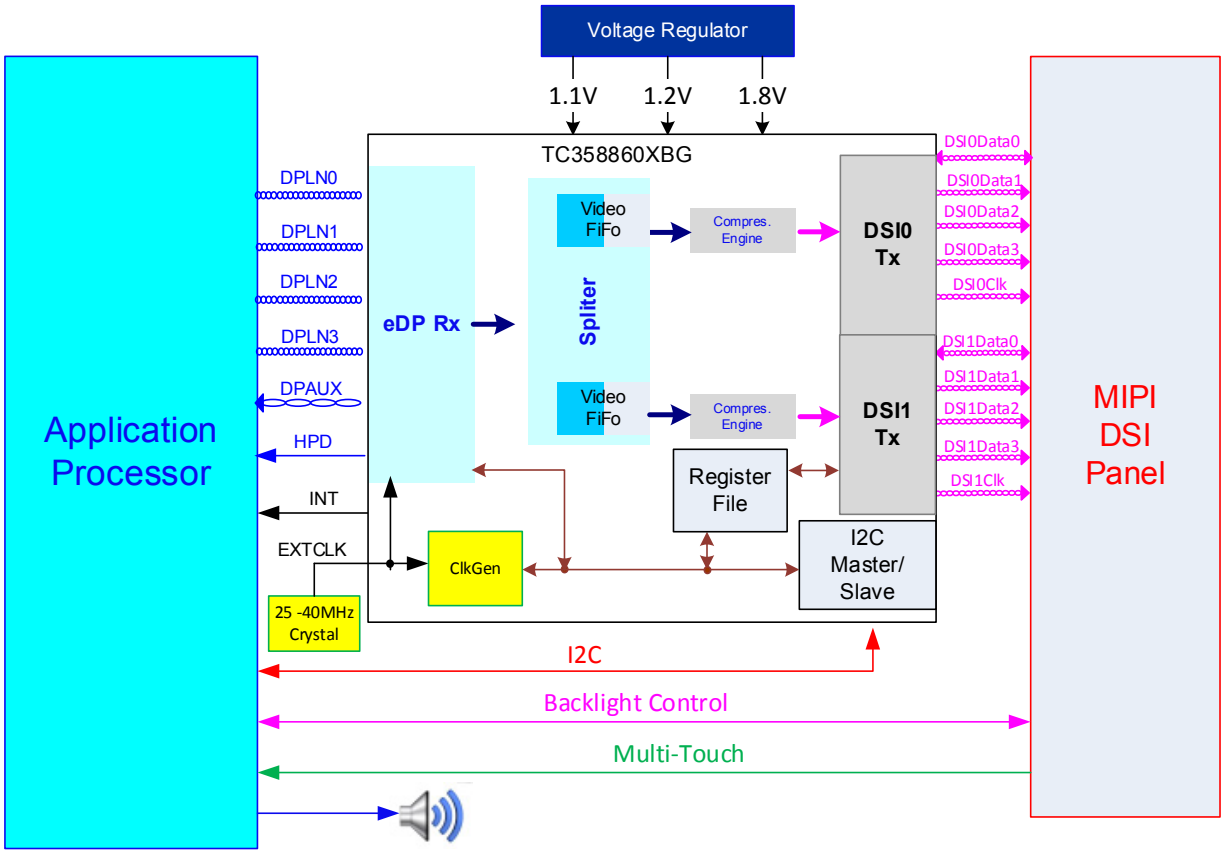

Figure 1.1 TC358860XBG in System Application

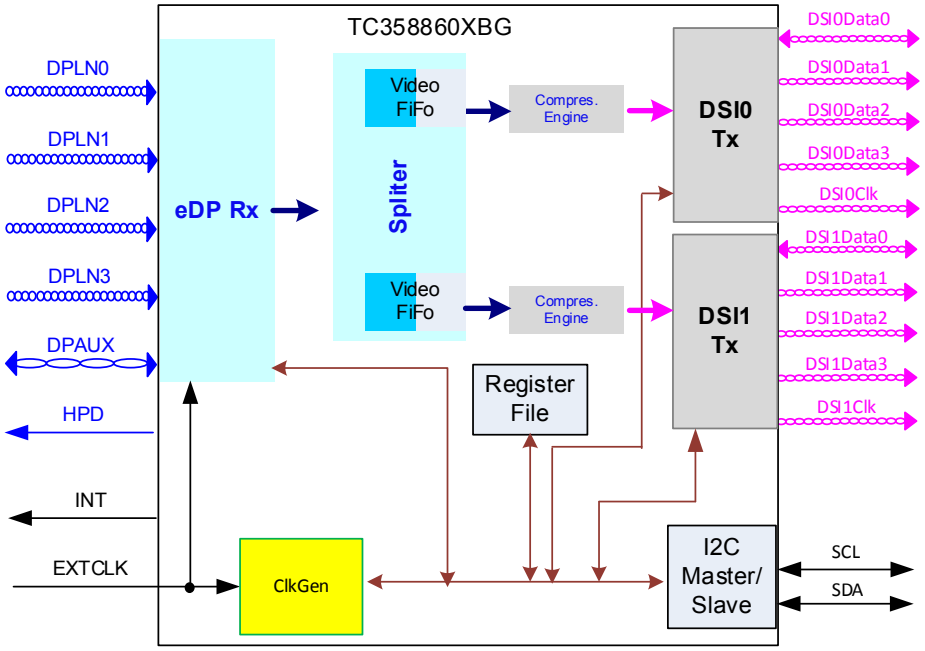

Figure 1.2 TC358860XBG Block Diagram and Functional

2. Features

- TC358860XBG follows the following standards:
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  - ✧ MIPI Alliance Specification for D-PHY Version 1.1, Nov 7 2011
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  - ✧ Bit Rate @ 1.62, 2.16, 2.43, 2.7, 3.24, 4.32, 4.86 or 5.4Gbps, Voltage Swing @0.2 to 1.2 V, Pre-Emphasis Level @3.5dB.
  - ✧ There are four lanes available in eDP main Link, which can operate in 1-, 2- or 4-lane configuration.
  - ✧ Support Single-Stream Transport (SST), not multi-Stream Transport (MST)
  - ✧ Capable of Full and Fast Link Training
  - ✧ AUX channel with nominal bit rate at 1 Mbps.
  - ✧ Video input data formats supported: RGB666 and RGB888
  - ✧ Absolute maximum pixel rate is 600Mpixel/s.
  - ✧ Does not support HDCP encryption, Alternate Scrambler Seed Reset (ASSR) is used for content protection.
    - System designer can connect ASSR_Disable Pad to GND, which prevents eDPTx (Source device) to disable ASSR mode TC358860XBG.
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  - ✧ No audio SDP, Multi-touch and Backlight DPCD registers support
  - ✧ Support REFCLK from 24 MHz to 40 MHz with 1.0 MHz step.

- DSI Transmitter
  - ✧ Dual 4-Data Lane DSI Links with Bi-direction support at Data Lane 0. Each link can be used in 1-, 2-, 3- or 4-data lane configuration. Maximum speed at 1.0 Gbps/lane.
  - ✧ No deep color support, Video input data formats: RGB666 and RGB888
    - TC358860XBG performs dithering for RGB888 video stream to RGB666 panel
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  - ✧ Interlaced video mode is not supported.
  - ✧ Dual links with Left-Right split: DSI0 carries the left half data of eDP Rx video stream and DSI1 carries the right one
    - DSI0 can be assigned/programmed to either DSITx port.
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  - ✧ Built in Color Bar Generator to verify Dual DSI link without eDPRx input.
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- Video function
  - ✧ Compression engine : 2 to 1 compression

- ✧ Magic square
- ✧ Color bar output for debug

- I^2C Slave Port
  - ✧ Support for normal (100 kHz), fast (400 kHz or 1 MHz, if SysClk is running at 25 MHz) modes.
  - ✧ External I^2C master can access TC358860XBG internal and DPCD registers and read/write DSI panel register (via DSI link).
  - ✧ Address auto increment is supported.
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- Power Supply
  - ✧ MIPI D-PHY 1.2 V
  - ✧ Core, MIPI D-PHY and eDP-PHY 1.1 V
  - ✧ eDP-PHY: 1.8 V
  - ✧ I/O: 1.8 V or 3.3 V (all IO pins must be same power level)
  - ✧ HPD Output Pad 1.8 V or 3.3 V

- Power Consumption (Typical Condition)
  - ✧ 130 mW
    - Condition: Input 5.4 Gbps eDP 1 lane, Output DSI port 4 data lane, Full HD@60fps resolution,24 bpp

- Packaging
  - ✧ 65-pin FBGA Package with 0.5 mm ball pitch
  - ✧ 5 x 5 mm^2

3. External Pins

3.1. Pinout Description

The following table gives the signals of TC358860XBG and their function.

Table 3.1 TC358860XBG Functional Signal List

Group	Pin Name	I/O	Type	Initial	Function	Power Supply
SYSTEM (8)	RESET_N	I	SCH	I	System Reset – active Low	1.8 or 3.3 V
	EXTCLK	I	SCH	I	Either 24 to 40 MHz Ref Clock	1.8 or 3.3 V
	DIS_ASSR	I	Normal	I	1: Source device can Disable ASSR 0: Source device cannot Disable ASSR	1.8 or 3.3 V
	INT	O	Normal	O	Interrupt	1.8 or 3.3 V
	GPIO[3:0]	I/O	Normal	I	GPIO, in case of no-use, tie to GND	1.8 or 3.3 V
DSI0Tx (10)	DSI0CP	O	MIPI-DPHY	O	MIPI-DSI0 Tx Clock Lane Positive	1.2 V
	DSI0CM	O	MIPI-DPHY	O	MIPI-DSI0 Tx Clock Lane Negative	1.2 V
	DSI0DP_0	I/O	MIPI-DPHY	O	MIPI-DSI0 Tx Data Lane0 Positive	1.2 V
	DSI0DM_0	I/O	MIPI-DPHY	O	MIPI-DSI0 Tx Data Lane0 Negative	1.2 V
	DSI0DP_3,2,1	O	MIPI-DPHY	O	MIPI-DSI0 Tx Data Lane Positive	1.2 V
	DSI0DM_3,2,1	O	MIPI-DPHY	O	MIPI-DSI0 Tx Data Lane Negative	1.2 V
DSI1Tx (10)	DSI1CP	O	MIPI-DPHY	O	MIPI-DSI1 Tx Clock Lane Positive	1.2 V
	DSI1CM	O	MIPI-DPHY	O	MIPI-DSI1 Tx Clock Lane Negative	1.2 V
	DSI1DP_0	I/O	MIPI-DPHY	O	MIPI-DSI1 Tx Data Lane0 Positive	1.2 V
	DSI1DM _0	I/O	MIPI-DPHY	O	MIPI-DSI1 Tx Data Lane0 Negative	1.2 V
	DSI1DP_3,2,1	O	MIPI-DPHY	O	MIPI-DSI1 Tx Data Lane Positive	1.2 V
	DSI1DM_3,2,1	O	MIPI-DPHY	O	MIPI-DSI1 Tx Data Lane Negative	1.2 V
eDP Rx (11)	DPLNP_3,2,1,0	I	eDP-PHY	I	eDP Output Main Link Positive	1.8 V
	DPLNM_3,2,1,0	I	eDP-PHY	I	eDP Output Main Link Negative	1.8 V
	DPAUXP	I/O	eDP-PHY	I	eDP Output AUX Channel Positive	1.8 V
	DPAUXM	I/O	eDP-PHY	I	eDP Output AUX Channel Negative	1.8 V
	HPD	O	Normal	O	eDP Rx INT/Detected Output	1.8 or 3.3 V
I2C (2)	I2C_SCL	I/O	FS/SCH	I	I^2C Clock	1.8 or 3.3 V
	I2C_SDA	I/O	FS/SCH	I	I^2C Data	1.8 or 3.3 V
TEST(4)	TM	I	Normal	I	Test Pins, tie to GND	1.8 or 3.3 V
	TEST1	I	-	I	Test Pins, tie to GND	1.8 V
	TEST2	O	Analog	O	Analog TEST , Open	-
	TEST3	I	Normal	I	Test Pins, connect to Pull-Up 1kohm	1.1 V
POWER (10)	VDDC (2)	-	-	-	VDD for internal Core	1.1 V
	VDDIO(1)	-	-	-	VDD for I/O voltage	1.8 or 3.3 V
	VDDP2(1)	-	-	-	VDD for PLL	1.1 V
	VDD_DP18(2)	-	-	-	VDD for DP PHY	1.8 V
	VDD_DP11(2)	-	-	-	VDD for DP PHY	1.1 V
	VDD_DSI0(1)	-	-	-	VDD for MIPI DPHY	1.2 V
	VDD_DSI1(1)	-	-	-	VDD for MIPI DPHY	1.2 V
GROUND (10)	VSS(10)	-	-	-	VSS for internal core/I/O, DPHY	-

Normal:	Normal IO (Programmable Output Drive Strength 2,4,8 and 12 mA)
OD:	Pseudo open-drain output, schmidtt input
FS/SCH:	Fail Safe schmidtt input buffer
MIPI-PHY:	Front-end analog IO for MIPI
eDP-PHY:	Front-end analog IO for eDP RX

Table 3.2 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	8	
DSI Tx	20	CLK + Data 4 lane x 2 port
eDP Rx	11	Data 4 lane + AUX 1 lane+ HPD
I2C	2	
TEST	4	
POWER	10	
GROUND	10	
Total	**65**	

3.2. Pin Layout

The mapping of TC358860XBG signals to the external pins is shown in the figure below.

DSI1

A1	A2	A3	A4	A5	A6	A7	A8	A9
VDD_DSI0	VDD_DSI1	DSI1DP_3	DSI1DP_2	DSI1CP	DSI1DP_1	DSI1DP_0	VDDC	VDDIO
B1	B2	B3	B4	B5	B6	B7	B8	B9
DSI0DP_0	DSI0DM_0	DSI1DM_3	DSI1DM_2	DSI1CM	DSI1DM_1	DSI1DM_0	RESET_N	DIS_ASSR
C1	C2	C3	C4	C5	C6	C7	C8	C9
DSI0DP_1	DSI0DM_1	no-ball	no-ball	no-ball	no-ball	no-ball	I2C_SDA	I2C_SCL
D1	D2	D3	D4	D5	D6	D7	D8	D9
DSI0CP	DSI0CM	no-ball	VSS	VSS	TEST1	no-ball	GPIO2	GPIO3
E1	E2	E3	E4	E5	E6	E7	E8	E9
DSI0DP_2	DSI0DM_2	no-ball	VSS	VSS	TM	no-ball	GPIO0	GPIO1
F1	F2	F3	F4	F5	F6	F7	F8	F9
DSI0DP_3	DSI0DM_3	no-ball	VSS	TEST2	TEST3	no-ball	INT	EXTCLK
G1	G2	G3	G4	G5	G6	G7	G8	G9
VDDC	VSS	no-ball	no-ball	no-ba...	no-ball	no-ball	HPD	VDDP2
H1	H2	H3	H4	H5	H6	H7	H8	H9
VSS	DPLNM_3	VSS	DPLNM_2	VSS	DPLNM_1	VSS	DPLNM_0	DPAUXM
J1	J2	J3	J4	J5	J6	J7	J8	J9
VDD_DP11	DPLNP_3	VDD_DP18	DPLNP_2	VDD_DP11	DPLNP_1	VDD_DP18	DPLNP_0	DPAUXP

DSI0

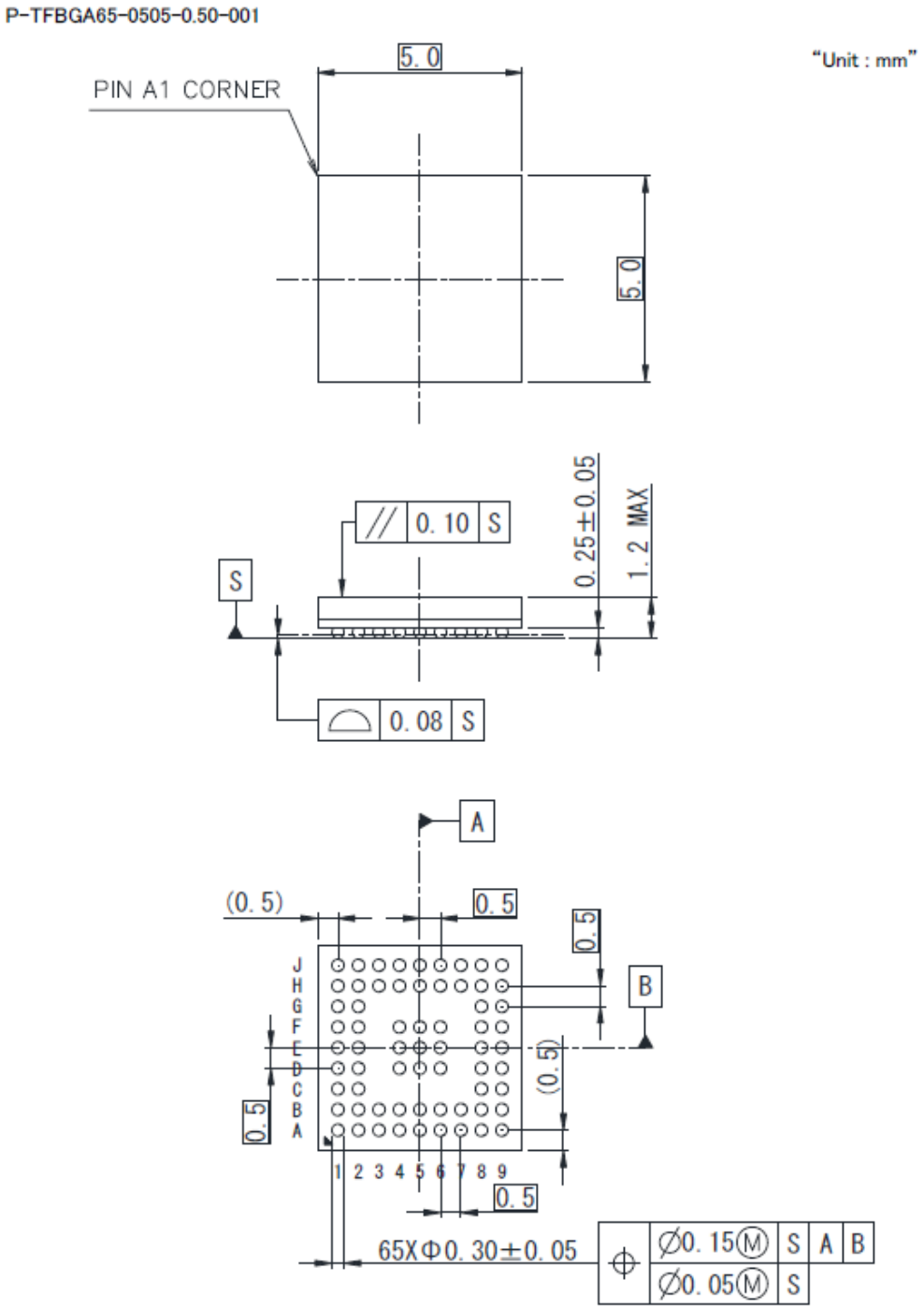
eDP

Figure 3.1 TC358860XBG Chip Pin Layout (Top view)

□	Signal(VDDIO)
□	Differential signal
□	Analog signal
□	Power
□	GND
□	No-ball or Reserved ball

4. Package

TC358860XBG housed in a 5.0 mm by 5.0 mm size package with 0.5mm ball pitch. The detailed package drawing is shown below.



Weight: 48.2 mg (Typ.)

Figure 4.1 Package Dimension

Table 4.1 Package Details

Package	Solder Ball Pitch	Solder Ball Height	Package Dimension	Package Height	Note
65-Pin	0.50 mm	0.25mm	5.0 x 5.0 mm^2	1.2mm Max	

5. Electrical characteristics

5.1. Absolute Maximum Ratings

All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

Table 5.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V – Digital IO) (3.3V – Digital IO)	VDDIO	-0.3 to +1.96 -0.3 to +3.63	V
Supply voltage (1.1V – Digital Core)	VDDC	-0.3 to +1.54	V
Supply voltage (1.2V – MIPI DSI PHY)	VDD_MIPI	-0.3 to +1.54	V
Supply voltage (1.8V – eDP PHY)	VDD_DP18	-0.3 to +1.98	V
Supply voltage (1.1V – eDP PHY)	VDD_DP11	-0.3 to +1.54	V
Input voltage (DSI I/O)	V_{IN_DSI}	-0.3 to VDD_MIPI+0.3	V
Output voltage (DSI I/O)	V_{OUT_DSI}	-0.3 to VDD_MIPI+0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 to VDDIO+0.3	V
Output voltage (Digital IO)	V_{OUT_IO}	-0.3 to VDDIO+0.3	V
Input current	Iin	-10 to +10	mA
Junction temperature	Tj	125	^{o}C
Storage temperature	T_{stg}	-40 to +125	°C

5.2. Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8 V – Digital IO)	VDDIO	1.62	1.8	1.98	V
Supply voltage (3.3 V – Digital IO)	VDDIO	2.97	3.3	3.63	V
Supply voltage (1.1V – PLL)	VDDP2	1.04	1.10	1.16	V
Supply voltage (1.1 V – Digital Core)	VDDC	1.04	1.10	1.16	V
Supply voltage (1.1 V – eDP PHY)	VDD_DP11	1.04	1.10	1.16	V
Supply voltage (1.8 V – eDP PHY)	VDD_DP18	1.71	1.8	1.89	V
Supply voltage (1.2 V – MIPI-DPHY)	VDD_MIPI0 VDD_MIPI1	1.1	1.2	1.25	V
Operating internal frequency	fopr	-	-	300	MHz
Operating temperature (ambient temperature with voltage applied)	T_a	-40	+25	+85	°C
Supply noise voltage	V_{SN}			100	mV_{pp}

5.3. DC Electrical Specification

All typical values are at normal operating conditions unless otherwise specified.

5.3.1. Normal CMOS I/Os DC Specifications

Table 5.3 Normal CMOS IOs DC Specifications

Parameter – CMOS I/Os	Symbol	Conditions	Min	Typ.	Max	Unit
Input voltage, High level Input Note1	V_{IH}	-	0.7 VDDIO	-	VDDIO + 0.3V	V
Input voltage, Low level Input Note1	V_{IL}	-	VSS -0.3V	-	0.3 VDDIO	V
Input voltage High level CMOS Schmidtt Trigger Note 1,2	V_{IHS}	-	0.7 VDDIO	-	VDDIO	V
Input voltage Low level CMOS Schmidtt Trigger Note 1,2	V_{ILS}	-	0	-	0.3 VDDIO	V
Output voltage, High level Note1, 2	V_{OH}	I_{OH} = 2/4/8/12mA	VDDIO -0.4V	-	-	V
Output voltage, Low level Note1, 2	V_{OL}	I_{OL} = 2 mA 2/4/8/12mA	-	-	0.4	V
Input leakage current, High level without Pull-down I/O pin	I_{ILH1}	V_{IN} = +VDDIO, VDDIO = 3.6 V	-	-	10	µA
Input leakage current, Low level	I_{ILL}	V_{IN} = 0 V, VDDIO = 3.6 V	-	-	10	µA

Note1: Each power source is operating within recommended operating condition.

Note2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

5.3.2. MIPI DSI I/Os DC Specifications

Timing specification below has been ported from MIPI Alliance specification for D-PHY version 01-00-00. Timing defined in MIPI Alliance specification for D-PHY version 01-00-00 has precedence over timing described in the sections below.

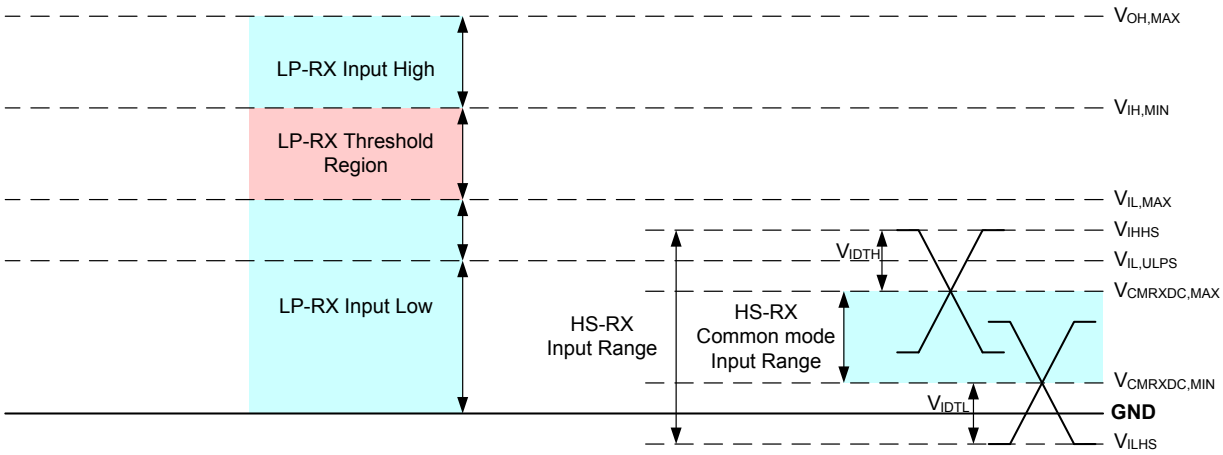


Figure 5.1 Signaling and voltage levels

Table 5.4 MIPI HSTX and LPTX DC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
HS mode						
VCMTX	HS transmit static common mode voltage	150	200	250	mV	1
|ΔVCMTX(1,0)|	VCMTX mismatch when output is Differential-1 or Differential-0	-	-	5	mV	2
|VOD|	HS transmit differential voltage	140	200	270	mV	1
|ΔVOD|	VOD mismatch when output is Differential-1 or Differential-0	-	-	14	mV	2
VOHHS	HS output high voltage	-	-	360	mV	-
ZOS	Single ended output impedance	40	50	62.5	Ω	-
ΔZOS	Single ended output impedance mismatch	-	-	10	%	-
LP Mode						
VOH	Thevenin output high level	1.1	1.2	1.25	V	-
VOL	Thevenin output low level	-50	-	50	mV	-
ZOLP	Output impedance of LP transmitter	110	-	-	Ω	3

Notes:

1. Value when driving into load impedance anywhere in the ZID range.
2. It is recommended the implementer minimize ΔVOD and ΔVCMTX(1,0) in order to minimize radiation and optimize signal integrity.
3. Though no maximum value for ZOLP is specified, the LP transmitter output impedance shall ensure the TRLP/TFLP specification is met.

Table 5.5 LPRX DC Specification

Parameter	Description	Remarks	Min	Typ.	Max	Unit
V_{IL}	Input low threshold	Not in ULPS	-	-	550	mV
V_{IL-UPS}	Input low threshold in ULPS		-	-	300	mV
V_{IH}	Output high threshold		880	-	-	mV
V_{HYST}	Input hysteresis		25	-	-	mV

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.1	2014-09-29	Newly released

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