TPS60150 5-V, 140-mA Charge-Pump

1 Features

- 2.7-V to 5.5-V Input Voltage Range
- Fixed Output Voltage of 5 V
- Maximum Output Current: 140 mA
- 1.5-MHz Switching Frequency
- Typical 90-µA Quiescent Current at No Load Condition (Skip Mode)
- X2 Charge Pump
- Hardware Enable and Disable Function
- Built-in Soft Start
- Built-in Undervoltage Lockout Protection
- Thermal and Overcurrent Protection
- Available in a 2-mm × 2-mm 6-Pin SON Package with 0.8-mm Height

2 Applications

- USB On-the-Go (OTG)
- HDMI
- Portable Communication Devices
- PCMCIA Cards
- Mobile Phones, Smart Phones
- Handheld Meters

3 Description

The TPS60150 device is a switched capacitor voltage converter that produces a regulated, low noise, and low-ripple output voltage of 5 V from an unregulated input voltage.

The 5-V output can supply a minimum of 140-mA current.

The TPS60150 device operates in skip mode when the load current falls less than 8 mA under typical condition. In skip mode operation, quiescent current is reduced to 90 µA.

Only 3 external capacitors are needed to generate the output voltage, therefore saving PCB space.

Inrush current is limited by the soft-start function during power on and power transient states.

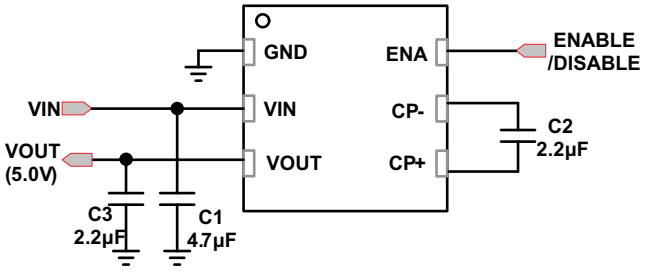
The TPS60150 device operates over a free-air temperature range of –40°C to 85°C. The device is available with a small 2-mm × 2-mm 6-pin SON package (QFN).

Device Information(1)

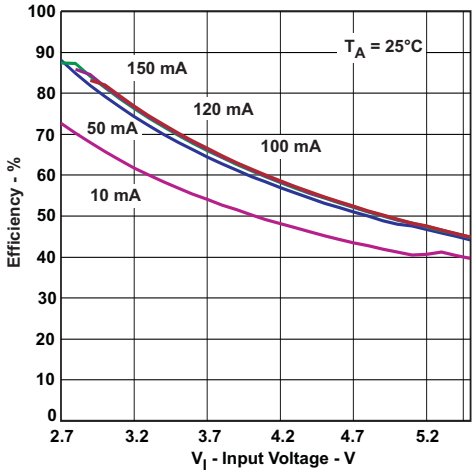
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS60150	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Efficiency vs Input Voltage



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2011) to Revision C **Page**

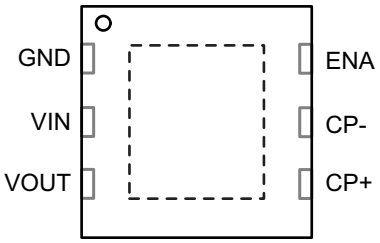
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (April 2009) to Revision B **Page**

- Added the Thermal Table and deleted the Dissipation Rating Table ... 4

5 Pin Configuration and Functions

DRV Package
6-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CP+	4	—	Connect to the flying capacitor
CP–	5	—	Connect to the flying capacitor
ENA	6	IN	Hardware enable/disable pin (High = Enable)
GND	1	—	Ground
VIN	2	IN	Supply voltage input
VOUT	3	OUT	Output, connect to the output capacitor

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{IN}	Input voltage (all pins)	–0.3	7	V
T_A	Operating temperature	–40	85	°C
T_J	Maximum operating junction temperature		150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model (HBM) is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The testing is done according JEDECs EIA/JESD22-A114.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		5.5	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C
C_{in}	Input capacitor	2.2			µF
C_o	Output capacitor	2.2			µF
C_f	Flying capacitor	1			µF

6.4 Thermal Information

THERMAL METRIC (1)		TPS60150 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	69.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{IN} = 3.6 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C, C1 = C3 = 2.2 µF, C2 = 1 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER STAGE						
V_{IN}	Input voltage range		2.7		5.5	V
V_{UVLO}	Undervoltage lockout threshold			1.9	2.1	V
I_Q	Operating quiescent current	I_{OUT} = 140 mA, Enable = V_{IN}		4.7		mA
I_{Qskip}	Skip mode operating quiescent current	I_{OUT} = 0 mA, Enable=V_{IN} (no switching)		80		µA
		I_{OUT} = 0 mA, Enable = V_{IN}(minimum switching)		90		µA
I_{SD}	Shut down current	2.7 V ≤ V_{IN} ≤ 5.5 V, Enable = 0 V			1	µA
V_{OUT}	Output voltage(1)	I_{OUT} ≤ 50 mA, 2.7 V ≤ V_{IN} < 5.5 V	4.8	5	5.2	V
$V_{OUT(skip)}$	Skip mode output voltage	I_{OUT} = 0 mA, 2.7 V ≤ V_{IN} ≤ 5.5 V		V_{OUT} + 0.1		V
F_{SW}	Switching frequency			1.5		MHz
SS_{TIME}	Soft-start time	From the rising edge of enable to 90% output		150		µs
OUTPUT CURRENT						
I_{OUT_nom}	Maximum output current	V_{OUT} remains from 4.8 V to 5.2 V, 3.1 V ≤ V_{IN} ≤ 5.5 V	120			mA
		3.3 V < V_{IN} < 5.5 V	140			
I_{OUT_short}	Short circuit current(2)	V_{OUT} = 0 V		80		mA
RIPPLE VOLTAGE						
V_R	Output ripple voltage	I_{OUT} = 140 mA		30		mV
ENABLE CONTROL						
V_{HI}	Logic high input voltage	2.7 V ≤ V_{IN} ≤ 5.5 V	1.3		V_{IN}	V
V_{LI}	Logic low input voltage		–0.2		0.4	V
I_{HI}	Logic high input current				1	µA
I_{LI}	Logic low input current				1	µA
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature			160		°C
T_{RC}	Shutdown recovery			140		°C

(1) When in skip mode, output voltage can exceed V_{OUT} spec because $V_{OUT(skip)}$ = V_{OUT}+0.1.
(2) The TPS60150 device has internal protection circuit to protect IC when V_{OUT} shorted to GND.

6.6 Typical Characteristics

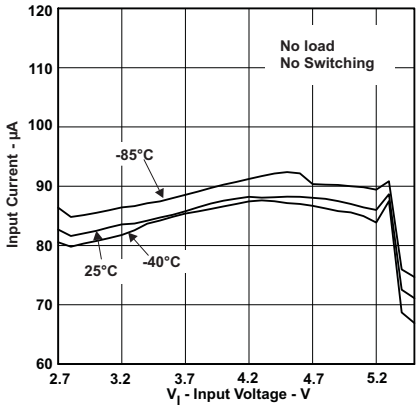


Figure 1. Quiescent Current vs Input Voltage

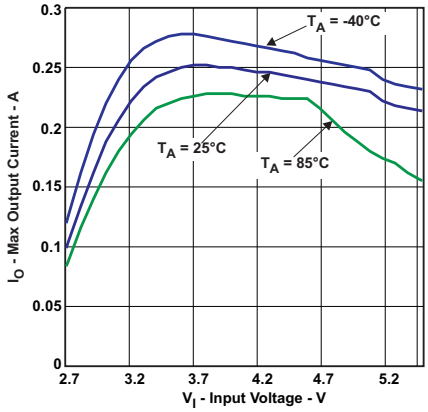


Figure 2. Maximum Output Current vs Input Voltage at Temperature

7 Detailed Description

7.1 Overview

The TPS60150 regulated charge pump provides a regulated output voltage for various input voltages. The TPS60150 device regulates the voltage across the flying capacitor to 2.5 V and controls the voltage drop of Q1 and Q2 while a conversion clock with 50% duty cycle drives the FETs.

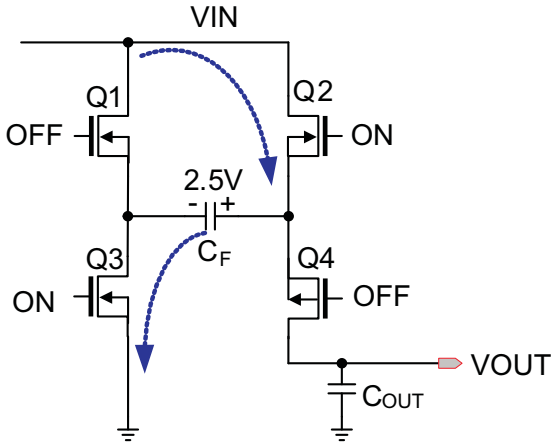


Figure 3. Charging Mode

During the first half cycle, Q2 and Q3 transistors are turned on and flying capacitor, C_F, will be charged to 2.5 V ideally.

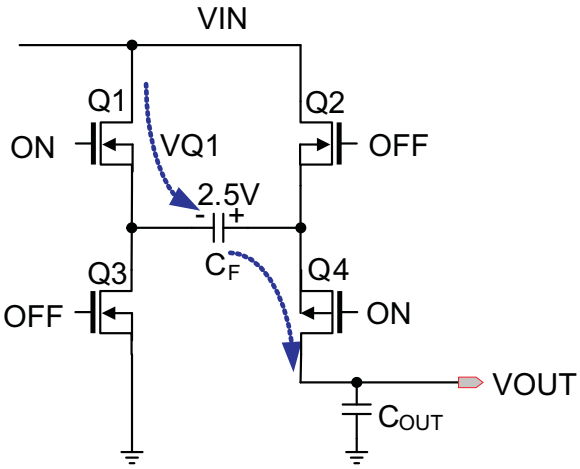


Figure 4. Discharging Mode

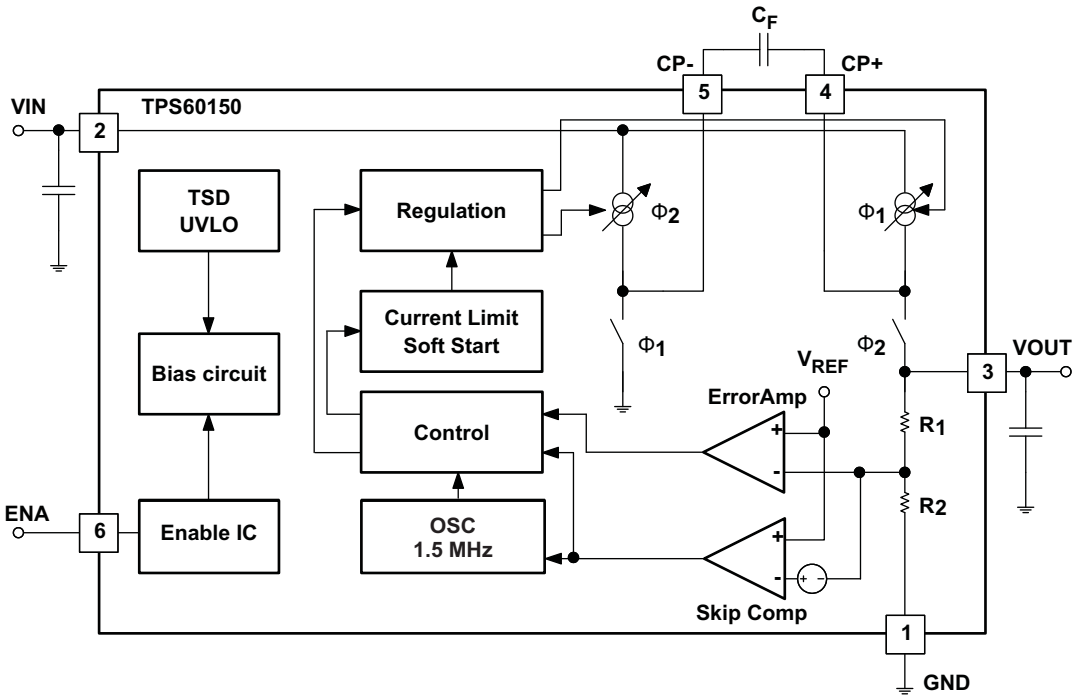
During the second half cycle, Q1 and Q4 transistors are turned on. Capacitor C_F will then be discharged to output.

Use Equation 1 to calculate the output voltage.

$$V_{OUT} = V_{IN} - VQ1 + V(C_F) - VQ4 = V_{IN} - VQ1 + 2.5\ V - VQ4 = 5\ V \quad \text{(Ideal)} \tag{1}$$

The output voltage is regulated by output feedback and an internally compensated voltage control loop.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable

An enable pin on the regulator is used to place the device into an energy-saving shutdown mode. In this mode, the output is disconnected from the input, and the input quiescent current is reduced to 10 µA maximum.

7.3.2 Undervoltage Lockout

When the input voltage drops, the undervoltage lockout prevents misoperation by switching off the device. The converter starts operation again when the input voltage exceeds the threshold, provided the enable pin is high.

7.3.3 Thermal Shutdown Protection

The regulator has thermal shutdown circuitry that protects it from damage caused by overload conditions. The thermal protection circuitry disables the output when the junction temperature reached approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is automatically reenabled. Continuously running the regulator into thermal shutdown can degrade reliability. The regulator also provides current limit to protect itself and the load.

7.4 Device Functional Modes

7.4.1 Soft Start

An internal soft start limits the inrush current when the device is being enabled.

7.4.2 Normal Mode and Skip Mode Operation

The TPS60150 device has skip mode operation as shown in Figure 5. The TPS60150 device enters skip mode if the output voltage reaches 5 V +0.1 V and the load current is less than 8 mA (typical). In skip mode, the TPS60150 device disables the oscillator and decreases the prebias current of the output stage to reduce the power consumption. Once the output voltage dips less than the threshold voltage of 5 V +0.1 V, the TPS60150 device begins switching to increase output voltage until the output reaches 5 V +0.1 V. When the output voltage dips less than 5 V, the TPS60150 device returns to normal pulse width modulation (PWM) mode; thereby reenabling the oscillator and increasing the prebias current of the output stage to supply output current.

The skip threshold voltage and current depend on input voltage and output current conditions.

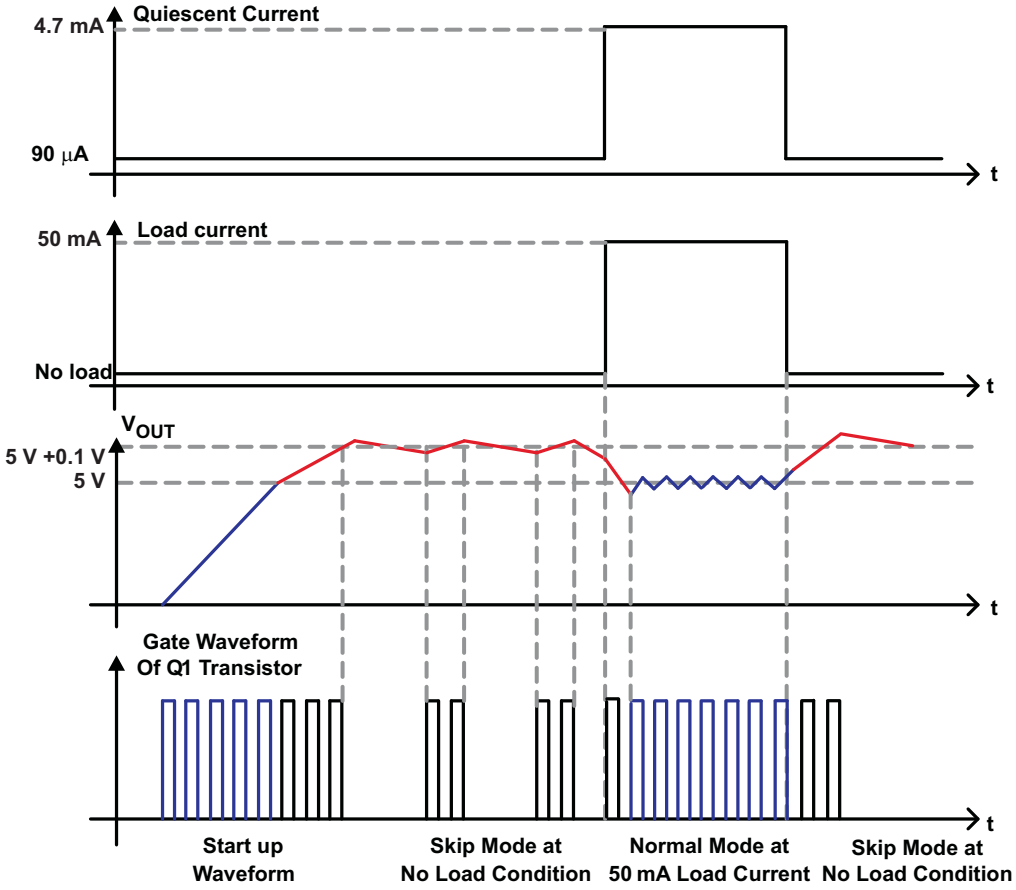


Figure 5. Normal Mode and Skip Mode Operation

7.4.3 Short Circuit Protection

The TPS60150 device has internal short circuit protection to protect the IC when the output is shorted to ground. To avoid damage when output is shorted to ground, the short circuit protection circuitry senses output voltage and clamps the maximum output current to 80 mA (typical).

Device Functional Modes (continued)

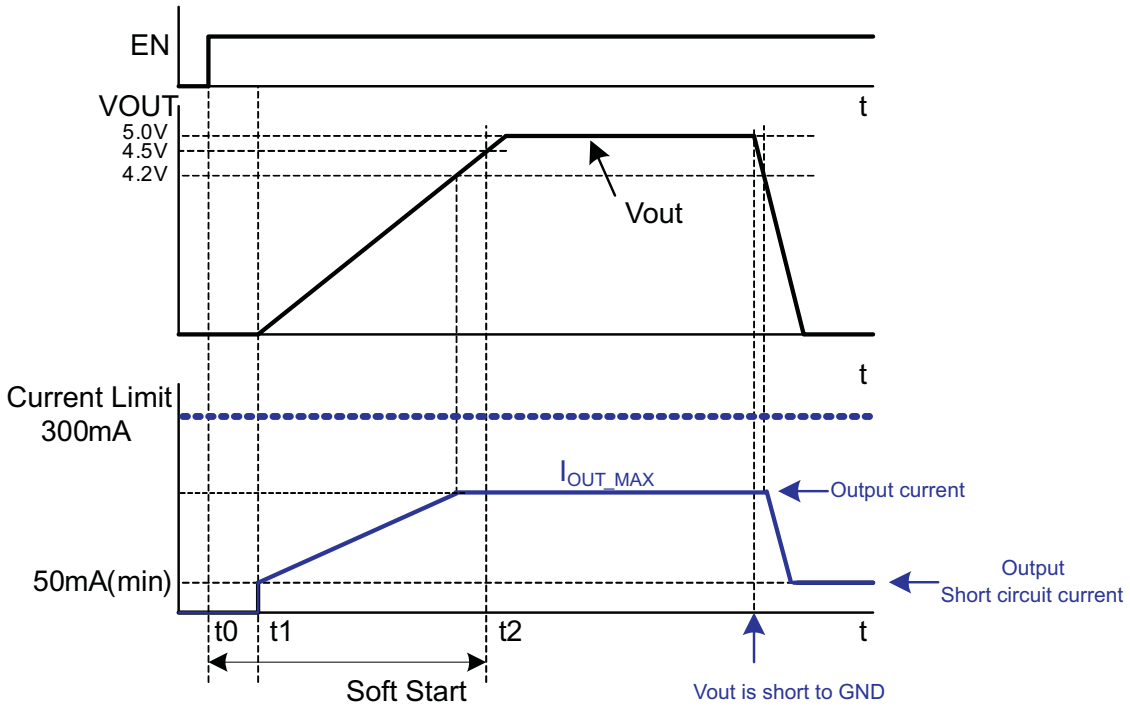


Figure 6. Maximum Output Current Capability and Short Circuit Protection

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Most of today's battery-powered portable electronics allow and/or require data transfer with a PC. One of the fastest data transfer protocols is through USB On-the-Go (OTG). As Figure 7 shows, the USB OTG circuitry in the portable device requires a 5-V power rail and up to 140 mA of current. The TPS60150 device may be used to provide a 5-V power rail in a battery powered system.

8.2 Typical Application

8.2.1 USB On the Go Circuitry

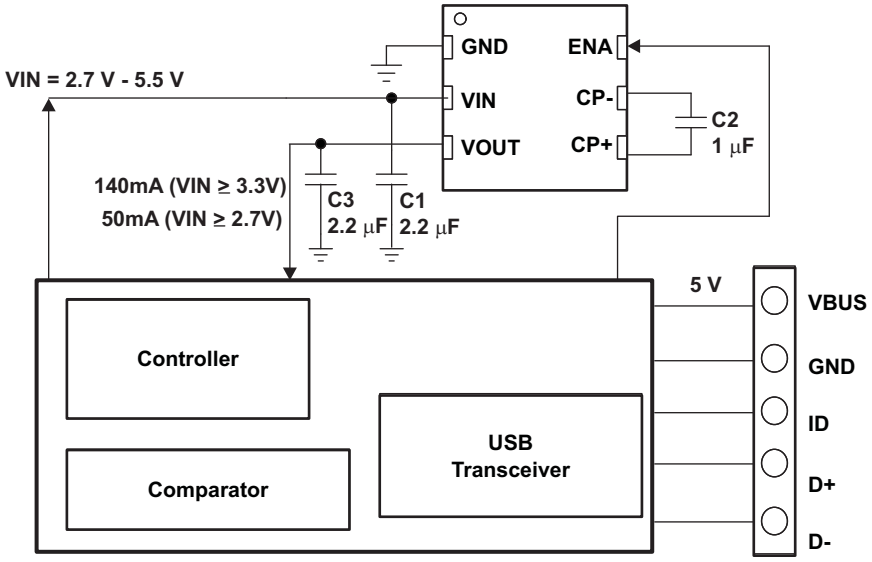


Figure 7. Application Circuit for OTG System

8.2.1.1 Design Requirements

The design guideline provides a component selection to operate the device within the *Recommended Operating Conditions*.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Capacitor Selection

For minimum output voltage ripple, the output capacitor (C_{OUT}) should be a surface-mount ceramic capacitor. Tantalum capacitors generally have a higher effective series resistance (ESR) and may contribute to higher output voltage ripple. Leaded capacitors also increase ripple due to the higher inductance of the package itself. To achieve the best operation with low input voltage and high load current, the input and flying capacitors (C_{IN} and C_F, respectively) should also be surface-mount ceramic types.

Typical Application (continued)

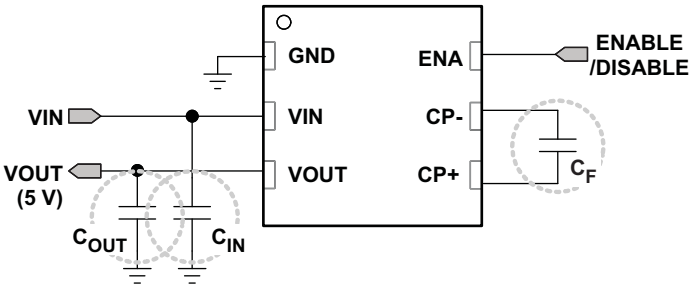


Figure 8. Capacitors

Generally, C_{FLY} can be calculated using Equation 2.

$$Q_{charging} = c \times v = C_{FLY} \times \Delta V_{CFLY},$$

$$Q_{discharging} = i_{discharge} \times t = 2 \times I_{LOAD(MAX)} \times \left(\frac{T}{2}\right), \text{ half duty.} \tag{2}$$

$$\therefore 2 \times I_{LOAD(MAX)} \times \left(\frac{T}{2}\right) = C_{FLY} \times \Delta V_{CFLY}$$

Both equation should be same,

$$\therefore C_{FLY} \geq \frac{2 \times I_{LOAD(MAX)} \times \left(\frac{T}{2}\right)}{\Delta V_{CFLY}} = \frac{I_{LOAD(MAX)}}{\Delta V_{CFLY} \times f} \tag{3}$$

If I_{LOAD} = 140 mA, f = 1.5 MHZ, and ΔV_{CFLY} = 100 mV, the minimum value of the flying capacitor should be 1 µF.

Output capacitance, C_{OUT}, is also strongly related to output ripple voltage and loop stability,

$$V_{OUT(RIPPLE)} = \frac{I_{LOAD(MAX)}}{(2 \times f \times C_{OUT})} + 2 I_{LOAD(MAX)} \times ESR_{COUT} \tag{4}$$

The minimum output capacitance for all output levels is 2.2 µF due to control stability. Larger ceramic capacitors or low ESR capacitors can be used to lower the output ripple voltage.

Table 1. Suggested Capacitors (Input, Output, and Flying Capacitor)

VALUE	DIELECTRIC MATERIAL	PACKAGE SIZE	RATED VOLTAGE
4.7 µF	X5R or X7R	0603	10 V
2.2 µF	X5R or X7R	0603	10 V

The efficiency of the charge pump regulator varies with the output voltage, the applied input voltage and the load current.

Use Equation 5 and Equation 6 to calculate the approximate efficiency in normal operating mode is given by:

$$\text{Efficiency}(\%) = \frac{PD(out)}{PD(in)} \times 100 = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100, \; I_{IN} = 2 \times I_{OUT} + I_Q \tag{5}$$

$$\text{Efficiency}(\%) = \frac{V_{OUT}}{2 \times V_{IN}} \times 100 \; (I_{IN} = 2 \times I_{OUT}) \quad \text{Quiescent current was neglected.} \tag{6}$$

8.2.1.3 Application Curves

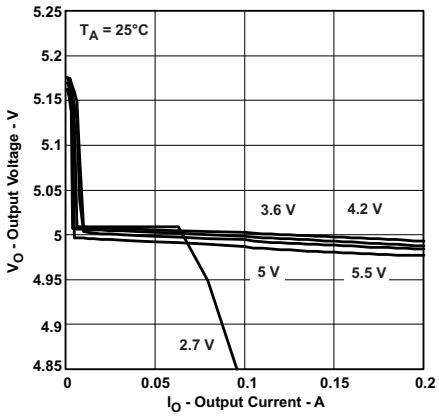


Figure 9. Output Voltage vs Output Current

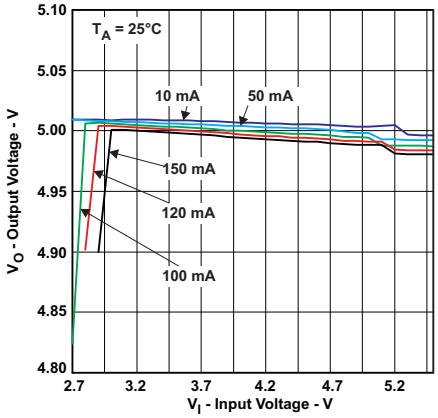


Figure 10. Output Voltage vs Input Voltage

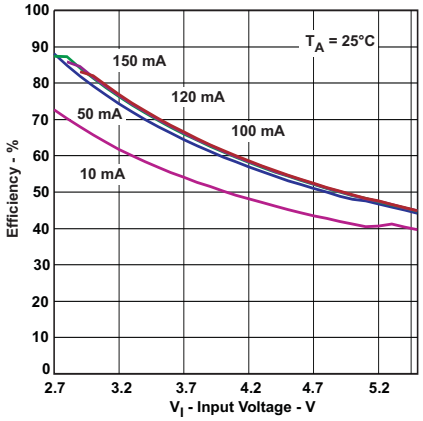
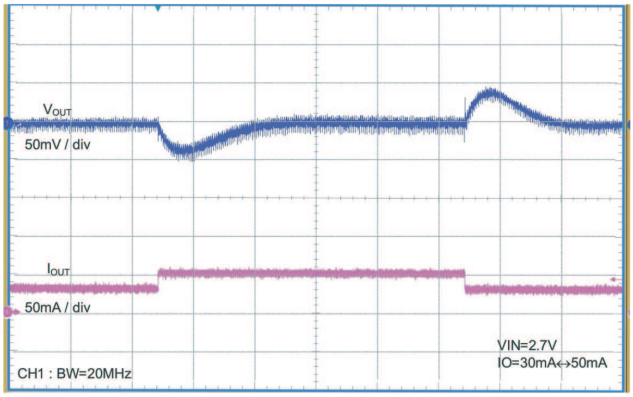
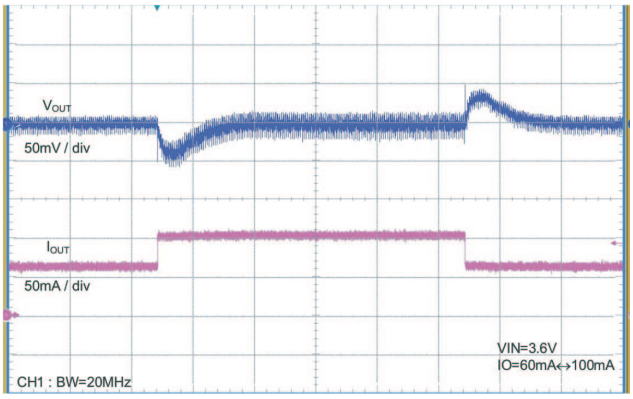


Figure 11. Efficiency vs Input Voltage



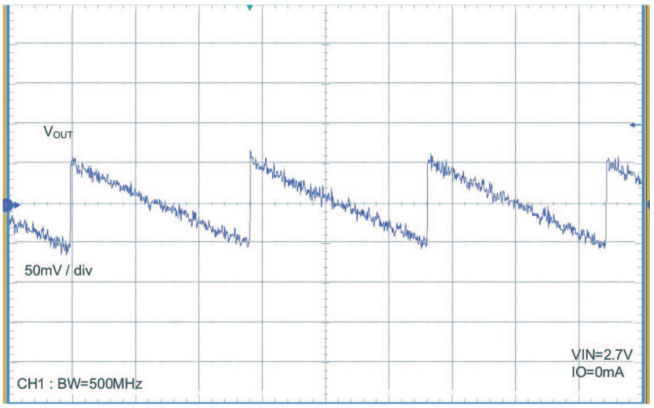
20 µs/div

Figure 12. Load Transient Response
V_{IN} = 2.7 V, IO = 30 mA to 50 mA



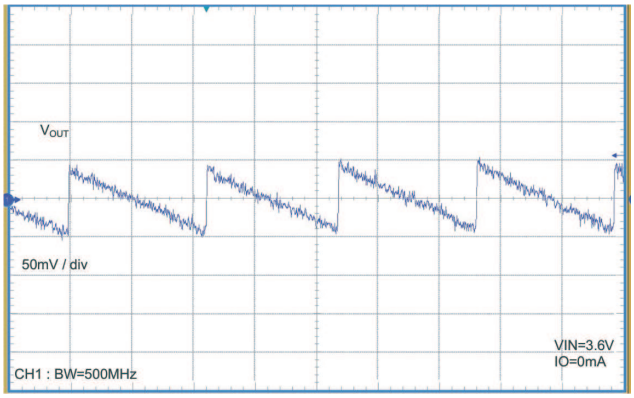
20 µs/div

Figure 13. Load Transient Response
V_{IN} = 3.6 V, IO = 60 mA to 100 mA



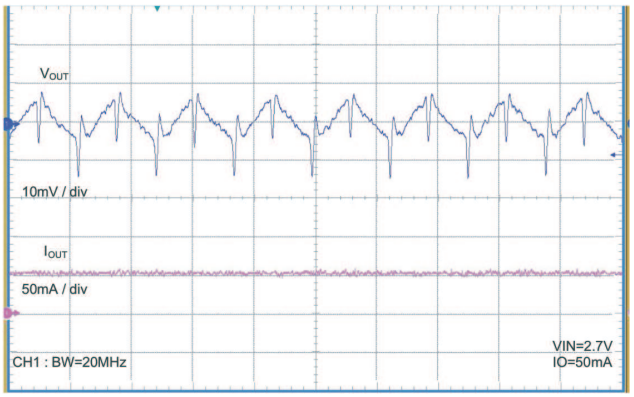
5 ms/div

Figure 14. Output Ripple Voltage (Skip Mode)
V_{IN} = 2.7 V, IO = 0 mA



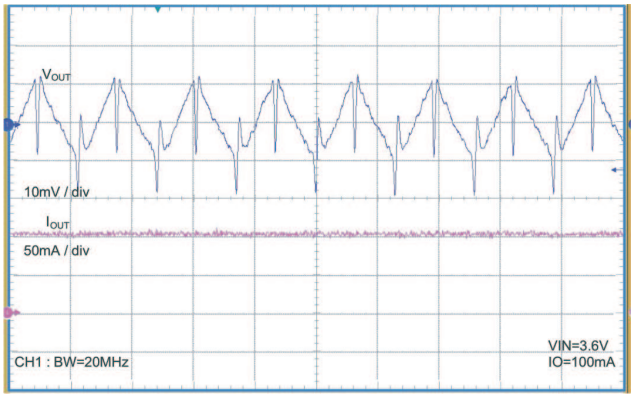
5 ms/div

Figure 15. Output Ripple Voltage (Skip Mode)
V_{IN} = 3.6 V, IO = 0 mA



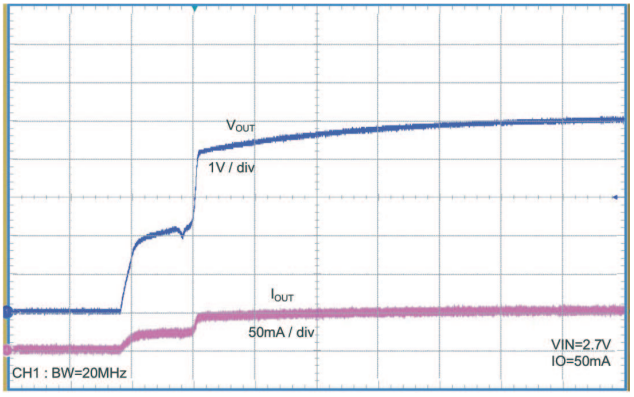
500 ns/div

Figure 16. Output Ripple Voltage (Normal Mode)
V_{IN} = 2.7 V, IO = 50 mA



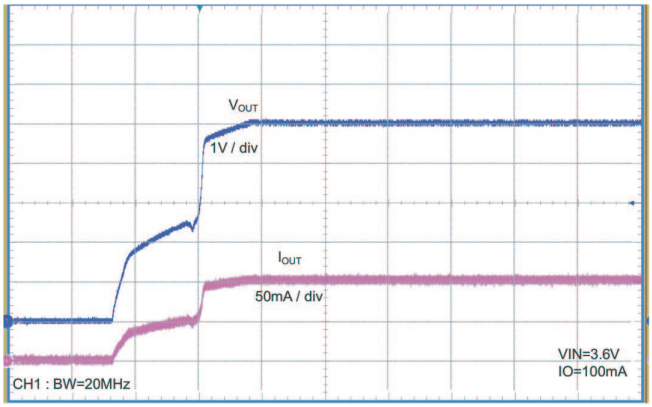
500 ns/div

Figure 17. Output Ripple (Normal Mode)
V_{IN} = 3.6 V, IO = 100 mA



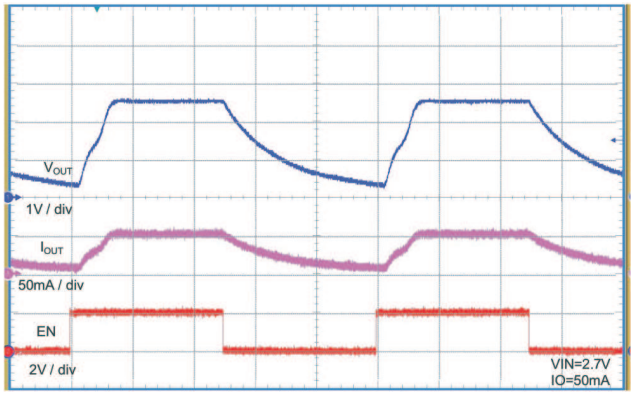
1 ms/div

Figure 18. Power On
V_{IN} = 2.7 V, IO = 50 mA



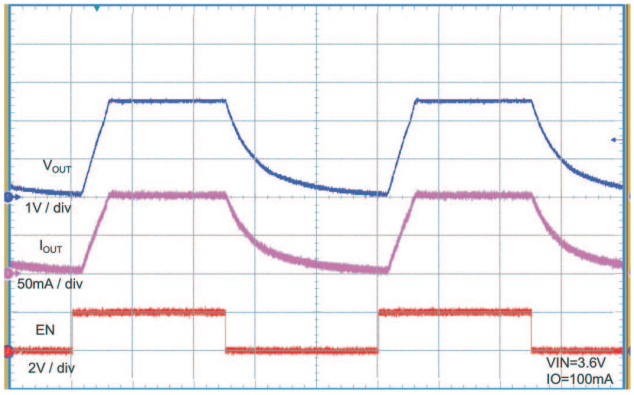
1 ms/div

Figure 19. Power On
V_{IN} = 3.6 V, IO = 100 mA



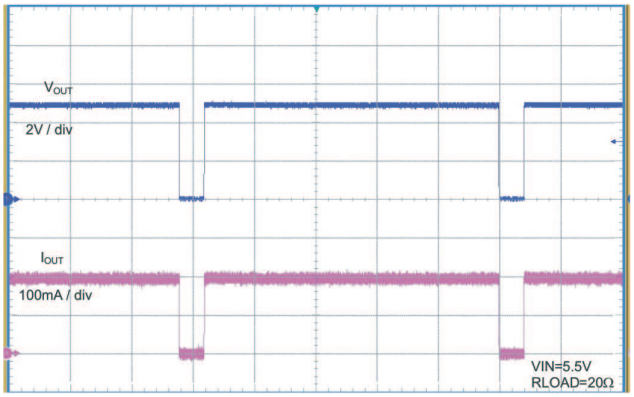
200 µs/div

Figure 20. Enable / Disable
V_{IN} = 2.7 V, IO = 50 mA



200 µs/div

Figure 21. Enable / Disable
V_{IN} = 3.6 V, IO = 100 mA



50 ms/div

Figure 22. Thermal Shutdown Operation
V_{IN} = 5.5 V, R_{LOAD}= 20 Ω

8.2.2 System Example

Low-cost portable electronics with small LCD displays require a low-cost solution for providing the WLED backlight. As shown in Figure 23, the TPS60150 device can also be used to drive several WLEDs in parallel, with the help of ballast resistors.

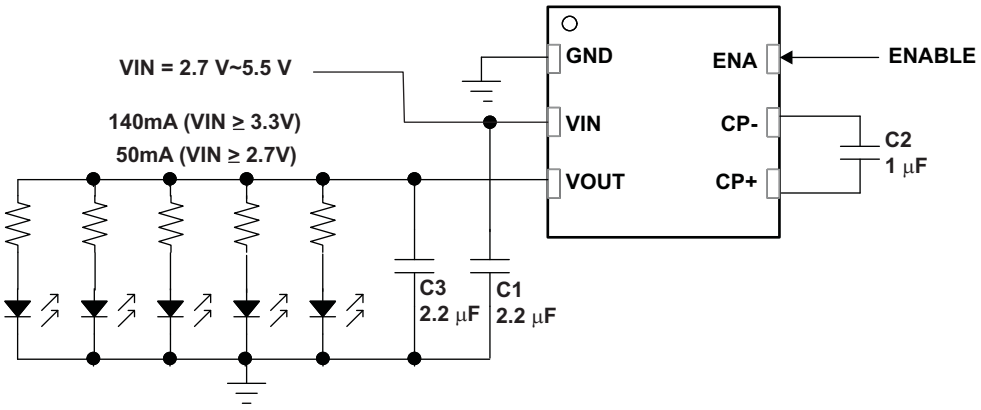


Figure 23. Application Circuit for Driving White LEDs

9 Power Supply Recommendations

The TPS60150 device has no special requirements for its input power supply. The input power supply's output current must be rated according to the supply voltage, output voltage and output current of the TPS60150 device.

10 Layout

10.1 Layout Guidelines

Large transient currents flow in the VIN, VOUT, and GND traces. To minimize both input and output ripple, keep the capacitors as close as possible to the regulator using short, direct circuit traces.

10.2 Layout Example

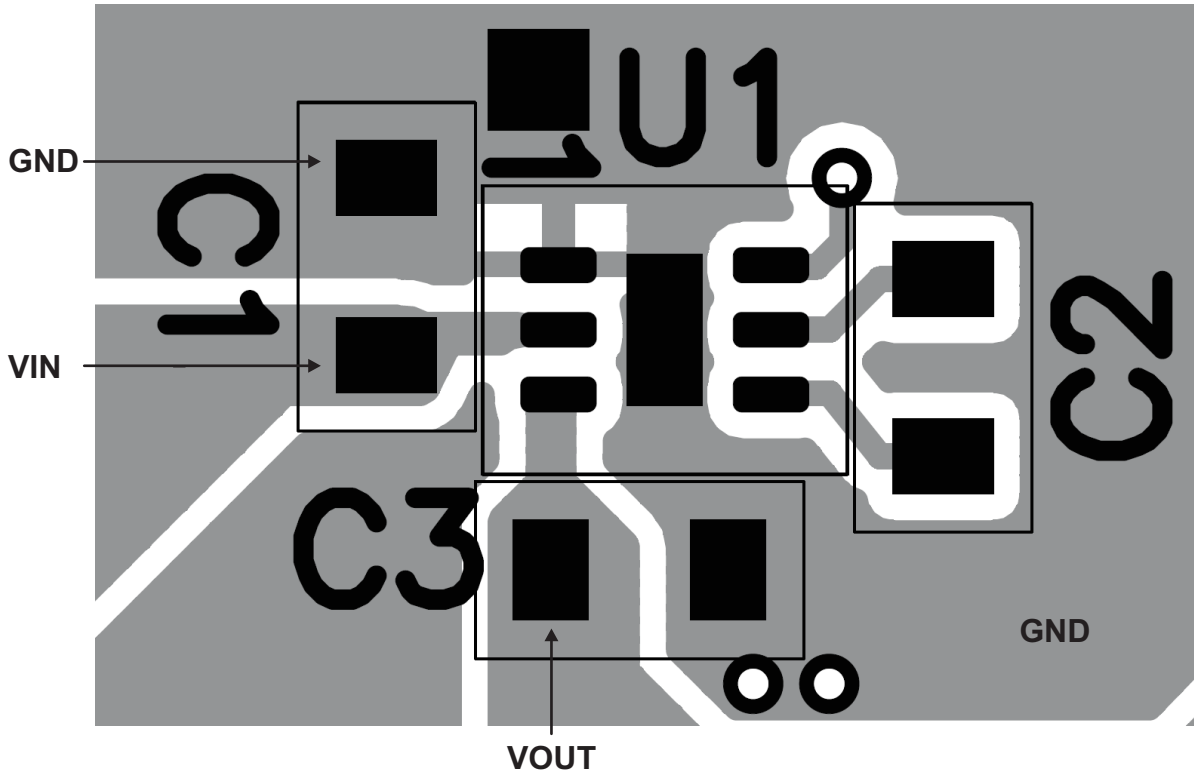


Figure 24. Recommended PCB Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60150DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CGO	Samples
TPS60150DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CGO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

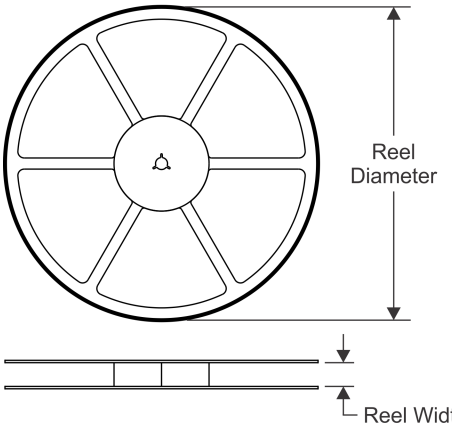
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

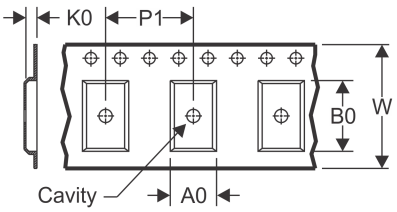
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

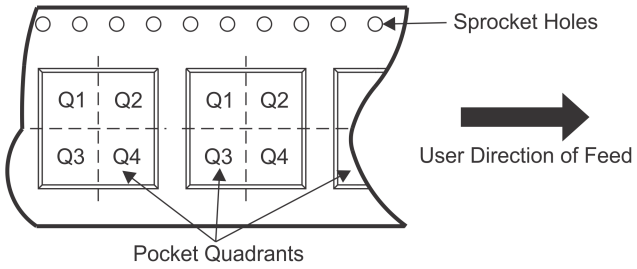


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

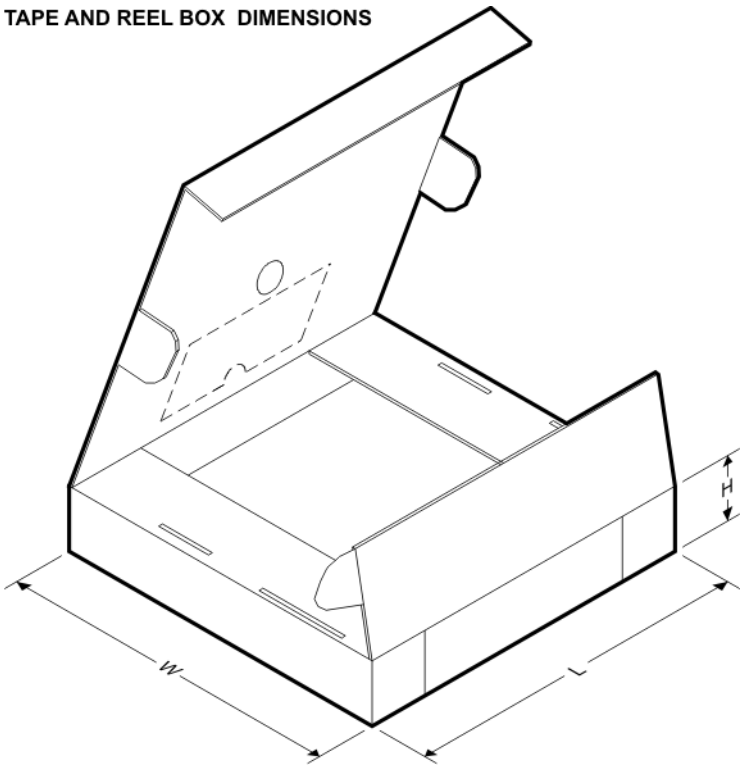
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60150DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS60150DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS60150DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS60150DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

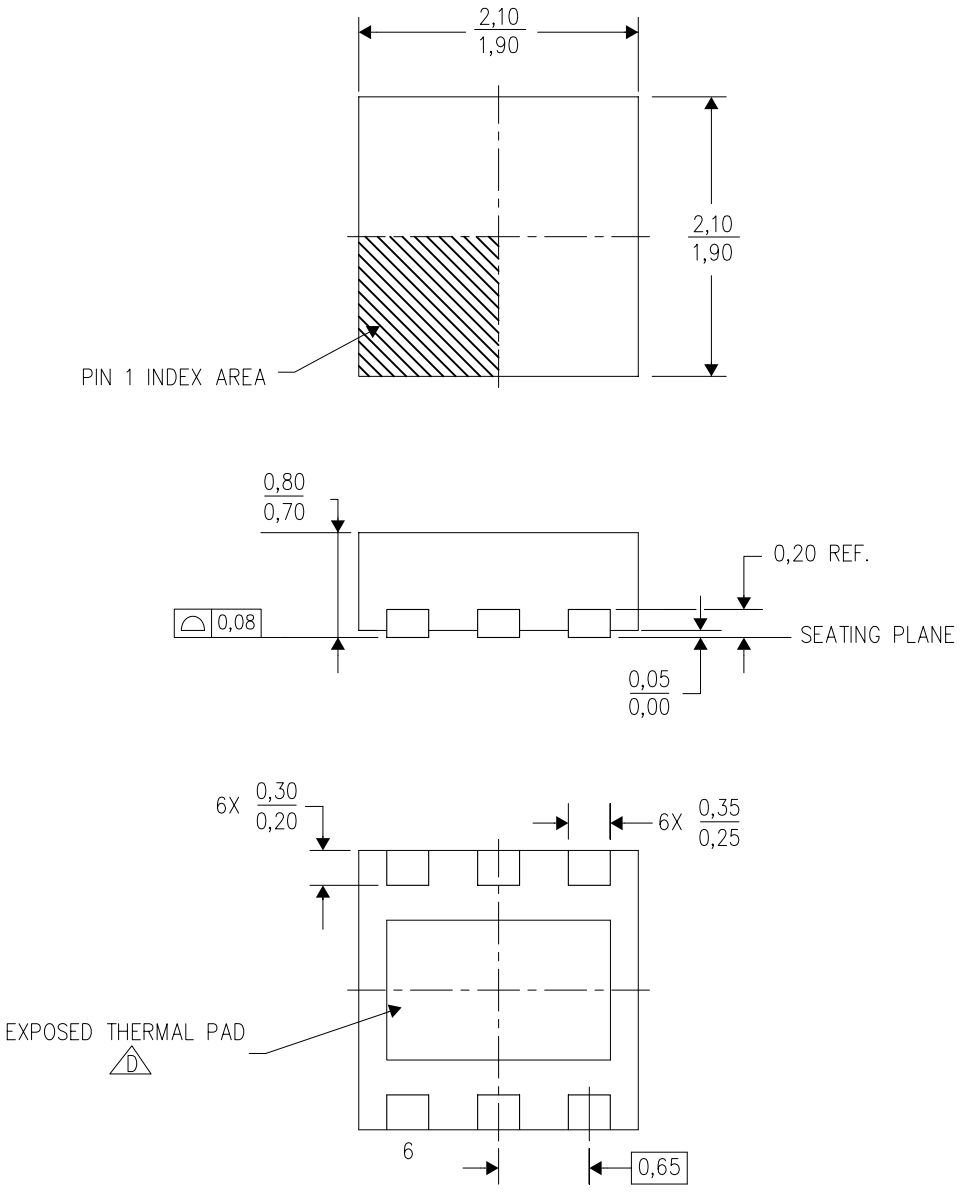
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60150DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS60150DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS60150DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS60150DRVT	WSON	DRV	6	250	210.0	185.0	35.0

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

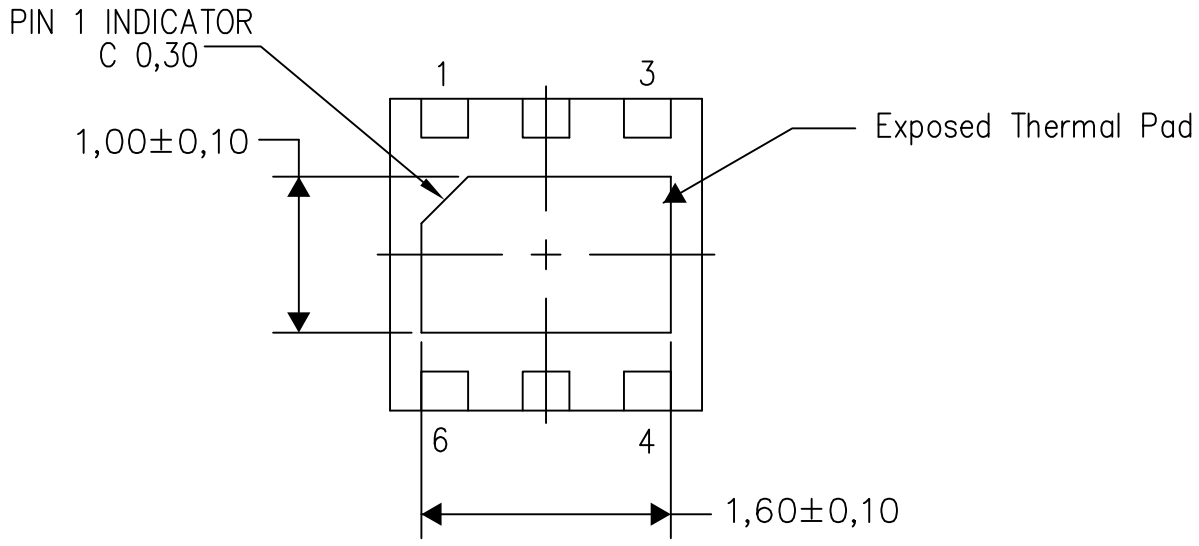
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



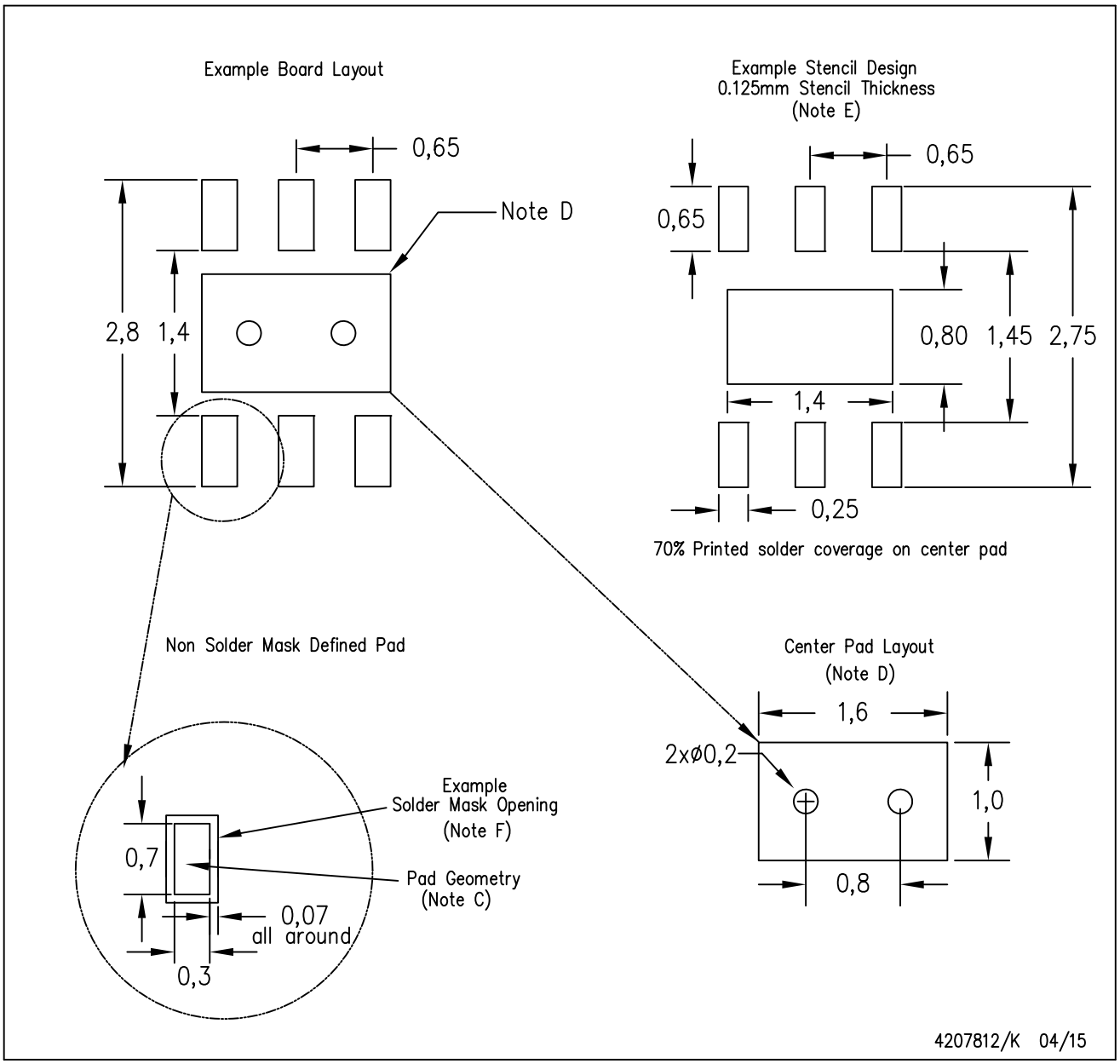
Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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