AK7757

Audio DSP with 24bit 3ch ADC + 4ch DAC + MIC Amp

GENERAL DESCRIPTION

The AK7757 is a digital signal processor with an integrated 4ch DAC, a stereo ADC with input selector, a mono ADC and an integrated digital audio interface. The audio DSP has 1536 step/fs (at 48kHz sampling) parallel arithmetic operation performance. As the AK7757 is a RAM based DSP, it is programmable for user requirements to realize the audio effects process or the proprietary high-performance HF. It is housed in a 48pin LQFP which is a small package to save the PCB space.

FEATURES

- ☐ **DSP**
  - **Word length: 24bits (Data RAM: F24 floating point)**
  - **Processing Speed: 13.6 ns (9216step/fs; fs = 8kHz)**
  - **Multiplication: 20 x 20 → 36-bit Double precision arithmetic available**
  - **Divider 20 / 20 → 20-bit**
  - **ALU: 40-bit arithmetic operation (overflow margin 4bits) 24-bit floating point arithmetic and logic operation**
  - **Program RAM: 4096 x 36bits**
  - **Coefficient RAM: 4096 x 20bits**
  - **Data RAM: 2048 x 24bits (F24 floating point)**
  - **Delay RAM: 4096 x 20bits, 4096 x 20bits**
  - **Master Clock: 73.7MHz**
  - **JX pins (interrupt)**
- ☐ **2ch ADC1**
  - **Sampling Frequency: 8kHz~48kHz**
  - **3in / 1out Input Selector (Diffrentialx1 single endx1 single end with MicAmpx1)**
  - **ADC S/N: 96dBA, S/ (N+D): 88dB**
- ☐ **1ch ADC2**
  - **Sampling Frequency: 8kHz~48kHz**
  - **ADC S/N: 89dBA, S/(N+D): 82dB**
- ☐ **4ch DAC**
  - **Sampling Frequency: 8kHz~48kHz**
  - **DAC S/N: 107dBA, S/ (N+D): 92dB**
- ☐ **Microphone Interface**
  - **Differential or single-end input**
  - **Programmable Gain (+33dB ~ +15dB and 0dB, 3dB step)**
  - **Low Noise Microphone Bias**
- ☐ **Automatic Power Down (CODEC, DSP)**
- ☐ **µP I/F: SPI, I^2C**
- ☐ **Power supply**
  - **Analog (AVDD): 3.0V ~ 3.6V (typ.3.3V)**
  - **Digital1 (DVDD): 3.0V ~ 3.6V (typ.3.3V)**
  - **Digital2 (DVDD18): 1.7V ~ 1.9V (typ.1.8V)**
- ☐ **Operating temperature range: -40°C ~ 85°C**
- ☐ **Package: 48pin LQFP**

■ Block Diagram

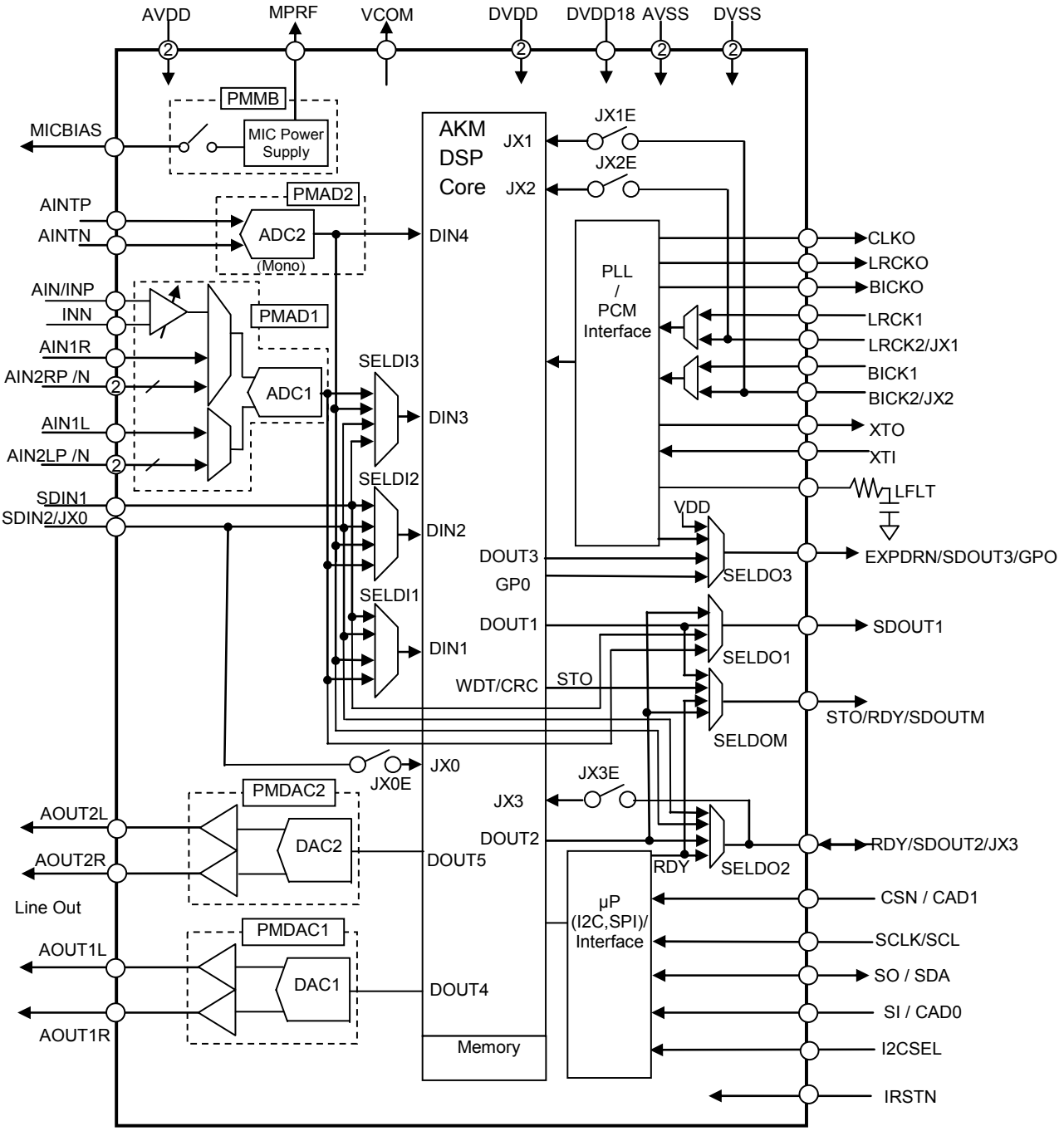

Figure 1. Block Diagram

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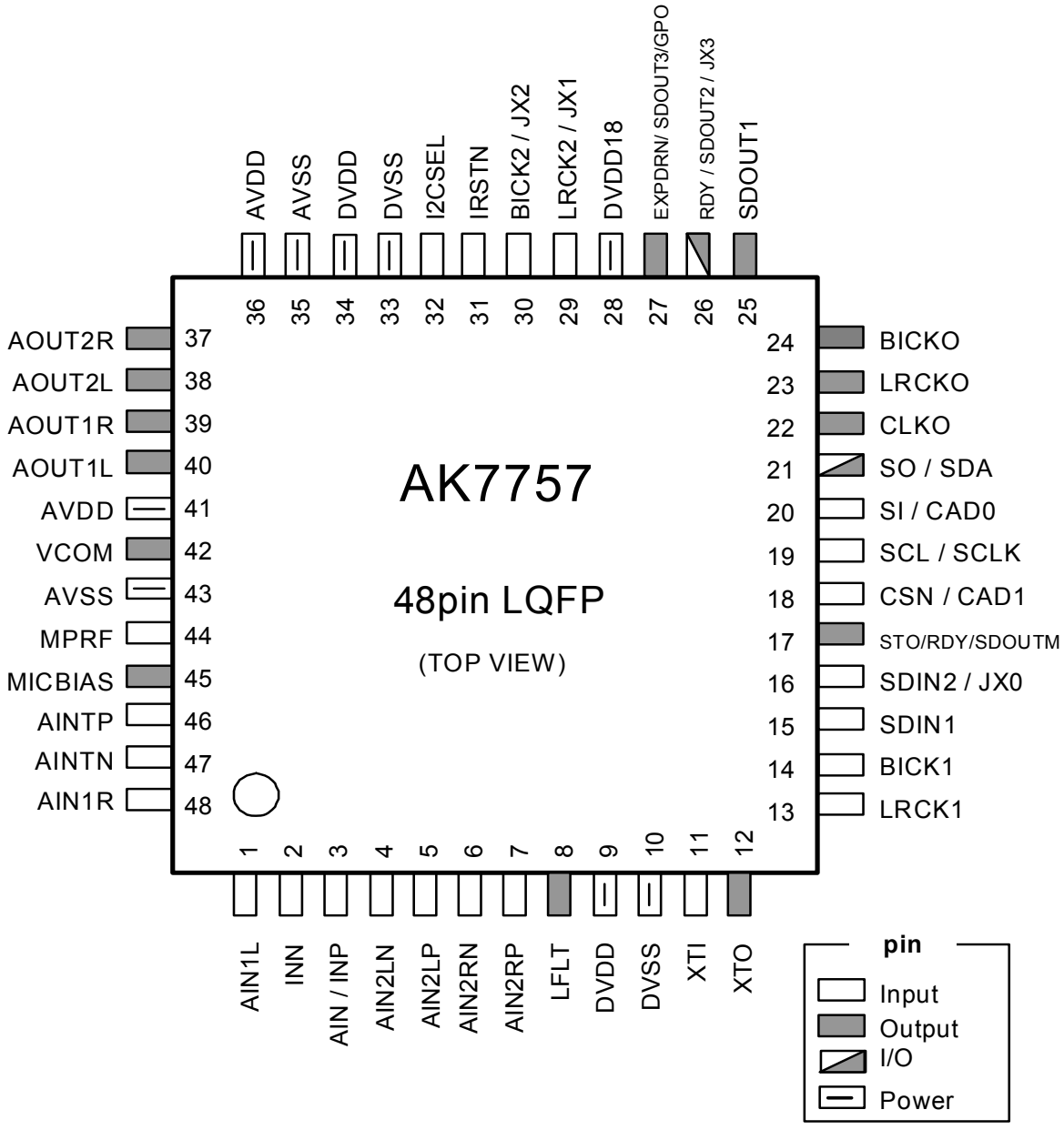
■ Ordering Guide

AK7757VQ	-40 ~ +85°C	48pin LQFP
AKD7757	Evaluation Board for AK7757	

■ Pin Layout



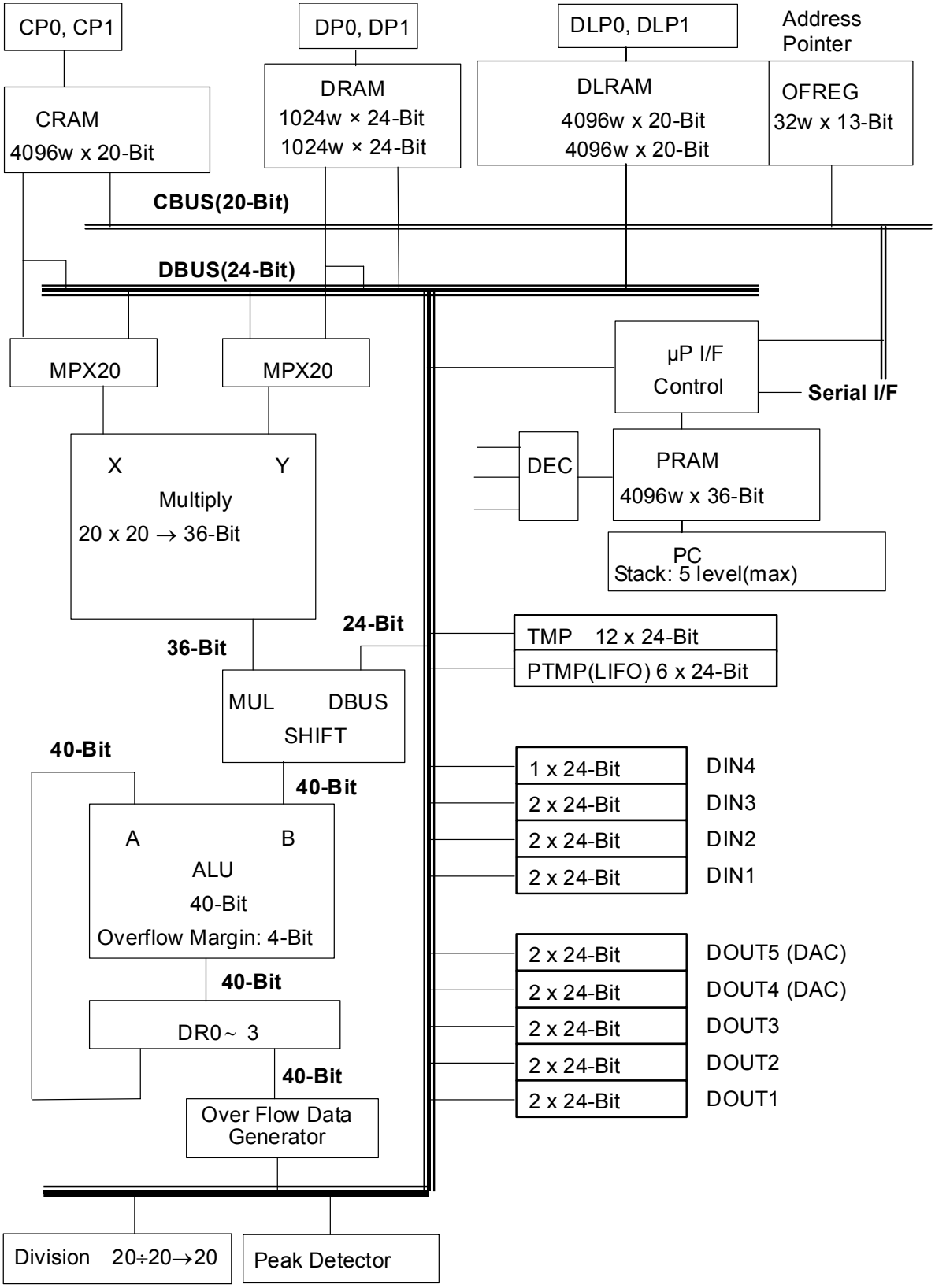


Figure 2. Main DSP Block Diagram of the AK7757

PIN FUNCTION

No.	Pin Name	I/O	Function
1	AIN1L	I	ADC1 Lch Single-ended Input 1 Pin.
2	INN	I	Microphone Inverted Differential Input Pin
3	AIN	I	Microphne Single-ended Input Pin
	INP	I	Microphone Non-inverted Differential Input Pin
4	AIN2LN	I	ADC1 Lch Inverted Differential Input 2 Pin
5	AIN2LP	I	ADC1 Lch Non-inverted Differential Input 2 Pin
6	AIN2RN	I	ADC1 Rch Inverted Differential Input 2 Pin
7	AIN2RP	I	ADC1 Rch Non-inverted Differential Input 2 Pin
8	LFLT	O	R and C Components Connect Pin for PLL Refer to "7. LFLT Pin External Connection". This pin outputs "L" during initial reset.
9	DVDD	-	Digital Power Supply Pin 3.0~3.6V
10	DVSS	-	Ground Pin 0V
11	XTI	I	Crystal Oscillator Input Pin Connect a crystal oscillator between this pin and the XTO pin, or input an external clock to the XTI pin.
12	XTO	O	Crystal Oscillator Output Pin When a crystal oscillator is used, connect it between XTI and XTO. When an external clock is used, leave this pin open. During initial reset, the output of this pin is not determinable.
13	LRCK1	I	LR Channel Select Clock Pin 1 LR clock should be input to this pin in slave mode.
14	BICK1	I	Serial Bit Clock Input Pin 1 BITCLOCK (48fs or 64fs) should be input to this pin in slave mode.
15	SDIN1	I	Serial Data Input 1 Pin
16	SDIN2	I	Serial Data Input 2 Pin
	JX0	I	Conditional Jump Pin0 The conditional jump pin (JX0) is valid by setting control register (JX0E) to "1".
17	STO	O	Status Output Pin This pin outputs "H" during initial reset.
	RDY	O	Data Write Ready Output Pin for Microprocessor Interface This pin outputs RDY.
	SDOUTM	O	Serial Data Output Pin for Internal Monitoring
18	CSN	I	µP I/F Chip Select N Pin (I2CSEL pin = "L") When initial reset and µP I/F are not in use, leave the CSN pin High level.
	CAD1	I	I^2C-bus Address 1 Pin (I2CSEL pin = "H")
19	SCLK	I	µP I/F Serial Data Clock Pin (I2CSEL pin = "L") Set this pin to "H" when there are no clock inputs.
	SCL	I	I^2C I/F Data Clock Pin (I2CSEL pin= "H")

20	SI	I	µP I/F Serial Data Input Pin (I2CSEL pin = "L") Set this pin to "L" when not used.
	CAD0	I	I^2C-bus Address 0 Pin (I2CSEL pin = "H")
21	SO	O	µP I/F Serial Data Output Pin This pin outputs "Hi-Z" during initial reset.
	SDA	I/O	I^2C-bus I/F Serial Data In/Output Pin (I2CSEL pin= "H") This pin outputs Hi-Z during initial reset.
22	CLKO	O	Clock Output Pin This pin outputs "L" during initial reset.
23	LRCKO	O	LR Channel Select Output Pin This pin outputs "L" during initial reset in master mode.
24	BICKO	O	Serial Bit Clock Output Pin This pin outputs "L" during initial reset in master mode.
25	SDOUT1	O	Serial Data Output1 Pin This pin outputs "L" during initial reset.
26	RDY	O	Data Write Ready Output Pin for Microprocessor Interface Set DOUT2IOE bit= "1" and JX3E bit = "0" when this pin is used as an output pin. A pull-down resistor should be connected.
	SDOUT2	O	Serial Data Output2 Pin Set DOUT2IOE bit= "1" and JX3E bit = "0" when this pin is used as an output pin. A pull-down resistor should be connected.
	JX3	I	Conditional Jump Pin3 The conditional jump pin (JX3) is valid by setting control register (JX3E) to "1".
27	EXPDRN	O	Power Down Signal Output Pin
	SDOUT3	O	Serial Data Output3 Pin This pin outputs "L" during initial reset.
	GPO	O	General Purpose Output Pin for External Device Controlling
28	DVDD18	-	Digital Power Supply Pin 1.7~1.9V
29	LRCK2	I	LR Channel Select Clock Pin 2 LR clock should be input to this pin in slave mode.
	JX1	I	Conditional Jump Pin 1 The conditional jump pin (JX1) is valid by setting control register (JX1E) to "1".
30	BICK2	I	Serial Bit Clock Input Pin 2 BITCLOCK should be input to this pin in slave mode.
	JX2	I	Conditional Jump Pin 2 The conditional jump pin (JX2) is valid by setting control register (JX2E) to "1".
31	IRSTN	I	Initial Reset N Pin Use to initialize the AK7757. Set this pin to "L" when power-up the AK7757.
32	I2CSEL	I	I^2C BUS Select Pin I2CSEL pin = "L": 4-wired Interface I2CSEL pin = "H": I^2CBus selected mode. SCL and SDA are active. I2CSEL should be connected to "L" (DVSS) or "H" (DVDD).
33	DVSS	-	Ground Pin 0V
34	DVDD	-	Digital Power Supply Pin 3.0~3.6V
35	AVSS	-	Ground Pin 0V
36	AVDD	-	Analog Power Supply Pin 3.0~3.6V
37	AOUT2R	O	DAC2 Rch Analog Output Pin This pin outputs "Hi-Z" during initial reset.
38	AOUT2L	O	DAC2 Lch Analog Output Pin This pin outputs "Hi-Z" during initial reset.
39	AOUT1R	O	DAC1 Rch Analog Output Pin This pin outputs "Hi-Z" during initial reset.
40	AOUT1L	O	DAC1 Lch Analog Output Pin This pin outputs "Hi-Z" during initial reset.

41	AVDD	-	Analog Power Supply Pin 3.0~3.6V
42	VCOM	O	Analog Common Voltage Output pin Connect 0.1μF and 2.2μF capacitors between this pin and the AVSS pin. No external circuits should be connected to this pin. This pin outputs "L" during initial reset.
43	AVSS	-	Ground Pin 0V
44	MPRF	I	Output Pin for Ripple Filter of MICBIAS Circuit Connect a 1.0μF capacitor between this pin and AVSS. This pin outputs "H" during initial reset.
45	MICBIAS	O	Power Supply Pin for Microphone This pin outputs "Hi-Z" during initial reset.
46	AINTP	I	ADC2 Non-inverted Differential Input Pin
47	AINTN	I	ADC2 Inverted Differential Input Pin
48	AIN1R	I	ADC1 Rch Single-ended Input 1 Pin

Note 1. All digital input pins must not be left floating.
Note 2. DVDD or DVSS voltage must be input to the I2CSEL pin.
Note 3. All analog input pins (INP/AIN, INN pins) must be supplied signal via AC-coupling capacitor.
Note 4. Analog output pins (AOUT1/2 pins) must deliver signal via AC-coupling capacitor

■ Handling of Unused Pin

Unused I/O pins must be connected appropriately

Classification	Pin Name	Setting
Analog	MICBIAS, AINTP/N, AIN/INP, INN, AIN2LP/N, AIN1L/R, AIN2RP/N, AOUT1L/R, AOUT2L/R, MPRF	Open
Digital	XTO, SDOUT1, STO/RDY/SDOUTM, EXPDRN/SDOUT3/GPO, CLKO, LRCKO, BICKO	Open
	LRCK1, BICK1, LRCK2/JX1, BICK2/JX2, SDIN1, XTI, JX0/SDIN2, RDY/SDOUT2/JX3 (When Input Setting)	Connect to DVSS

ABSOLUTE MAXIMUM RATINGS

(AVSS=DVSS=0V: Note 5)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	–0.3	4.3	V
	Digital 1	DVDD	–0.3	4.3	V
	Digital 2	DVDD18	–0.3	2.5	V
	Difference(AVSS, DVSS)	ΔGND	-0.3	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 6)		VINA	–0.3	(AVDD+0.3) or 4.3	V
Digital Input Voltage (Note 7)		VIND1	–0.3	(DVDD+0.3) or 4.3	V
Ambient Temperature (powered applied)		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 5. All voltages are with respect to ground. AVSS and DVSS must be in the same voltage.
Note 6. AINTP/N, AIN/INP, INN, AIN2LP/N, AIN1L/R, AIN2RP/N pins
Note 7. IRSTN, I2CSEL, SI/CAD0, SCL/SCLK, CSN/CAD1, BICK1, LRCK1, BICK2/JX2, LRCK2/JX1, SDIN1, SDIN2/JX0, and RDY/SDOUT2/JX3 pins
Note 8. Pull-up resistors at SDA and SCL pins must be connected to the DVDD voltage or less. Do not turn off the power supplies when the SDA and SCL pins are pulled-up to DVDD.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS=DVSS =0V: Note 5)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 9)	Analog	AVDD	3.0	3.3	3.6	V
	Digital	DVDD	3.0	3.3	3.6	V
	Digital	DVDD18	1.7	1.8	1.9	V
	Difference1	AVDD – DVDD	-0.3	0	+0.3	V

Note 5. All voltages are with respect to ground. AVSS and DVSS must be in the same voltage.
Note 9. The power supply sequence for AVDD, DVDD and DVDD18 is not critical but all power supplies must be On before start operating the AK7757.

WARNING: Do not turn off the power supply of the AK7757 with the power supply of the surrounding device turned on. Pull-up of SDA and SCL pins must not exceed DVDD. (A diode exists for DVDD in the SDA and SCL pins.)
AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

ANALOG CHARACTERISTICS (CODEC)

■ ADC Characteristics

1. Microphone Amplifier

(Ta= 25ºC; AVDD=DVDD=3.3V; DVDD18=1.8V; AVSS=DVSS=0V)

	Parameter		min	typ	max	Unit
MIC AMP	Input impedance		22.5	30		kΩ
	Gain	MGAIN[2:0]bits=0h		0		dB
		MGAIN[2:0]bits=1h		15		dB
		MGAIN[2:0]bits=2h		18		dB
		MGAIN[2:0]bits=3h		21		dB
		MGAIN[2:0]bits=4h		24		dB
		MGAIN[2:0]bits=5h		27		dB
		MGAIN[2:0]bits=6h		30		dB
		MGAIN[2:0]bits=7h		33		dB

2. Microphone Bias

(Ta= 25ºC; AVDD=DVDD=3.3V; DVDD18=1.8V; AVSS=DVSS=0V)

	Parameter		min	typ	max	Unit
MIC BIAS	Output Voltage	Load Current 0mA		2.46		V
		Load Current 1mA		2.32		V
	Load Resistance		2			kΩ
	Load Capacitance				30	pF

Note 10. The output voltage is proportional to AVDD.

3. ADC1

(Ta=25ºC; AVDD=DVDD=3.3V, DVDD18=1.8V, VSS=0V, BICK=64fs; Signal frequency 1kHz; Measurement frequency = 20Hz~20kHz @fs=48kHz; with Differential Input; Unless otherwise specified.)

Parameter			min	typ	max	Unit
ADC Section	Resolution				24	Bits
	Dynamic Characteristics					
	S/(N+D) (-1dBFS)	MGAIN[2:0]=0h(0dB)	78	88		dB
		MGAIN[2:0]=3h(+21dB)	70	80		dB
	Dynamic Range (A-weighted) (Note 11)	MGAIN[2:0]=0h(0dB)	86	96		dB
		MGAIN[2:0]=3h(+21dB)	76	86		dB
	S/N (A-weighted)	MGAIN[2:0]=0h(0dB)	86	96		dB
		MGAIN[2:0]=3h(+21dB)	76	86		dB
	Inter-Channel Isolation (fin=1kHz) (Note 12)		90	110		dB
	DC accuracy					
	Channel Gain Mismatch			0.0	0.3	dB
	Analog Input					
	Input Voltage (Differential)		±2.00	±2.20	±2.40	Vp-p
	Input Voltage (Single-ended)		2.00	2.20	2.40	Vp-p
	Input Impedance		22.5	30		kΩ

Note 11. S/(N+D) when -60dB FS signal is applied.

Note 12. Inter-channel isolation between AINR and AINL with –1dB FS signal input.

2. ADC2

(Ta=25ºC; AVDD=DVDD=3.3V, DVDD18=1.8V, VSS=0V, BICK=64fs; Signal frequency 1kHz; Measurement frequency = 20Hz~20kHz @fs=48kHz; with Differential Input, Unless otherwise specified.)

Parameter		min	typ	max	Unit
ADC Section	Resolution			24	Bits
	Dynamic Characteristics				
	S/(N+D) (-1dBFS)	74	82		dB
	Dynamic Range (A-weighted) (Note 11)	81	89		dB
	S/N (A-weighted)	81	89		dB
	Analog Input				
	Input Voltage (Differential)	±2.00	±2.20	±2.40	Vp-p
	Input Impedance	22.5	30		kΩ

Note 11. S/(N+D) when -60dB FS signal is applied.

■ DAC Characteristics

(Ta=25ºC; AVDD=DVDD=3.3V; DVDD18=1.8V, VSS=0V, BICK=64fs; Signal frequency 1kHz; Measurement frequency = 20Hz~20kHz @fs=48kHz; in Differential Input, Unless otherwise specified.)

Parameter			min	typ	max	Unit
DAC1 DAC2	Resolution				24	Bits
	Dynamic Characteristics					
	S/(N+D) (0 dBFS)	0dBFS output mode	82	92		dB
		-20dBFS output mode	75	85		dB
	Dynamic Range (A-weighted) (Note 11)	0dBFS output mode	100	107		dB
		-20dBFS output mode	80 (Note 15)	90		dB
	S/N (A-weighted)	0dBFS output mode	100	107		dB
		-20dBFS output mode	80 (Note 15)	90		dB
	Inter-channel Isolation (f=1kHz) (Note 13)		90	110		dB
	DC accuracy					
	Channel Gain Mismatch (Note 14)			0.0	0.7	dB
	Analog output					
	Output Voltage	0dBFS output mode	2.0	2.2	2.4	Vp-p
		-20dBFS output mode	0.2	0.22	0.24	Vp-p
	Load Resistance		5			kΩ
	Load Capacitance				30	pF

Note 11. S/(N+D) when -60dB FS signal is applied.
Note 13. Indicates isolation between each DAC of Lch and Rch when -1dBFS signal is applied.
Note 14. Channel gain mismatch between all output channels (DAC1L/R, DAC2L/R).
Note 15. Ta=25ºC, AVDD=DVDD=3.0~3.6V

DC CHARACTERISTICS

(Ta=Tmin~Tmax; AVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V; AVSS=DVSS=0V)

Parameter	Symbol	min	typ	max	Unit
High level input voltage (Note 16)	VIH	80%DVDD			V
Low level input voltage (Note 16)	VIL			20%DVDD	V
SCL, SDA High level input voltage	VIH	70%DVDD			V
SCL, SDA Low level input voltage	VIL			30%DVDD	V
High level output voltage: Iout=-100µA (Note 17)	VOH	DVDD-0.4			V
Low level output voltage: Iout=100µA (Note 17)	VOL			0.4	V
SDA Low level output voltage Iout=3mA	VOL			0.4	V
Input leak current (Note 18)	Iin			±10	µA
Input leak current XTI pin	Iix		26		µA

Note 16. SCL and SDA/SO pins are not included.
Note 17. Except the SDA/SO pin.
Note 18. Except the XTI pin.

POWER CONSUMPTION

(Ta=25ºC; AVDD=DVDD=3.3V; DVDD18=1.8V; AVSS=DVSS=0V, fin=1 kHz, 24-bit, fs=8 kHz (CKM mode = 0), DSPS=BITFS=PMOSC bits= "0" PMMB bit="1", DSP running with programmed connecting DIN2 with DOUT1 and DIN1 with DOUT3.)

Parameter			min	typ	max	Unit
Power Supplies: (Note 19)						
Power-Up (IRSTN pin = "H") CODEC+DSP						
All Circuit Power-up						
	AVDD+DVDD	AVDD=DVDD=3.3V		50	-	mA
	DVDD18	DVDD18=1.8V		50	-	mA
	Power Consumption			255		mW
	AVDD+DVDD	AVDD=DVDD=3.6V			70	mA
	DVDD18	DVDD18=1.9V			70	mA
Reset (IRSTN pin = "L"), Power-down condition (Note 20)						
AVDD+DVDD (Referential)			-	1		µA
DVDD18 (Referential)				6		µA

Note 19. The current of DVDD changes depending on the system frequency and contents of the DSP program.
Note 20. All digital input pins are fixed to DVDD or DVSS.

DIGITAL FILTER CHARACTERISTICS

■ ADC Block (ADC1/2)

1. fs=48kHz

(Ta=-40ºC ~85ºC, AVDD=DVDD=3.0~3.6V, fs=48kHz, Note 21)

Parameter	Symbol	min	typ	max	Unit
Passband (±0.1dB) (Note 22)	PB	0		18.9	kHz
(-0.2dB)			20.0		kHz
(-3.0dB)			23.0		kHz
Stopband	SB	28			kHz
Passband Ripple (Note 22)	PR			±0.04	dB
Stopband Attenuation (Note 23, Note 24)	SA	68			dB
Group Delay Distortion	ΔGD		0		μs
Group Delay (Ts=1/fs)	GD		16		Ts

Note 21. The passband and stopband frequencies are proportional to fs (system sampling rate). High-pass filter characteristics are not included.

Note 22. The passband is from DC to 18.9kHz when fs=48kHz.

Note 23. The stopband is 28kHz to 3.044MHz when fs=48kHz.

Note 24. When fs = 48kHz, the analog modulator samples the input signal at 3.072MHz. There is no attenuation of an input signal in band (n x 3.072MHz ±28kHz; n=0, 1, 2, 3…) of integer times of the sampling frequency by the digital filter.

■ DAC1-4

(Ta=-40ºC ~85ºC; AVDD=DVDD=3.0~3.6V; fs=48kHz; DEM=OFF)

Parameter	Symbol	min	typ	max	Unit
Passband (±0.05dB) (Note 25)	PB	0		21.7	kHz
(-6.0dB)			24		kHz
Stopband (Note 25)	SB	26.2			kHz
Passband Ripple	PR			±0.01	dB
Stopband Attenuation	SA	64			dB
Group Delay (Ts=1/fs) (Note 26)	GD		24		Ts
Digital Filter + Analog Filter					
Amplitude Characteristics 20Hz~20.0kHz			±0.5		dB

Note 25. The pass band and stop band frequencies are proportional to “fs” (system sampling rate), and represents PB=0.4535fs (@±0.05dB) and SB=0.5465fs, respectively.

Note 26. The digital filter delay is calculated as the time from setting data into the input register until an analog signal is output.

SWITCHING CHARACTERISTICS

■ System Clock

(Ta=-40ºC~85ºC; AVDD=DVDD=3.0~3.6V, VSS =0V)

Parameter	Symbol	min	typ	max	Unit
XTI CKM[2:0]=000, 001, 010					
a) with a Crystal Oscillator:					
CKM[2:0]=000 fs=44.1kHz fs=48kHz	fXTI	-	11.2896 12.288	-	MHz
CKM[2:0]=001 fs=44.1kHz fs=48kHz	fXTI	-	16.9344 18.432	-	MHz
b) with an External Clock					
Duty Cycle		40	50	60	%
CKM[2:0]=000, 010 fs=44.1kHz fs=48kHz	fXTI	11.0	11.2896 12.288	12.4	MHz
CKM[2:0]=001 fs=44.1kHz fs-48kHz	fXTI	16.5	16.9344 18.432	18.6	MHz
LRCK Frequency (Note 27)	fs	7.35		48	kHz
BICK Frequency					
High Level Width Low Level Width Frequency	tBCLKH tBCLKL fBCLK	64 64 0.23	 3.072	 3.1	ns ns MHz

Note 27. LRCK frequency and sampling rate (fs) should be the same.
Note 28. When BICK is the source of the master clock, it should be synchronized to LRCK and have stable frequency.

■ Reset

(Ta= Tmin~Tmax, AVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V; AVSS=DVSS=0V)

Parameter	Symbol	min	typ	max	Unit
Reset pulse width (Note 29)	tRST	600			ns

Note 29. Set the IRSTN pin to “H” after all power supplies are fed.

■ Digital Audio Interface (SDIN1-2, SDOUT1-3)

1) SDIN1/2, SDOUT1/2/3
(Ta= Tmin~Tmax, AVDD=DVDD= 3.0V ~ 3.6V, DVDD18= 1.7V ~ 1.9V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
I^2S and PCM Interface Input Timing					
Delay Time from BICK "↑" to LRCK (Note 30)	tBLRD	20			ns
Delay Time from LRCK to BICK "↑" (Note 30)	tLRBD	20			ns
Serial Data Input Latch Setup Time	tBSIDS	80			ns
Serial Data Input Latch Hold Time	tBSIDH	80			ns
Delay Time from LRCK to Serial Data Output (Note 31)	tLRD			80	ns
Delay Time from BICK "↓" or "↑"to LRCK Output	tBSOD			80	ns
I^2S and PCM Interface Output Timing SDOUT1/2					
BICK Frequency	fBICK		64		fs
BICK Duty cycle			50		%
Delay Time from BICK "↓" to LRCK	tMBL	-20		40	ns
Serial Data Input Latch Setup Time	tBSIDS	80			ns
Serial Data Input Latch Hold Time	tBSIDH	80			ns
Delay Time from LRCK to Serial Data Output (Note 31)	tLRD			80	ns
Delay Time from BICK "↓" or "↑"to LRCK Output	tBSOD			80	ns

Note 30. BICK edge must not occur at the same time as LRCK edge.
Note 31. Except I^2S.

■ µP Interface (SPI mode)

(Ta= Tmin~Tmax; AVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V, AVSS=DVSS=0V; CL=20pF)

Parameter	Symbol	min	typ	max	Unit
µP Interface Timing (SPI mode)					
CSN Fall Time	tWRF			30	ns
CSN Rise Time	tWRR			30	ns
SCLK Fall Time	tSF			30	ns
SCLK Rise Time	tSR			30	ns
SCLK Frequency	fSCLK			2.7	MHz
SCLK Low Level Width	tSCLKL	180			ns
SCLK High Level Width	tSCLKH	180			ns
CSN High Level Width	tWRQH	500			ns
From CSN "↑" to IRSTN "↑"	tRST1	600			ns
From IRSTN "↑" to CSN "↓"	tIRRQ	100			µs
From CSN "↓" to SCLK "↓"	tWSC	500			ns
From SCLK "↑" to CSN "↑"	tSCW	800			ns
SI Latch Setup Time	tSIS	180			ns
SI Latch Hold Time	tSIH	180			ns
AK7757 → µP					
Delay Time from SCLK "↓"to SO Output	tSOS			180	ns
Hold Time from SCLK "↑" to SO Output (Note 32)	tSOH	180			ns

Note 32. Except for, when writing to 8th bit of command code.

■ µP Interface (I^2C BUS mode)

(Ta= Tmin~Tmax; AVDD=DVDD=3.0~3.6V, DVDD18=1.7~1.9V, AVSS=DVSS=0V; CL=20pF)

Parameter	Symbol	min	typ	max	Unit
I^2C Timing					
SCL clock frequency	fSCL			400	kHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF

Note 33. I^2C-bus is a trademark of NXP B.V.

■ **Timing Diagram**

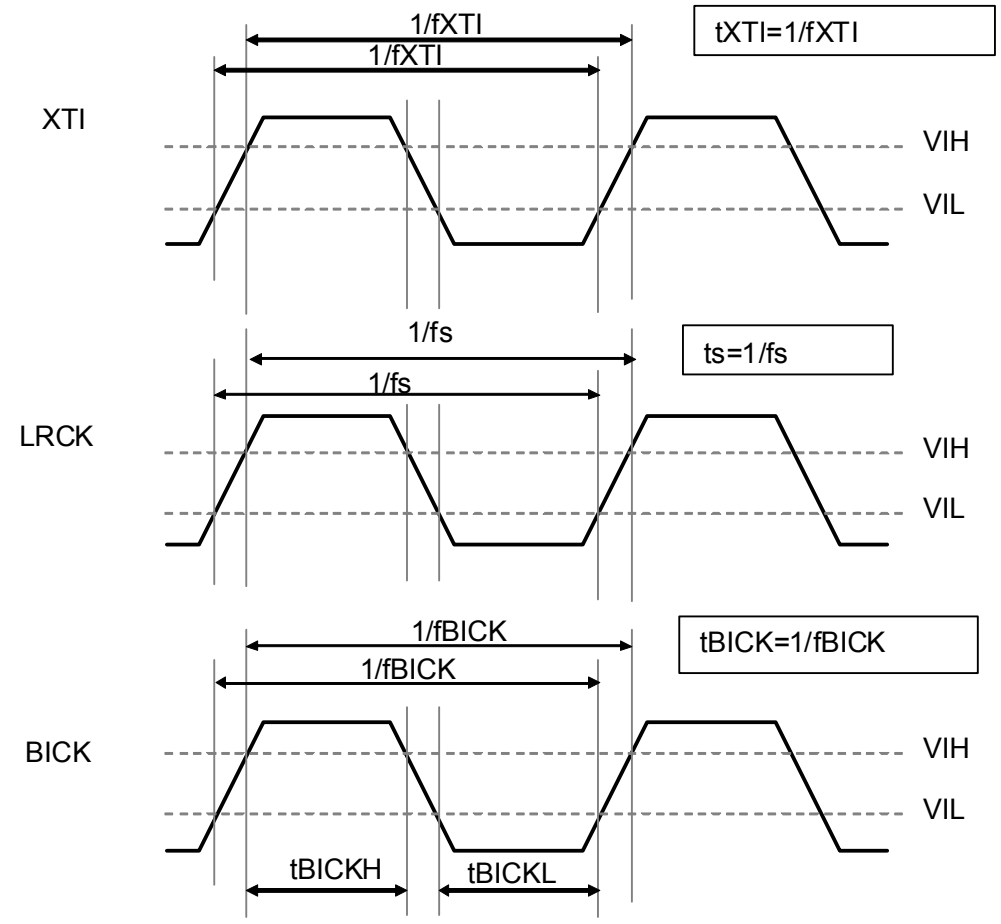


Figure 3. System Clock

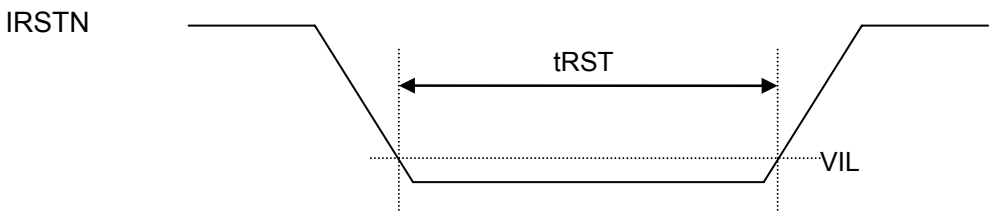


Figure 4. Reset

Note 34. The IRSTN pin must be "L" when power-up/power-down the AK7757.

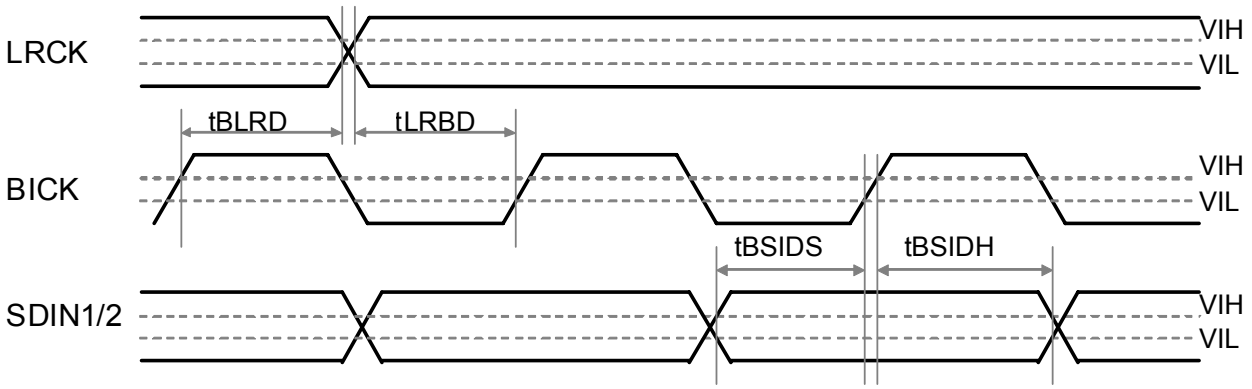


Figure 5. Audio Interface (Input Interface in Slave Mode)

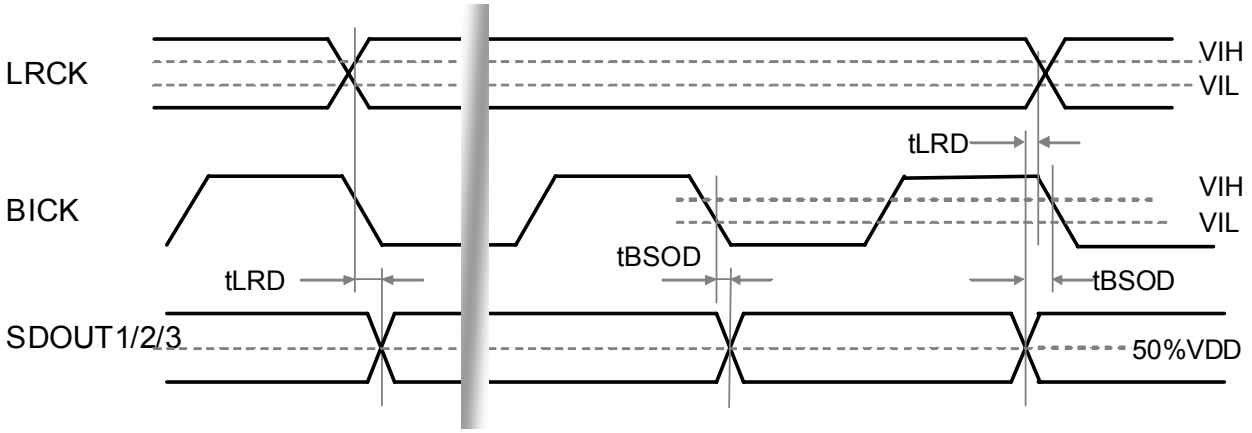


Figure 6. Audio Interface (Output Interface in Slave Mode)

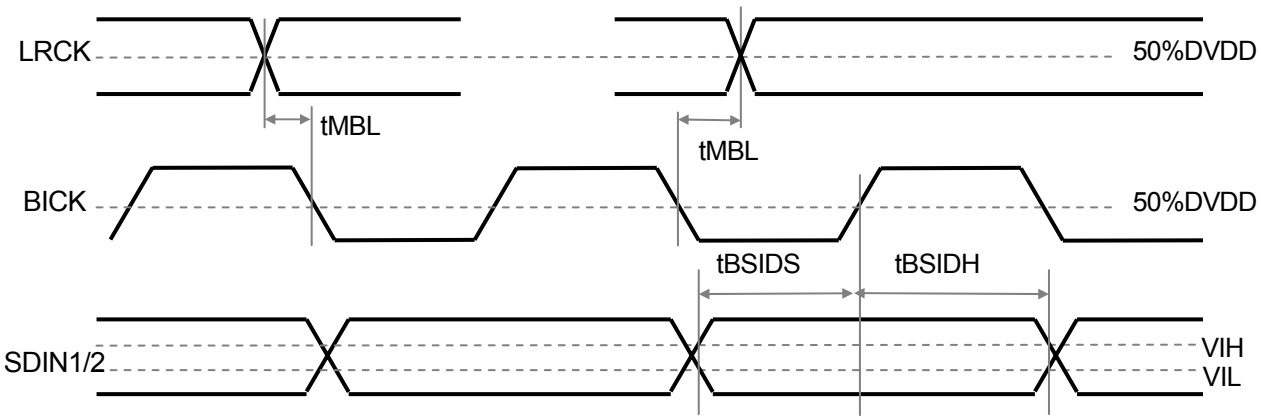


Figure 7. Audio Interface (Input Interface in Master Mode)

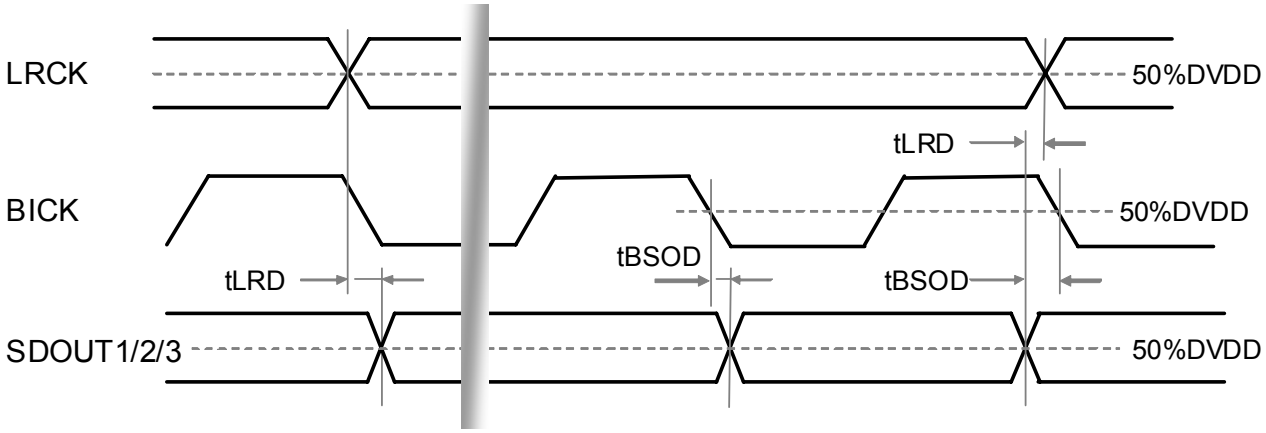


Figure 8. Audio Interface (Output Interface in Master Mode)

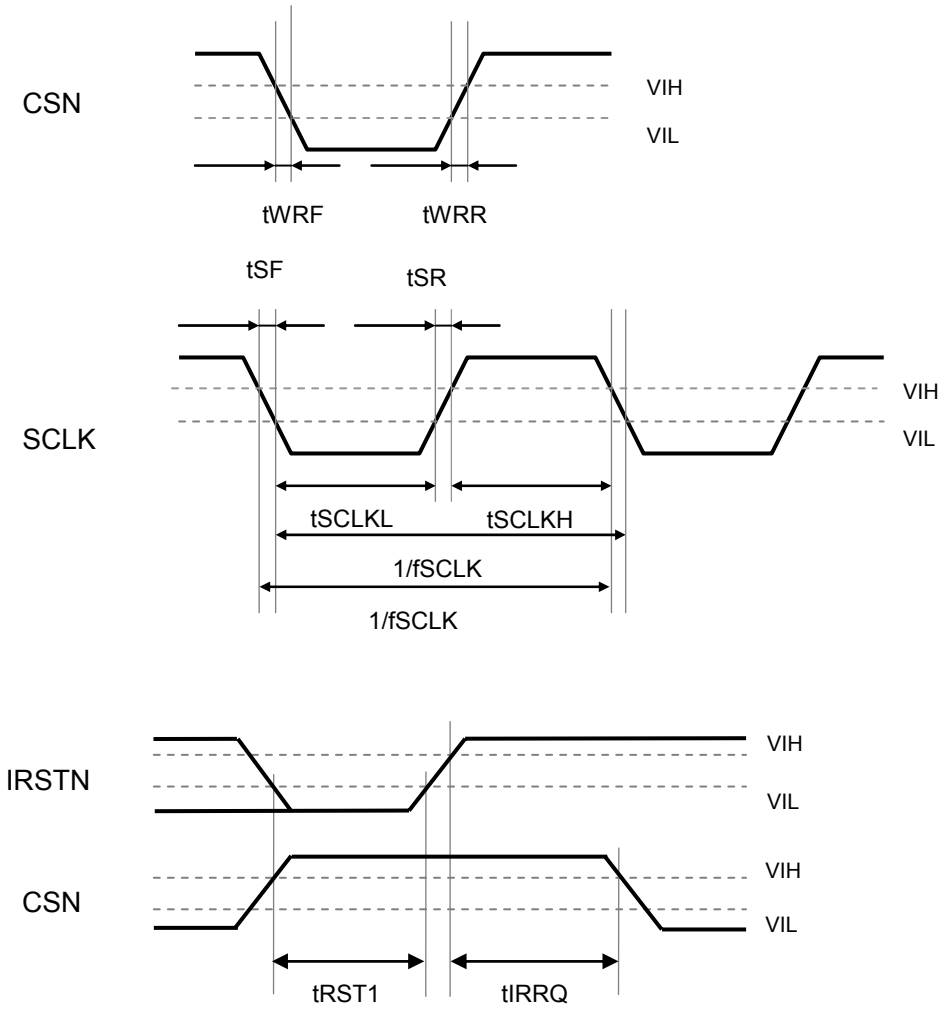


Figure 9. µP Interface 1 (SPI)

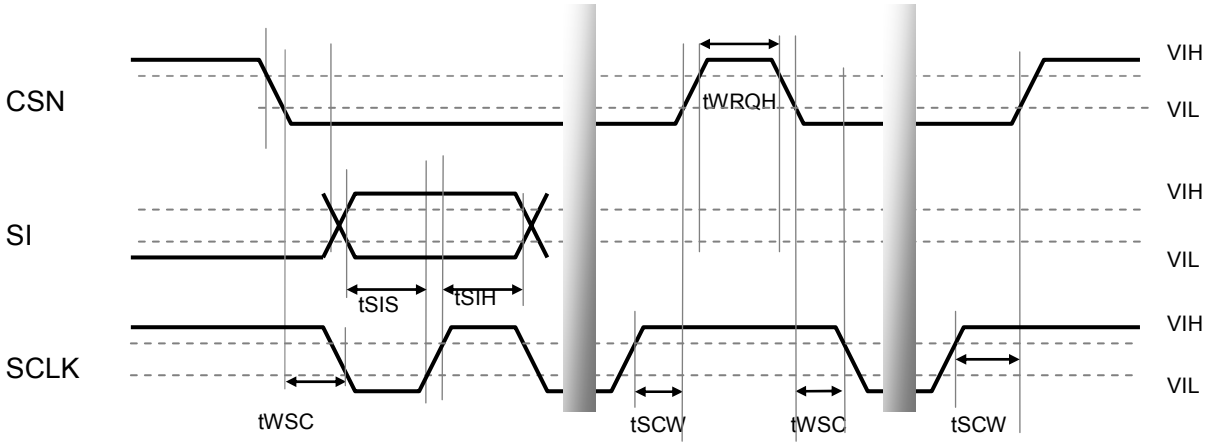


Figure 10. µP Interface 2 (SPI)

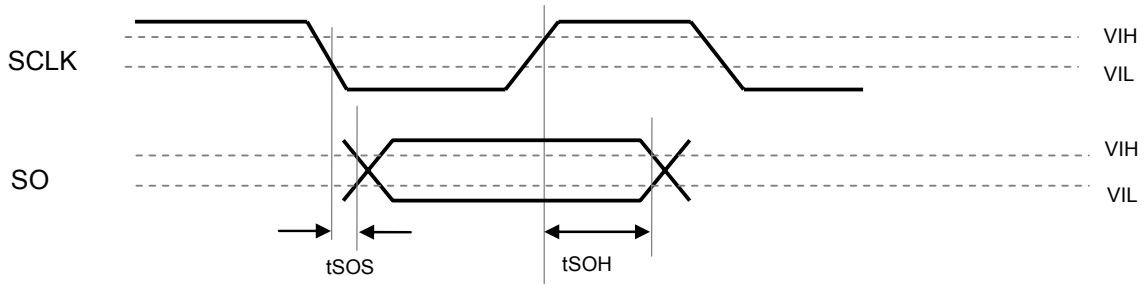


Figure 11. µP Interface 3 (SPI)

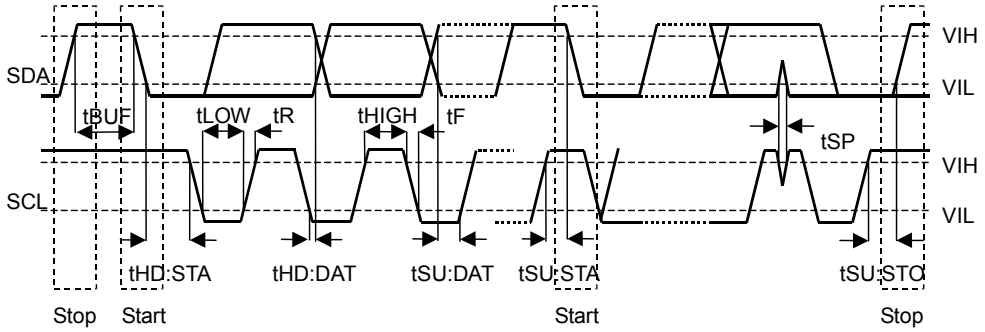
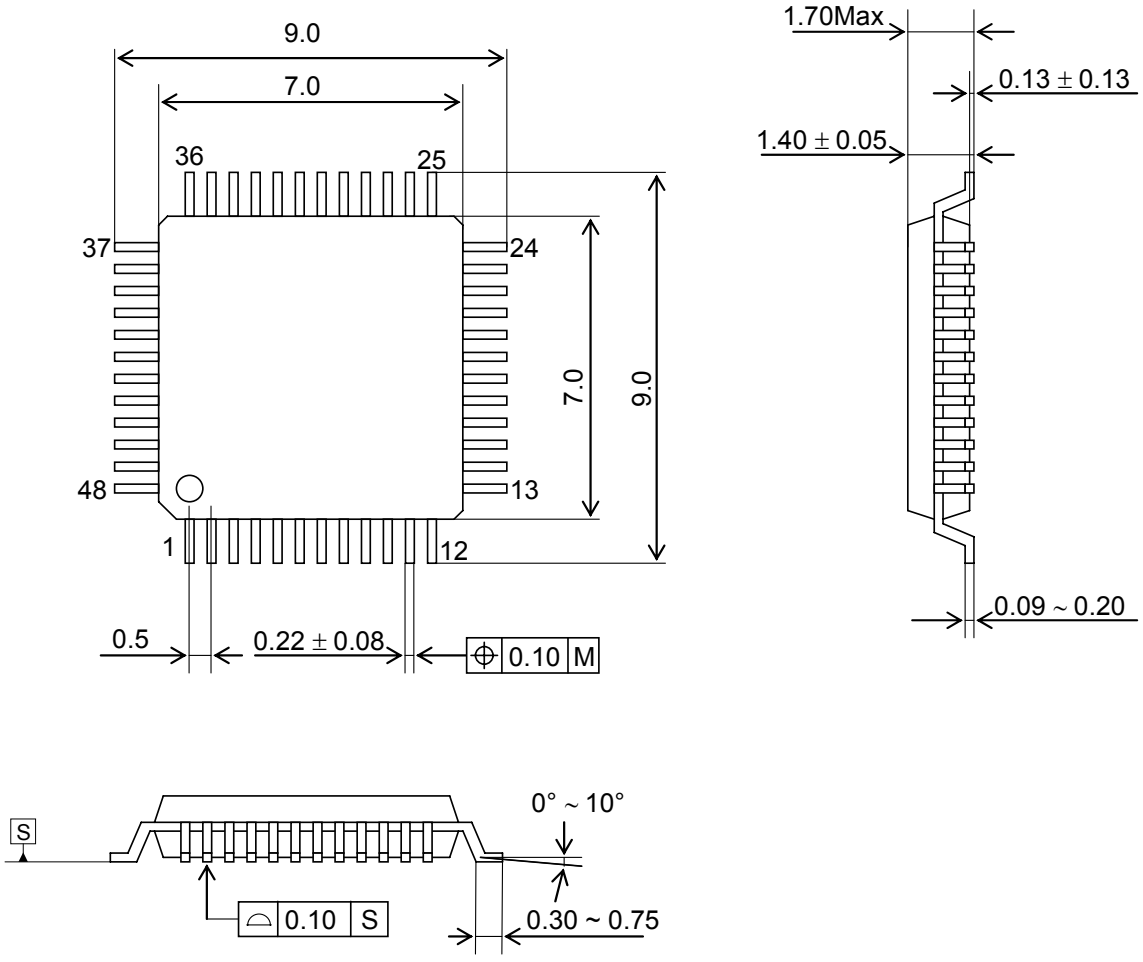


Figure 12. µP Interface (I^2C Bus)

PACKAGE

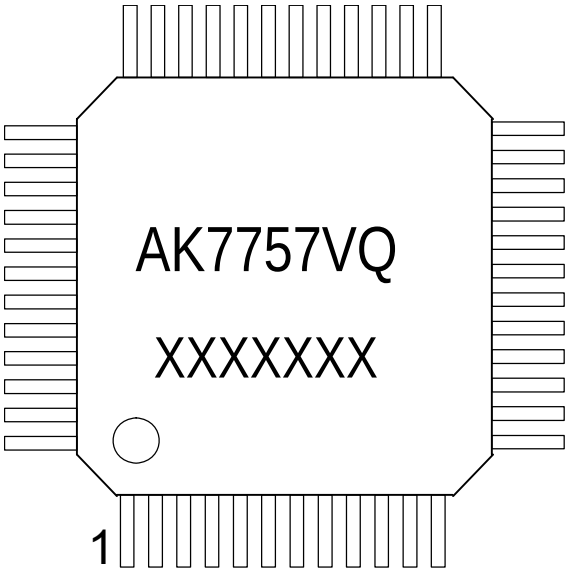
48pin LQFP(Unit: mm)



■ Materials and Lead Specification

Package:	Epoxy
Lead frame:	Copper
Lead-finish:	Soldering (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code: XXXXXXX(7digits)
3) Marking Code: AK7757VQ

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
13/01/24	00	First Edition		
13/05/17	01	Error Correction	12	DC CHARACTERISTICS Note 16 was changed.
		Specification Change	16	■ µP Interface (SPI mode) µP Interface Timing (SPI mode) SCLK Frequency: 2.1 → 2.7MHz (max) SCLK Low Level Width: 200 → 180ns (min) SCLK High Level Width: 200 → 180ns (min) SI Latch Setup Time: 200 → 180ns (min) SI Latch Hold Time: 200 → 180ns (min) AK7757 →µP Delay Time from SCLK "↓" to SO Output: 200→180ns(max) Hold Time from SCLK "↑" to SO Output: 200→180ns (min)
13/07/10	02	Error Correction	6	PIN FUNCTION Pin No.37~40: "Differential Analog Output Pin" → "Analog Output Pin"

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