

## 4.5-V TO 16-V INPUT, HIGH CURRENT, SYNCHRONOUS STEP DOWN THREE DC-DC CONVERTERS WITH INTEGRATED FET

Check for Samples: [TPS652510](#)

### FEATURES

- **Wide Input Supply Voltage Range:**  
4.5 V - 16 V
- **0.8-V, 1% Accuracy Reference**
- **Continuous Loading:**  
3 A (Buck1), 2 A (Buck2 and 3)
- **Maximum Current:**  
3.5 A (Buck 1), 2.5 A (Buck2 and 3)
- **Synchronous Operation, 300-kHz – 2.2-MHz**  
Switching Frequency Set By External Resistor
- **External Enable Pins With Built-In Current**  
Source for Easy Sequencing
- **External Soft Start Pins**
- **Adjustable Cycle-by-Cycle Current Limit Set by External Resistor**
- **Current-Mode Control With Simple Compensation Circuit**
- **Automatic Low Pulse Skipping (PSM) Power Mode, Allowing for an Output Ripple Better than 2%**
- **Support Pre-Biased Outputs**
- **Power Good Supervisor and Reset Generator**
- **Small, Thermally Efficient 40-Pin 6-mm x 6-mm RHA (QFN) package**
- **-40°C to 125°C Junction Temperature Range**

### DESCRIPTION/ORDERING INFORMATION

TPS652510 is a power management IC with three step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. The converters are designed to simplify its application while giving the designer the option to optimize their usage according to the target application.

The converters can operate in 5-, 9-, 12- or 15-V systems. The output voltage can be set externally using a resistor divider to any value between 0.8 V and the input supply minus the resistive drops on the converter path. Each converter features enable pin that allows a delayed start-up for sequencing purposes, soft start pin that allows adjustable soft-start time by choosing the soft-start capacitor, and a current limit (RLIM) pin that enables designer to adjust current limit by selecting an external resistor and optimize the choice of inductor. All converters operate in 'hiccup mode': Once an over-current lasting more than 10 ms is sensed in any of the converters, they will shut down for 10 ms and then the start-up sequencing will be tried again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case the converter will see another over-current event and shuts down again repeating the cycle (hiccup) until the failure is cleared. If an overload condition lasts for less than 10 ms, only the relevant converter affected will shut-down and re-start and no global hiccup mode will occur.

The switching frequency of the converters is set by an external resistor connected to ROSC pin. The switching regulators are designed to operate from 300 kHz to 2.2 MHz. The converters operate with 180° phase between them to minimize the input filter requirements. All converters have peak current mode control which simplifies external frequency compensation.

The device has a built-in slope compensation ramp to prevent sub harmonic oscillations in peak current mode control. A traditional type II compensation network can stabilize the system and achieve fast transient response. Moreover, an optional capacitor in parallel with the upper resistor of the feedback divider provides one more zero and makes the crossover frequency over 100 kHz.

All converters feature an automatic low power pulse PFM skipping mode which improves efficiency during light loads and standby operation, while guaranteeing a very low output ripple, allowing for a value of less than 2% at low output voltages.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

The device incorporates an overvoltage transient protection circuit to minimize voltage overshoot. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVP threshold which is 109% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP lower threshold which is 107%, the high side MOSFET is allowed to turn on the next clock cycle.

TPS652510 features a supervisor circuit which monitors each buck’s output and the PGOOD pin is asserted once sequencing is done. The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when all converter outputs are more than 90% of its nominal output voltage. The default reset time is 100 ms. The polarity of the PGOOD is active high.

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop operating when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

**ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	40-Pin (QFN) - RHA	Reel of 2500	TPS652510RHAR	TPS652510

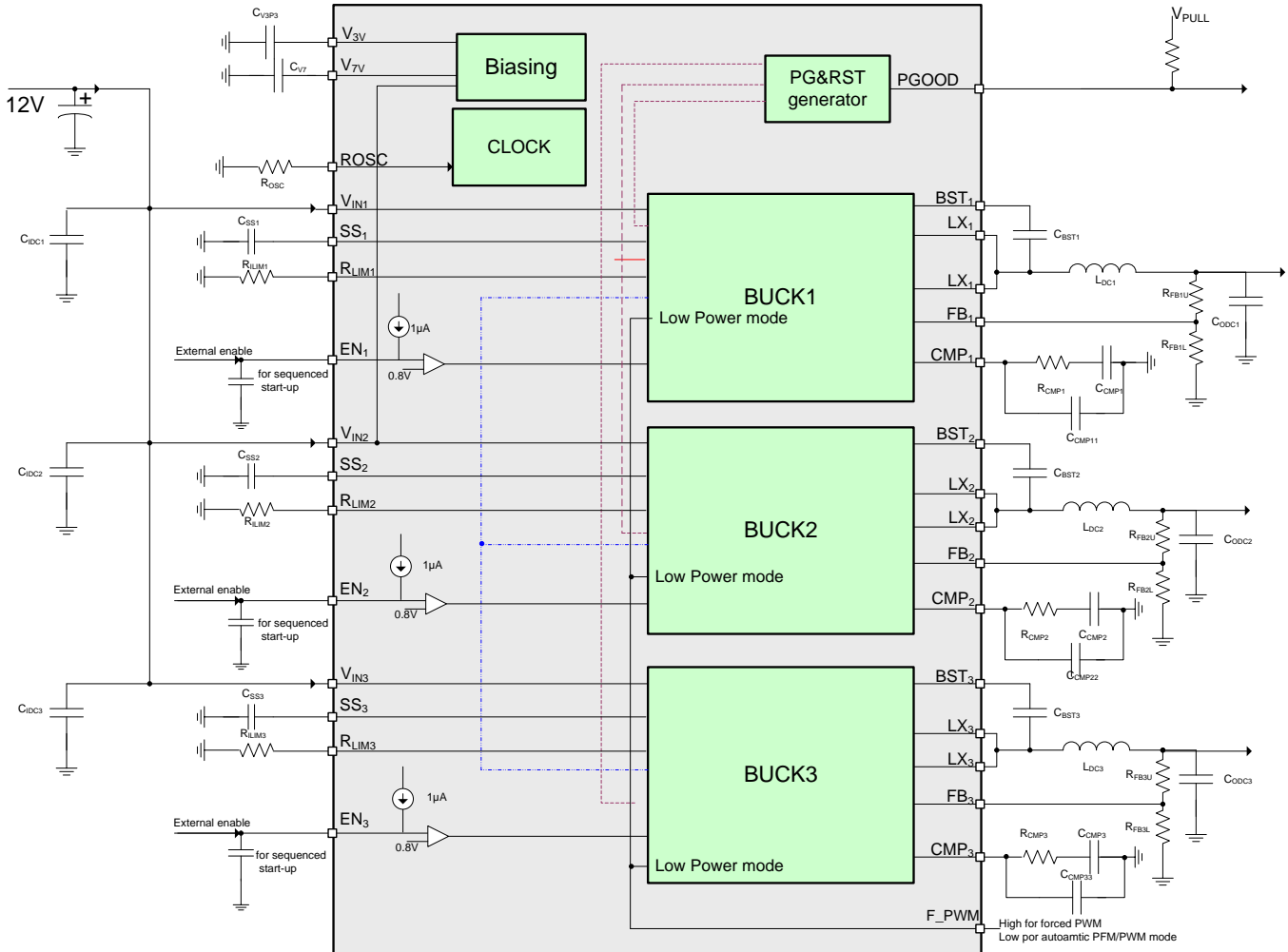
- (1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



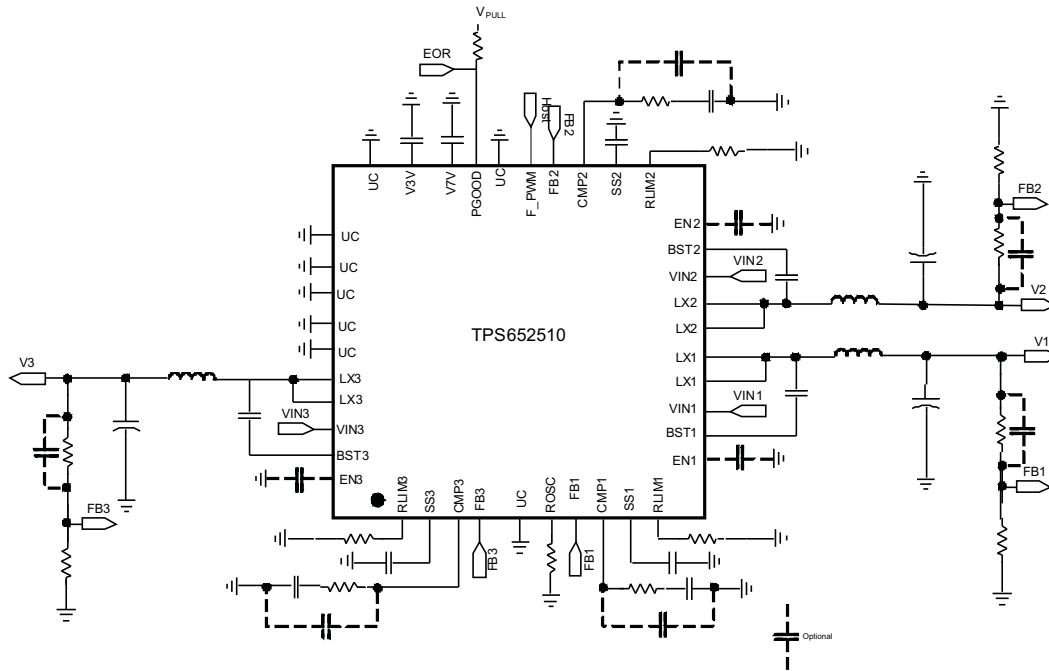
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

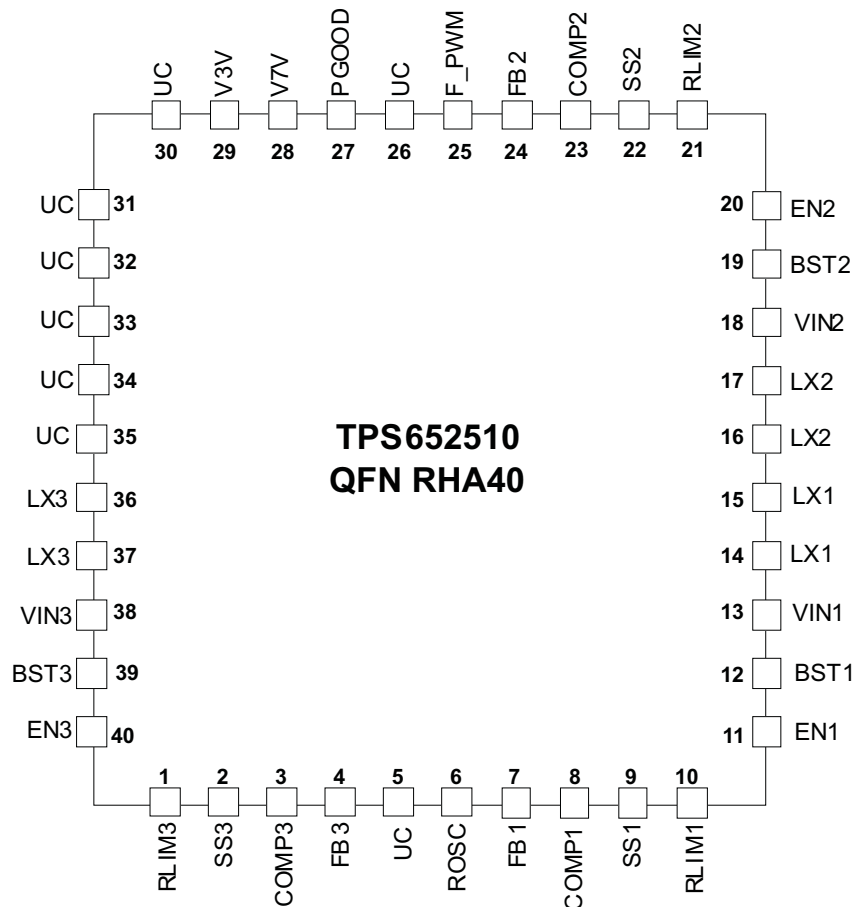
**FUNCTIONAL BLOCK DIAGRAM**



TYPICAL APPLICATION



PIN OUT



**TERMINAL FUNCTIONS**

NAME	NO.	I/O	DESCRIPTION
RLIM3	1	I	Current limit setting for Buck3. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS3	2	I	Soft start pin for Buck3. Fit a small ceramic capacitor to this pin to set the converter soft start time.
COMP3	3	O	Compensation for Buck3. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB3	4	I	Feedback pin for Buck3. Connect a divider set to 0.8 V from the output of the converter to ground.
UC	5		Unused pin, connect to ground
ROSC	6	I	Oscillator set. This resistor sets the frequency of internal autonomous clock.
FB1	7	I	Feedback pin for Buck1. Connect a divider set to 0.8 V from the output of the converter to ground.
COMP1	8	O	Compensation pin for Buck1. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
SS1	9	I	Soft-start pin for Buck1. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
RLIM1	10	I	Current limit setting pin for Buck1. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
EN1	11	I	Enable pin for Buck1. A high signal on this pin enables the regulator Buck. For a delayed start-up add a small ceramic capacitor from this pin to ground.
BST1	12		Bootstrap capacitor for Buck1. Fit a 47-nF ceramic capacitor from this pin to the switching node.
VIN1	13	I	Input supply for Buck1. Fit a 10- $\mu$ F ceramic capacitor close to this pin.
LX1	14, 15	O	Switching node for Buck1
LX2	16, 17	O	Switching node for Buck2
VIN2	18	I	Input supply for Buck2. Fit a 10- $\mu$ F ceramic capacitor close to this pin.
BST2	19		Bootstrap capacitor for Buck2. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN2	20	I	Enable pin for Buck2. A high signal on this pin enables the regulator. For a delayed start-up add a small ceramic capacitor from this pin to ground.
RLIM2	21	I	Current limit setting pin for Buck2. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS2	22	I	Soft-start pin for Buck2. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
COMP2	23	O	Compensation pin for Buck2. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB2	24	I	Feedback input for Buck2. Connect a divider set to 0.8 V from the output of the converter to ground.
F_PWM	25		Forces PWM operation in all converters when set high. If low converters will operate in automatic PFM/PWM mode.
UC	26		Unused pin, connect to ground
PGOOD	27	O	Power good. Open drain output asserted low after all converters and sequenced and within regulation. Polarity is factory selectable (active high default).
V7V	28	O	Internal supply. Connect a 4.7- $\mu$ F to 10- $\mu$ F ceramic capacitor from this pin to ground.
V3V	29	O	Internal supply. Connect a 3.3- $\mu$ F to 10- $\mu$ F ceramic capacitor from this pin to ground.
UC	30		Unused pin, connect to ground
UC	31		Unused pin, connect to ground
UC	32		Unused pin, connect to ground
UC	33		Unused pin, connect to ground
UC	34		Unused pin, connect to ground

**TERMINAL FUNCTIONS (continued)**

NAME	NO.	I/O	DESCRIPTION
UC	35		Unused pin, connect to ground
LX3	36, 37	O	Switching node for Buck3
VIN3	38	I	Input supply for Buck3. Fit a 10- $\mu$ F ceramic capacitor close to this pin.
BST3	39	I	Bootstrap capacitor for Buck3. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN3	40	I	Enable pin for Buck3. A high signal on this pin enables the converter. For a delayed start-up add a small ceramic capacitor from this pin to ground.
PowerPAD			PowerPAD. Connect to system ground for electrical and thermal connection.

**ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted, all voltages are with respect to GND)

Voltage range at VIN1, VIN2, VIN3, LX1, LX2, LX3	-0.3 to 18	V
Voltage range at LX1, LX2, LX3 (maximum withstand voltage transient < 10 ns)	-3 to 18	V
Voltage at BST1, BST2, BST3 referenced to LX pin	-0.3 to 7	V
Voltage at V7V, COMP1, COMP2, COMP3	-0.3 to 7	V
Voltage at V3V, RLIM1, RLIM2, RLIM3, EN1, EN2, EN3, SS1, SS2, SS3, FB1, FB2, FB3, F_PWM, PGOOD, ROSC	-0.3 to 3.6	V
T <sub>J</sub> Operating junction temperature range	-40 to 125	°C
T <sub>STG</sub> Storage temperature range	-55 to 150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VIN Input operating voltage	4.5		16	V
T <sub>A</sub> Junction temperature	-40		85	°C

**ELECTROSTATIC DISCHARGE (ESD) PROTECTION**

	MIN	MAX	UNIT
Human body model (HBM)	2000		V
Charge device model (CDM)	500		V

**PACKAGE DISSIPATION RATINGS <sup>(1)</sup>**

PACKAGE	$\theta_{JA}$ (°C/W)	T <sub>A</sub> = 25°C POWER RATING (W)	T <sub>A</sub> = 55°C POWER RATING (W)	T <sub>A</sub> = 85°C POWER RATING (W)
RHA	30	3.33	2.3	1.3

- (1) Based on JEDEC 51.5 HIGH K environment measured on a 76.2 x 114 x 0.6-mm board with the following layer arrangement:  
 (a) Top layer: 2 Oz Cu, 6.7% coverage  
 (b) Layer 2: 1 Oz Cu, 90% coverage  
 (c) Layer 3: 1 Oz Cu, 90% coverage  
 (d) Bottom layer: 2 Oz Cu, 20% coverage

## ELECTRICAL CHARACTERISTICS

 $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $f_{SW} = 500\text{ kHz}$  (unless otherwise noted)

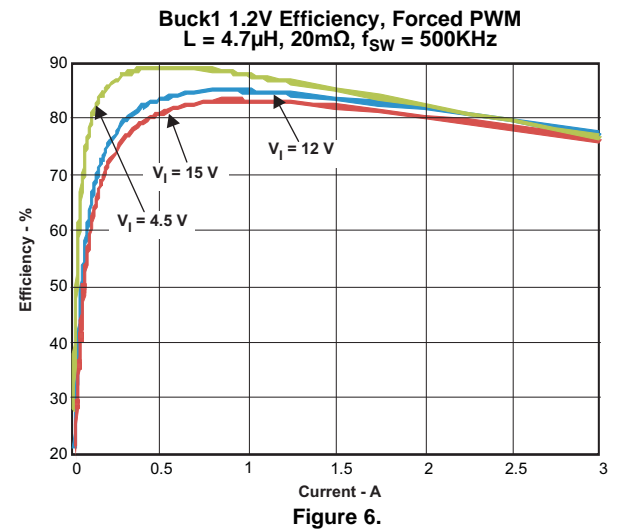
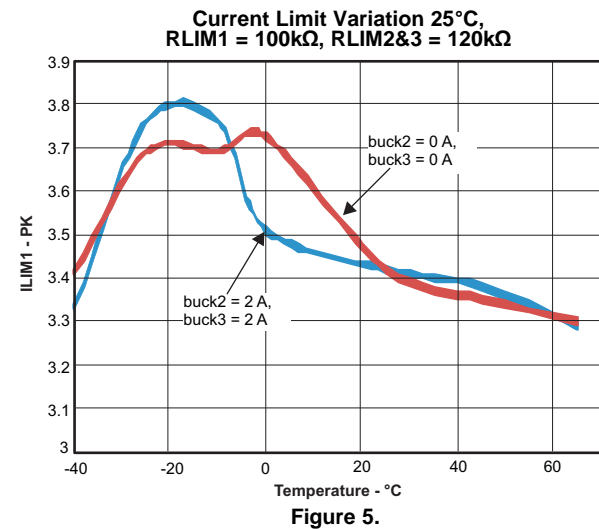
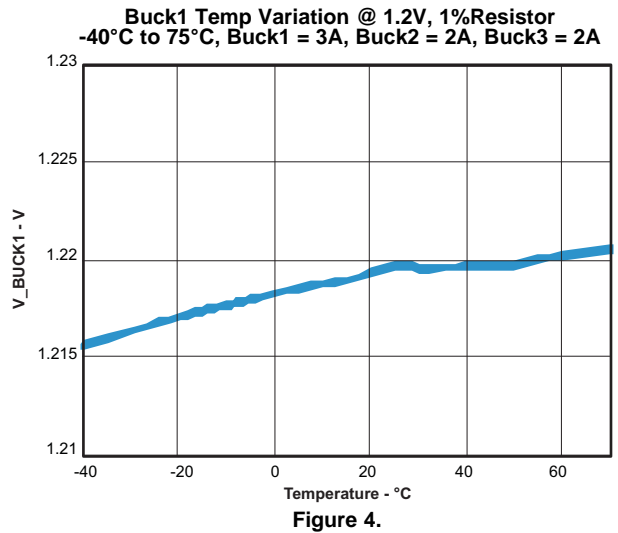
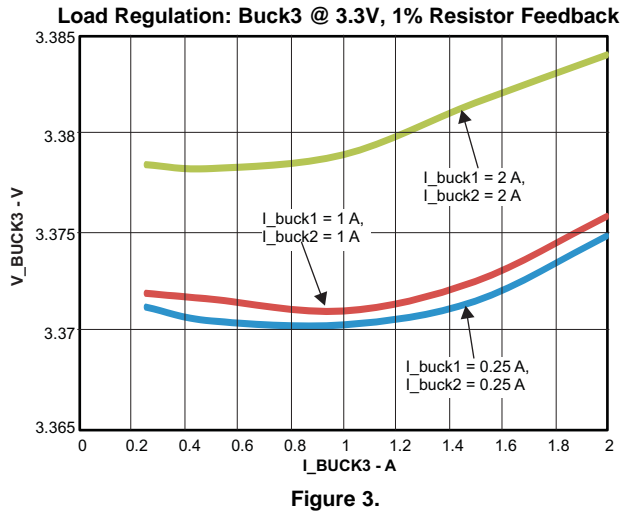
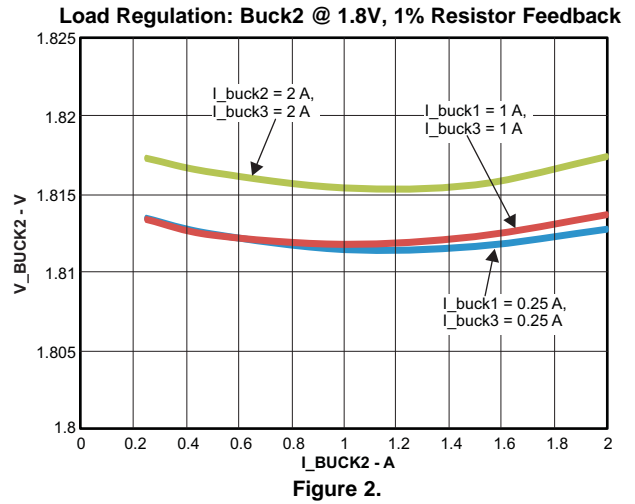
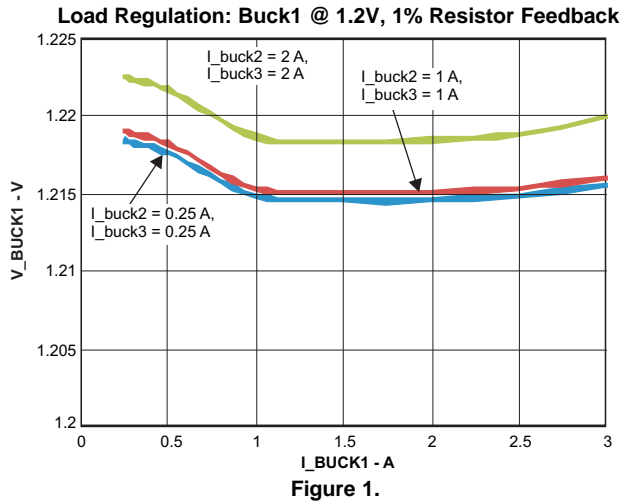
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT SUPPLY UVLO AND INTERNAL SUPPLY VOLTAGE</b>						
$V_{IN}$	Input voltage range		4.5		16	V
$I_{DDSDN}$	Shutdown	EN pin = low for all converters		170		$\mu\text{A}$
$I_{DDQ}$	Quiescent	Converters enabled, no load Buck1 = 1.2 V Buck2 = 1.8 V Buck3 = 3.3 V $T_A = 25^{\circ}\text{C}$ , F_PWM = Low		600		$\mu\text{A}$
	Quiescent, forced PWM	Converters enabled, no load F_PWM = High, L = 4.7 $\mu\text{H}$		18		mA
UVLO	$V_{IN}$ under voltage lockout	Rising $V_{IN}$		4.22		V
		Falling $V_{IN}$		4.1		
$UVLO_{DEGLITCH}$		Both edges		110		$\mu\text{s}$
$V_{3V}$	Internal biasing supply	$I_{LOAD} = 0\text{ mA}$	3.2	3.3	3.4	V
$I_{3V}$	Biasing supply output current	$V_{IN} = 12\text{ V}$			10	mA
$V_{7V}$	Internal biasing supply	$I_{LOAD} = 0\text{ mA}$	5.63	6.25	6.88	V
$I_{7V}$	Biasing supply output current	$V_{IN} = 12\text{ V}$			10	mA
$V_{7VUVLO}$	UVLO for internal V7V rail	Rising V7V		3.8		V
		Falling V7V		3.6		
$V_{7VUVLO\_DEGLITCH}$		Falling edge		110		$\mu\text{s}$
<b>BUCK CONVERTERS (ENABLE CIRCUIT, CURRENT LIMIT, SOFT-START AND SWITCHING FREQUENCY)</b>						
$V_{IH\_ENx}$	Enable threshold high	V3p3 = 3.2 V - 3.4 V, $V_{ENx}$ rising	1.55		1.82	V
$V_{IH}$	Enable high level	External GPIO	0.66 x V3p3			V
$V_{IL\_ENx}$	Enable threshold low	V3p3 = 3.2 V - 3.4 V, $V_{ENx}$ falling	0.98		1.24	V
$V_{IL}$	Enable low level	External GPIO			0.33 x V3p3	V
$I_{CHEN}$	Pull up current enable pin			1		$\mu\text{A}$
$t_D$	Discharge time enable pins	Power-up		10		ms
$I_{SS}$	Soft-start pin current source			5		$\mu\text{A}$
$F_{SW\_BK}$	Converter switching frequency range	Set externally with resistor	0.3		2.2	MHz
$R_{FSW}$	Frequency setting resistor		50		600	k $\Omega$
$f_{SW\_TOL}$	Internal oscillator accuracy	$f_{SW} = 800\text{ kHz}$	-10		10	%
<b>FEEDBACK, REGULATION, OUTPUT STAGE</b>						
$V_{FB}$	Feedback voltage	$V_{IN} = 12\text{ V}$ , $T_A = 25^{\circ}\text{C}$	-1%	0.8	1%	V
		$V_{IN} = 4.5\text{ V}$ to 16 V	-2%	0.8	2%	
$t_{ON\_MIN}$	Minimum on time (current sense blanking)				135	ns
$RLIM_x$	Limit resistance range		75		300	k $\Omega$
$ILIM_1$	Buck 1 adjustable current limit range	$V_{IN} = 12\text{ V}$ , $f_{SW} = 500\text{ kHz}$ , See <a href="#">Figure 36</a>	1.2		5.05	A
$ILIM_2$	Buck 2 adjustable current limit range	$V_{IN} = 12\text{ V}$ , $f_{SW} = 500\text{ kHz}$ , See <a href="#">Figure 37</a>	1.2		4.7	A
$ILIM_3$	Buck 3 adjustable current limit range	$V_{IN} = 12\text{ V}$ , $f_{SW} = 500\text{ kHz}$ , See <a href="#">Figure 38</a>	1.3		4.7	A

**ELECTRICAL CHARACTERISTICS (continued)**
 $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $f_{SW} = 500\text{ kHz}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>MOSFET (BUCK 1)</b>						
H.S. Switch	On resistance of high side FET on CH1	25°C, BOOT = 6.5 V		95		mΩ
L.S. Switch	On resistance of low side FET on CH1	25°C, VIN = 12 V		50		mΩ
<b>MOSFET (BUCK 2)</b>						
H.S. Switch	On resistance of high side FET on CH2	25°C, BOOT = 6.5 V		120		mΩ
L.S. Switch	On resistance of low side FET on CH2	25°C, VIN = 12 V		80		mΩ
<b>MOSFET (BUCK 3)</b>						
H.S. Switch	On resistance of high side FET on CH3	25°C, BOOT = 6.5 V		120		mΩ
L.S. Switch	On resistance of low side FET on CH3	25°C, VIN = 12 V		80		mΩ
<b>ERROR AMPLIFIER</b>						
$g_M$	Error amplifier transconductance	-2 μA < ICOMP < 2 μA		130		μS
$g_{mPS}$	COMP to ILX gm	I <sub>LX</sub> = 0.5 A		10		A/V
<b>POWER GOOD RESET GENERATOR</b>						
$V_{UV\_BUCKX}$	Threshold voltage for buck under voltage	Output falling		85		%
		Output rising (PG will be asserted)		90		
$t_{UV\_deglitch}$	Deglintch time (both edges)			11		ms
$t_{ON\_HICCUP}$	Hiccup mode ON time	VUV <sub>BUCKX</sub> asserted		12		ms
$t_{OFF\_HICCUP}$	Hiccup mode OFF time	All converters disabled. Once t <sub>OFF\_HICCUP</sub> elapses, all converters will go through sequencing again.		20		ms
$VOV\_BUCKX$	Threshold voltage for buck over voltage	Output rising (high side FET will be forced off)		109		%
		Output falling (high side FET will be allowed to switch )		107		
$t_{RP}$	minimum reset period	Measured after the later of Buck1 or Buck3 power-up successfully		100		ms
<b>THERMAL SHUTDOWN</b>						
$T_{TRIP}$	Thermal shut down trip point	Rising temperature		160		°C
$T_{HYST}$	Thermal shut down hysteresis	Device re-starts		20		°C
$T_{TRIP\_DEGLITCH}$	Thermal shut down deglitch			110		μs



TYPICAL CHARACTERISTICS



**TYPICAL CHARACTERISTICS (continued)**

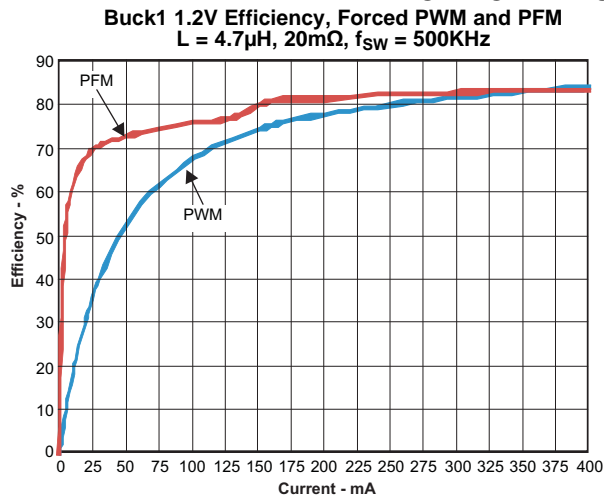


Figure 7.

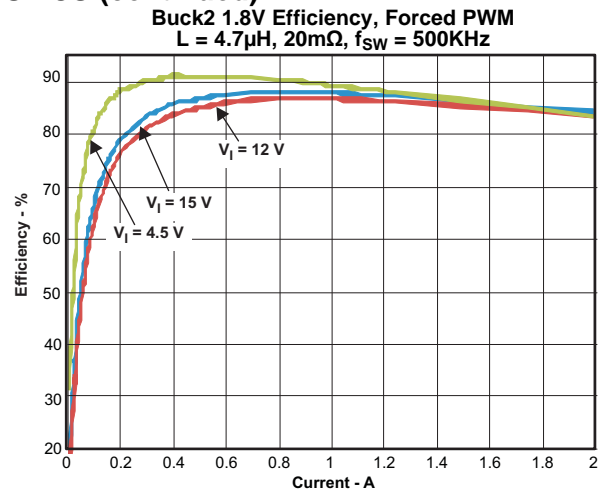


Figure 8.

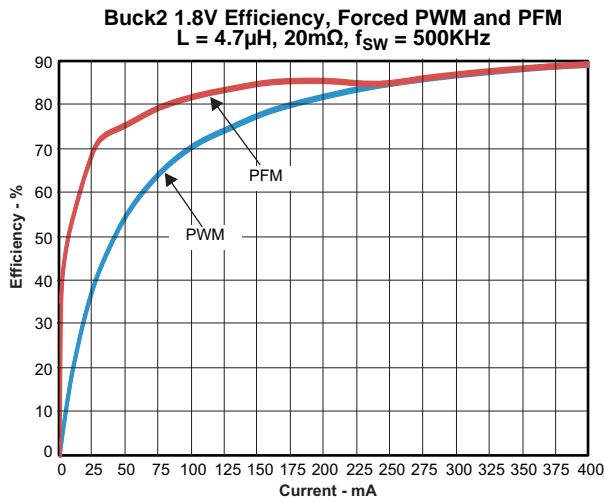


Figure 9.

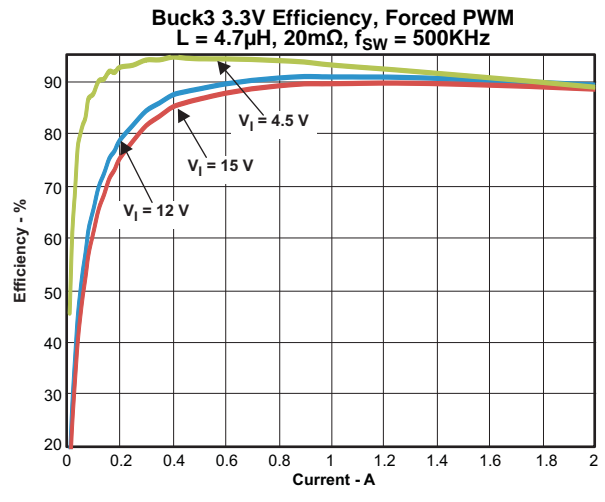


Figure 10.

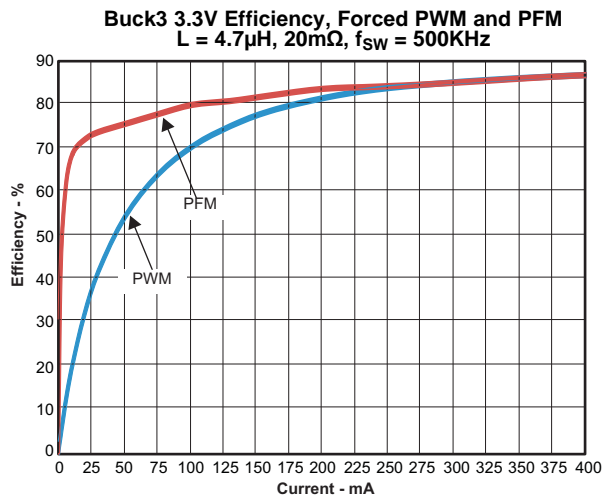


Figure 11.

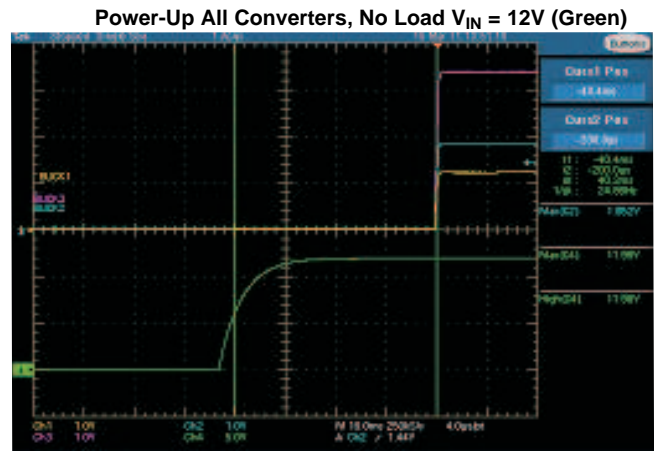


Figure 12.

**TYPICAL CHARACTERISTICS (continued)**

**Power-Up All Converters and PGOOD (Green), No Load**

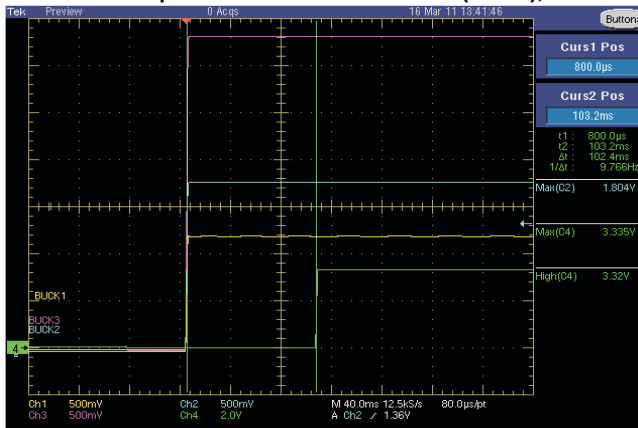


Figure 13.

**Detail of Start-Up 4.7nF Fitted to All Enable Pins**

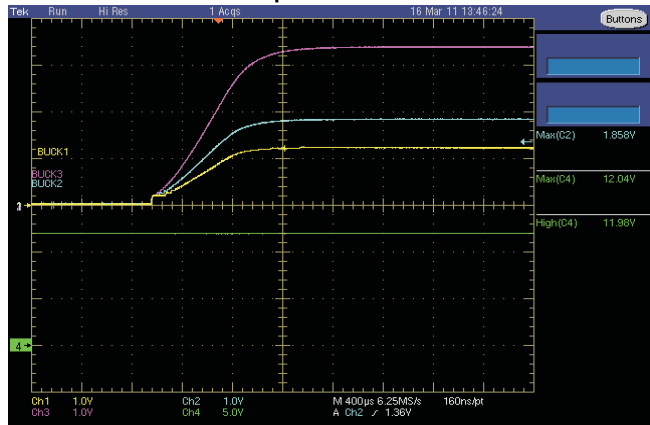


Figure 14.

**Ripple  $T_A = 25^\circ\text{C}$ , Buck1 = 3A, Buck2 = 2A, Buck3 = 2A**

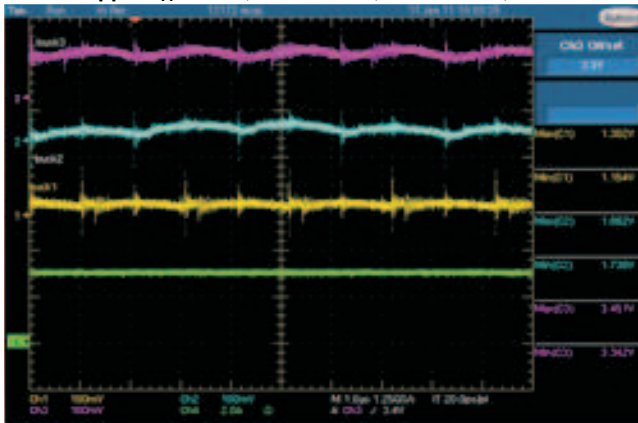


Figure 15.

**Ripple  $T_A = 70^\circ\text{C}$ , Buck1 = 3A, Buck2 = 2A, Buck3 = 2A**

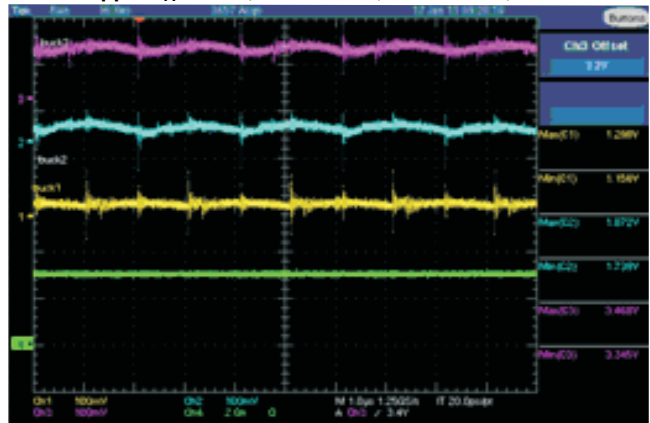


Figure 16.

**Ripple  $T_A = 10^\circ\text{C}$ , Buck1 = 3A, Buck2 = 2A, Buck3 = 2A**

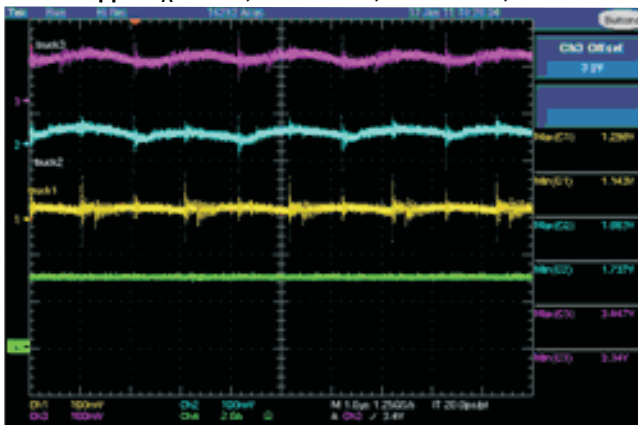


Figure 17.

**Ripple  $T_A = 40^\circ\text{C}$ , Buck1 = 3A, Buck2 = 2A, Buck3 = 2A**

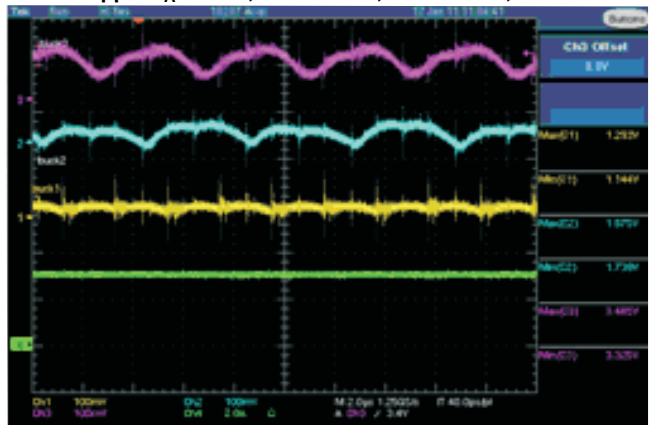


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Transient Response Buck1  
1.2V, 1-3A Step, Co = 22µF, L = 4.7µH, fsw = 500KHz

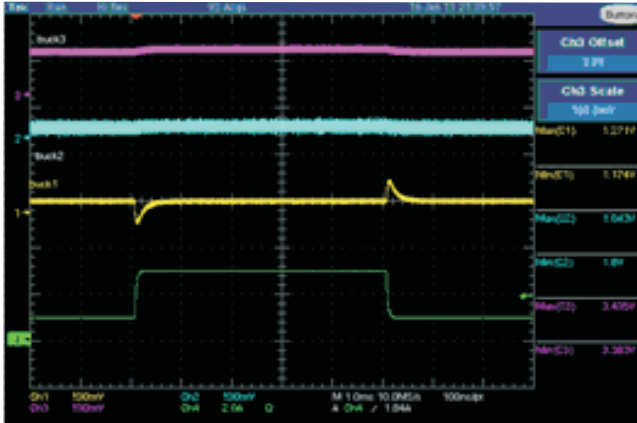


Figure 19.

Transient Response Buck2  
1.8V, 1-2A Step, Co = 22µF, L = 4.7µH, fsw = 500KHz

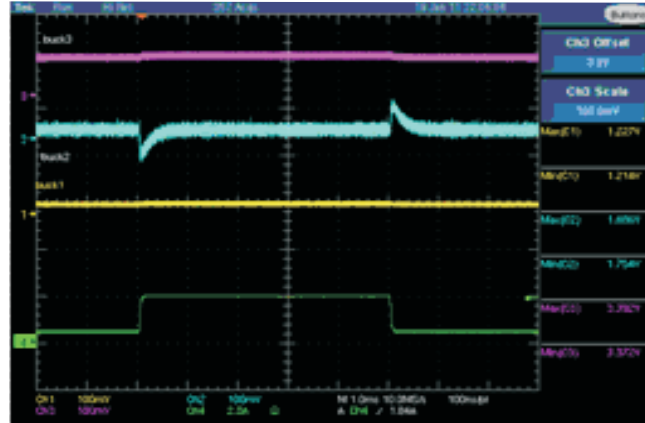


Figure 20.

Buck3 3.3V Efficiency Measured With L = 4.7µH, 20mΩ, fsw = 500kHz

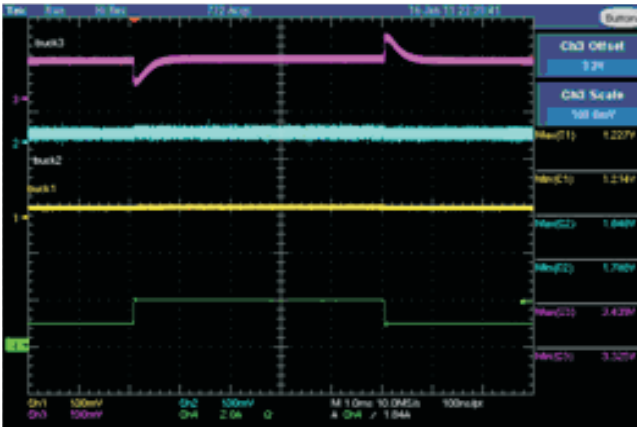


Figure 21.

PFM Operation 1.2V, 1.8V, 3.3V

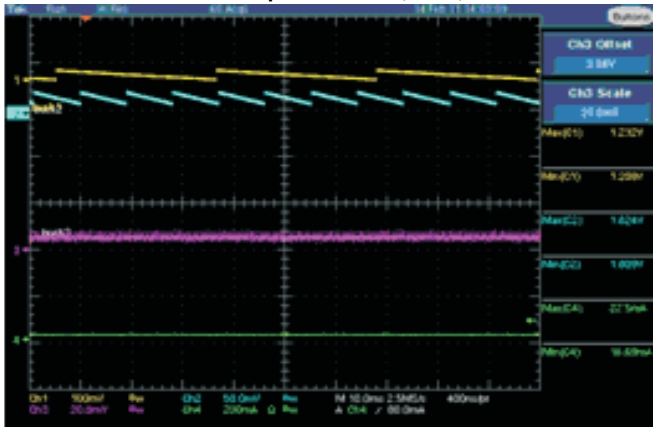


Figure 22.

PFM/PWM Transition (Pin 25 Pulled High)

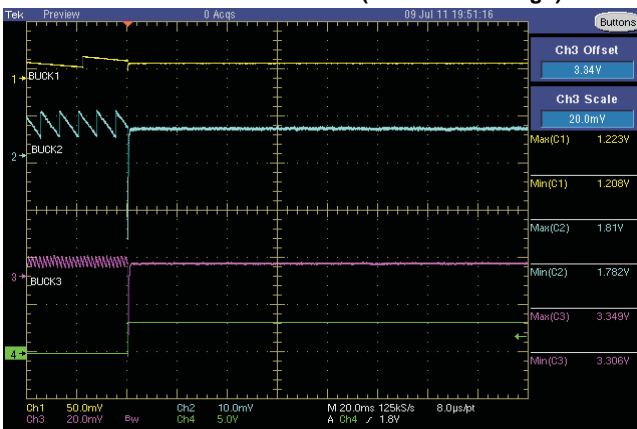


Figure 23.

PFM/PWM Transition (Pin 25 Pulled Low)

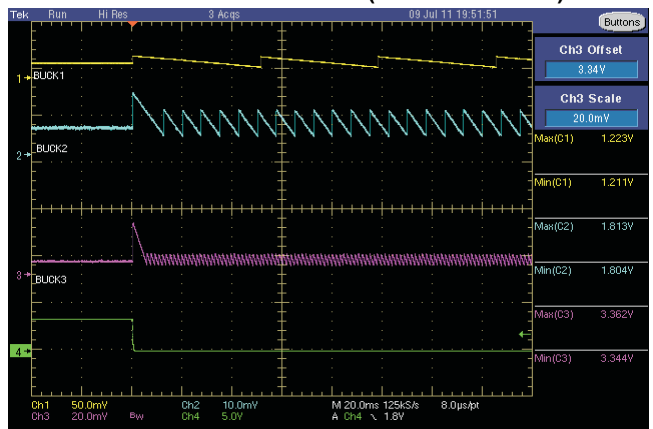


Figure 24.

**TYPICAL CHARACTERISTICS (continued)**

**Buck1 Dynamic Transition from PFM to PWM**  
4.7µH, 44µF, 500 kHz

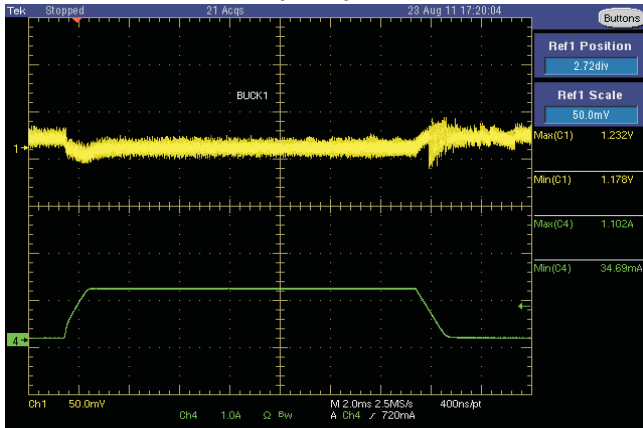


Figure 25.

**Buck2 Dynamic Transition from PFM to PWM**  
4.7µH, 44µF, 500 kHz

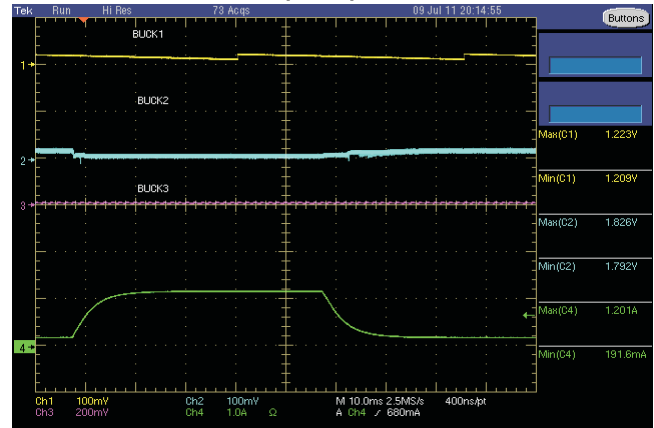


Figure 26.

**Buck3 Dynamic Transition from PFM to PWM**  
4.7µH, 22µF, 500 kHz



Figure 27.

**EVM Layout**

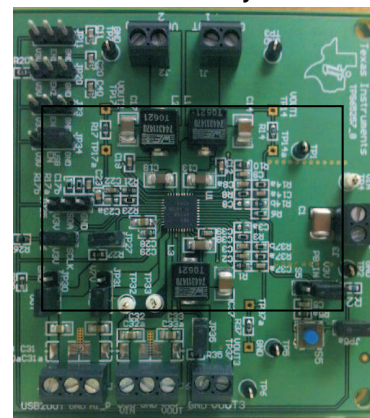


Figure 28.

$T_A = 25^\circ$ ,  $V_{IN} = 12V$ ,  $f_{SW} = 500kHz$   
 $B1 = 3A$ ,  $B2 = 2A$ ,  $B3 = 2A$

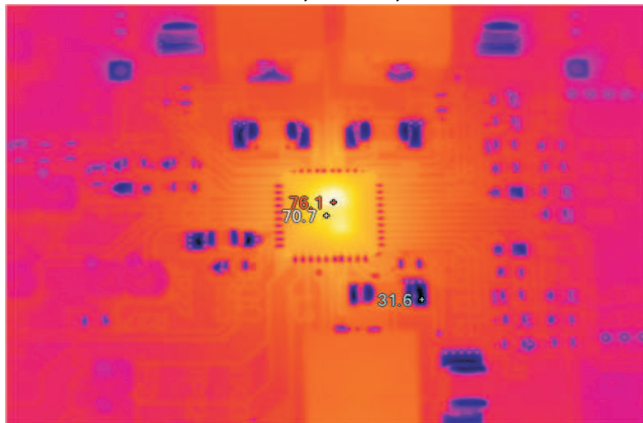


Figure 29.

$T_A = 25^\circ$ ,  $V_{IN} = 5V$ ,  $f_{SW} = 500kHz$   
 $B1 = 3A$ ,  $B2 = 2A$ ,  $B3 = 2A$

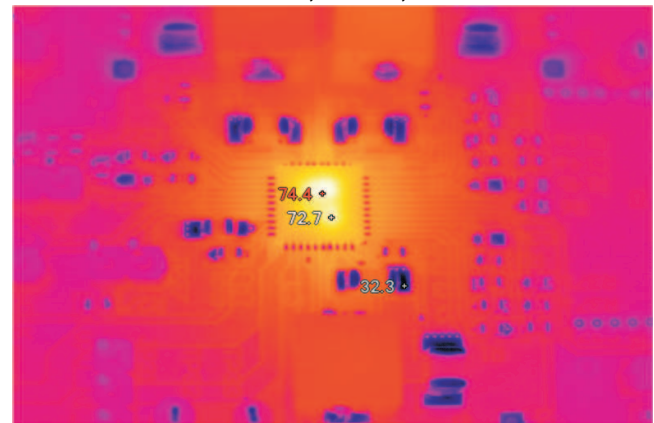


Figure 30.

**TYPICAL CHARACTERISTICS (continued)**

$T_A = 25^\circ$ ,  $V_{IN} = 5V$ ,  $f_{sw} = 1000kHz$   
 $B1 = 3A$ ,  $B2 = 2A$ ,  $B3 = 2A$

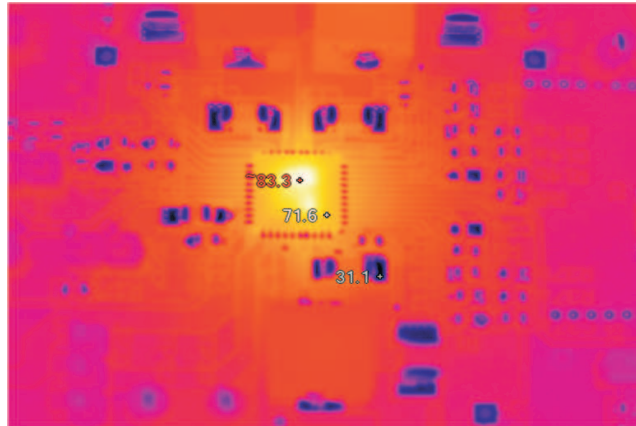


Figure 31.

**DETAILED DESCRIPTION**

**Adjustable Switching Frequency**

To select the internal switching frequency, connect a resistor from ROSC to ground. Figure 32 shows the required resistance for a given switching frequency.

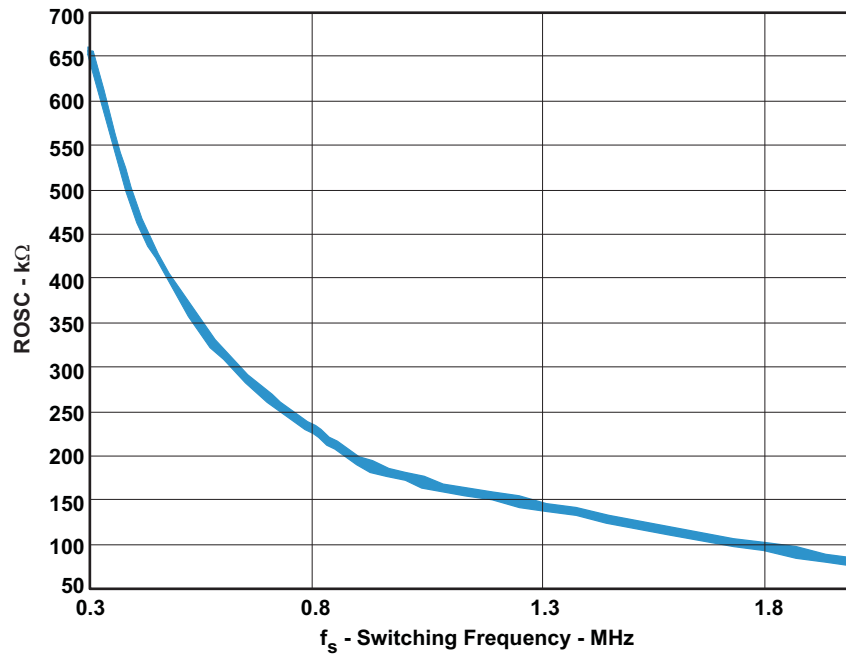


Figure 32. ROSC vs Switching Frequency

$$R_{osc}(k\Omega) = 174 \cdot f_{sw}^{-1.122} \tag{1}$$

## Output Inductor Selection

To calculate the value of the output inductor, use [Equation 2](#).

$$L_o = \frac{V_{in} - V_{out}}{I_o \cdot K_{ind}} \cdot \frac{V_{out}}{V_{in} \cdot f_{sw}} \quad (2)$$

$K_{ind}$  is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In general,  $K_{ind}$  is normally from 0.1 to 0.3 for the majority of applications. A value of 0.1 will improve the efficiency at light load, while a value of 0.3 will provide the lowest possible cost solution. The ripple current is:

$$I_{ripple} = \frac{V_{in} - V_{out}}{L_o} \cdot \frac{V_{out}}{V_{in} \cdot f_{sw}} \quad (3)$$

## Output Capacitor

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements. If a minimum transient specification is required use the following equation:

$$C_o > \frac{\Delta I_{OUT}^2 \cdot L_o}{V_{out} \cdot \Delta V_{out}} \quad (4)$$

The following equation calculates the minimum output capacitance needed to meet the output voltage ripple specification.

$$C_o > \frac{1}{8 \cdot f_{sw}} \cdot \frac{1}{\frac{V_{RIPPLE}}{I_{RIPPLE}}} \quad (5)$$

Where  $f_{sw}$  is the switching frequency,  $V_{RIPPLE}$  is the maximum allowable output voltage ripple, and  $I_{RIPPLE}$  is the inductor ripple current.

## Input Capacitor

A minimum 10- $\mu$ F X7R/X5R ceramic input capacitor is recommended to be added between VIN and GND of each converter. The input capacitor must handle the RMS ripple current shown in the following equation.

$$I_{cirms} = I_{out} \cdot \sqrt{\frac{V_{out}}{V_{in \min}} \cdot \frac{(V_{in \min} - V_{out})}{V_{in \min}}} \quad (6)$$

## Bootstrap Capacitor

The device has two integrated boot regulators and requires a small ceramic capacitor between the BST and LX pins to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.047  $\mu$ F. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

## Soft-Start Time

The device has an internal pull-up current source of 5  $\mu$ A that charges an external soft-start capacitor to implement a slow start time. [Equation 7](#) shows how to select a soft-start capacitor based on an expected slow start time. The voltage reference ( $V_{REF}$ ) is 0.8 V and the soft-start charge current ( $I_{ss}$ ) is 5  $\mu$ A. The soft-start circuit requires 1 nF per around 167  $\mu$ s to be connected at the SS pin. A 0.8-ms soft-start time is implemented for all converters fitting 4.7 nF to the relevant SS pin.

$$T_{ss}(ms) = V_{REF}(V) \cdot \left( \frac{C_{ss}(nF)}{I_{ss}(\mu A)} \right) \quad (7)$$

The Power Good circuit for the bucks has a 10-ms watchdog. Therefore the soft-start time should be lower than this value. It is recommended not to exceed 5 ms.

### Delayed Start-Up

If a delayed start-up is required on any of the buck converters fit a ceramic capacitor to the ENx pins. The delay added is ~1.67 ms per nF connected to the pin. Note that the EN pins have a weak 1-MΩ pull-up to the 3V3 rail.

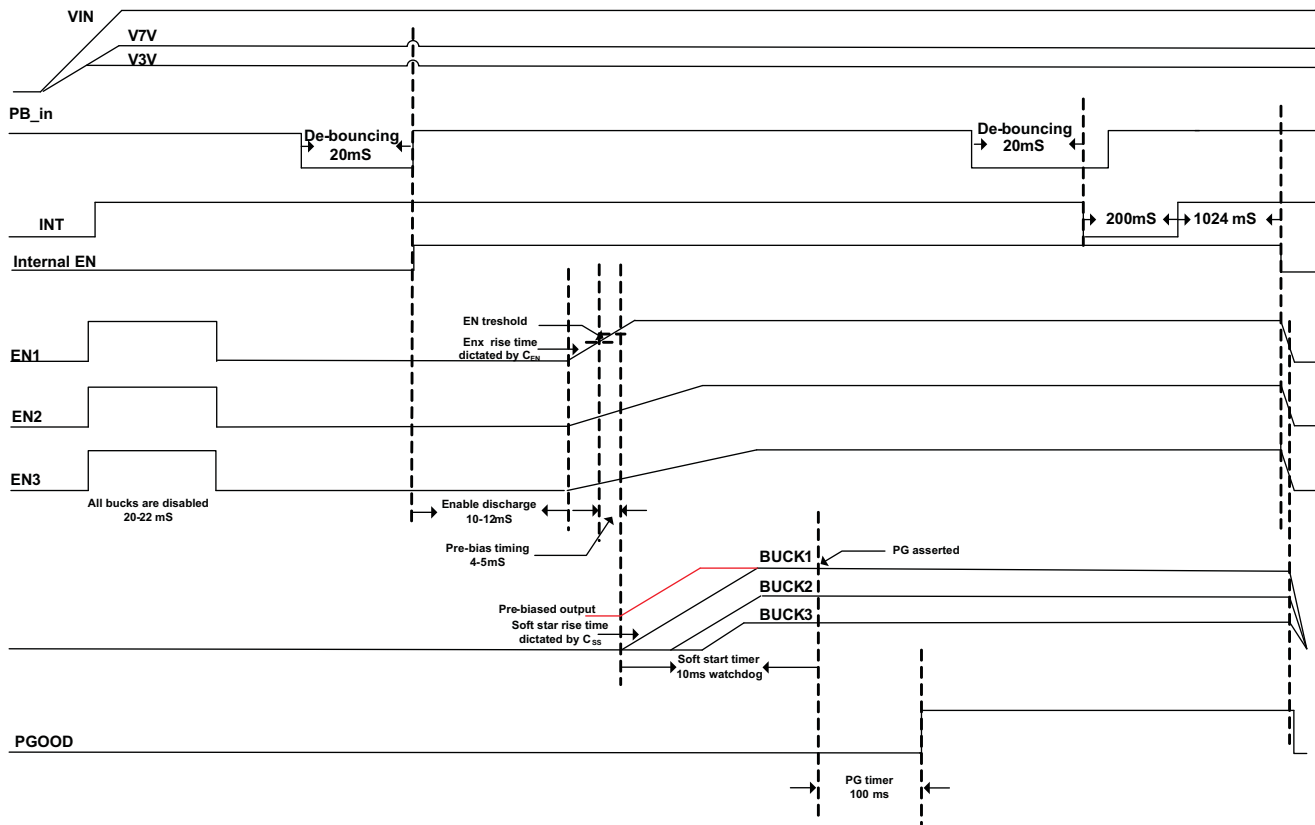


Figure 33. Delayed Start-Up

### Out-of-Phase Operation

In order to reduce input ripple current, Buck1 and Buck2 operate 180° out-of-phase. This enables the system having less input ripple, then to lower component cost, save board space and reduce EMI.

### Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. In order to improve efficiency at light load, start with a value close to 40 kΩ for the R1 resistor and use Equation 8 to calculate R2.

$$R2 = R1 \cdot \left( \frac{0.8V}{V_o - 0.8V} \right) \tag{8}$$



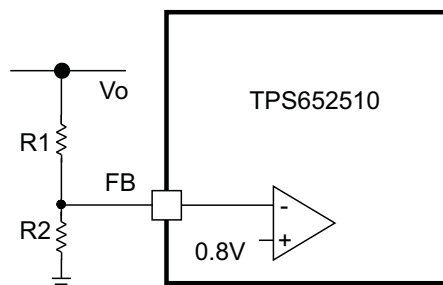


Figure 34. Voltage Divider Circuit

## Loop Compensation

TPS652510 is a current mode control DC/DC converter. The error amplifier is a transconductance amplifier with a  $g_M$  of  $130 \mu A/V$ . A typical compensation circuit could be type II ( $R_C$  and  $C_C$ ) to have a phase margin between  $60^\circ$  and  $90^\circ$ , or type III ( $R_C$  and  $C_C$  and  $C_{ff}$  to improve the converter transient response.  $C_{Roll}$  adds a high frequency pole to attenuate high-frequency noise when needed. It may also prevent noise coupling from other rails if there is possibility of cross coupling in between rails when layout is very compact.

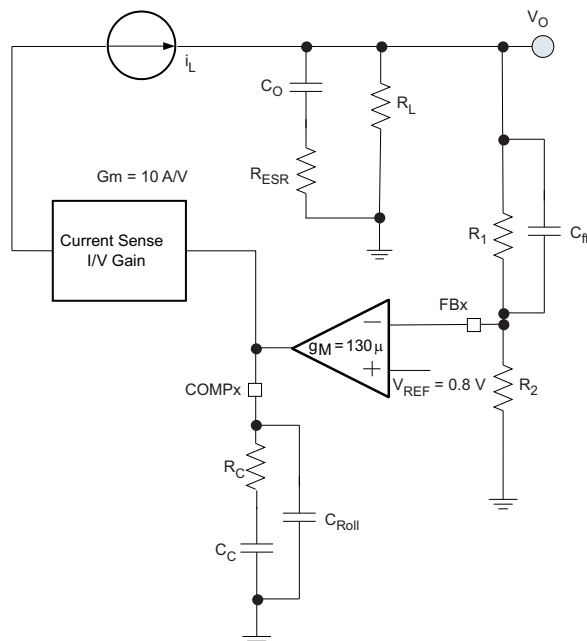


Figure 35. Loop Compensation Scheme

To calculate the external compensation components follow the following steps:

	TYPE II CIRCUIT	TYPE III CIRCUIT
Select switching frequency that is appropriate for application depending on L, C sizes, output ripple, EMI concerns and etc. Switching frequencies around 500 kHz yield best trade off between performance and cost. When using smaller L and C, switching frequency can be increased. To optimize efficiency, switching frequency can be lowered.		Type III circuit recommended for switching frequencies higher than 500 kHz.
Select cross over frequency ( $f_c$ ) to be at least 1/5 to 1/10 of switching frequency ( $f_s$ ).	Suggested $f_c = f_s/10$	Suggested $f_c = f_s/10$
Set and calculate $R_c$ .	$R_c = \frac{2\pi \cdot f_c \cdot V_o \cdot C_o}{g_M \cdot V_{ref} \cdot gm_{ps}}$	$R_c = \frac{2\pi \cdot f_c \cdot C_o}{g_M \cdot gm_{ps}}$
Calculate $C_c$ by placing a compensation zero at or before the converter dominant pole $fp = \frac{1}{C_o \cdot R_L \cdot 2\pi}$	$C_c = \frac{R_L \cdot C_o}{R_c}$	$C_c = \frac{R_L \cdot C_o}{R_c}$
Add $C_{Roll}$ if needed to remove large signal coupling to high impedance CMP node. Make sure that $fp_{Roll} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_{Roll}}$ is at least twice the cross over frequency.	$C_{Roll} = \frac{Re_{sr} \cdot C_o}{R_c}$	$C_{Roll} = \frac{Re_{sr} \cdot C_o}{R_c}$
Calculate $C_{ff}$ compensation zero at low frequency to boost the phase margin at the crossover frequency. Make sure that the zero frequency ( $fz_{ff}$ ) is smaller than equivalent soft-start frequency ( $1/T_{ss}$ ).	NA	$C_{ff} = \frac{1}{2 \cdot \pi \cdot fz_{ff} \cdot R_1}$

## Slope Compensation

The device has a built-in slope compensation ramp. The slope compensation can prevent sub harmonic oscillations in peak current mode control.

## Power Good

The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when both buck converters' outputs are more than 90% of its nominal output voltage.

The default reset time is 100 ms. The polarity of the PGOOD is active high.

### Current Limit Protection

Figure 36 shows the (peak) inductor current limit for Buck 1. The typical limit can be approximated with the following graph.

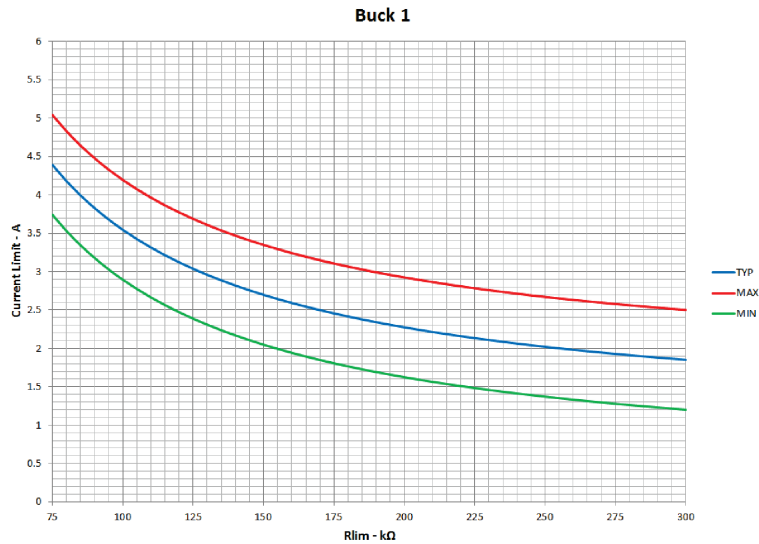


Figure 36. Buck 1

Figure 37 shows the (peak) inductor current limit for Buck 2. The typical limit can be approximated with the following graph.

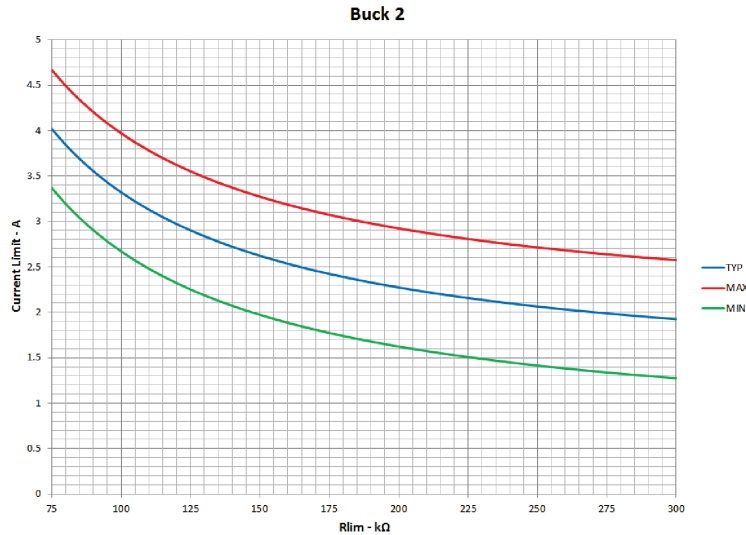


Figure 37. Buck 2

Figure 38 shows the (peak) inductor current limit for Buck 3. The typical limit can be approximated with the following graph.

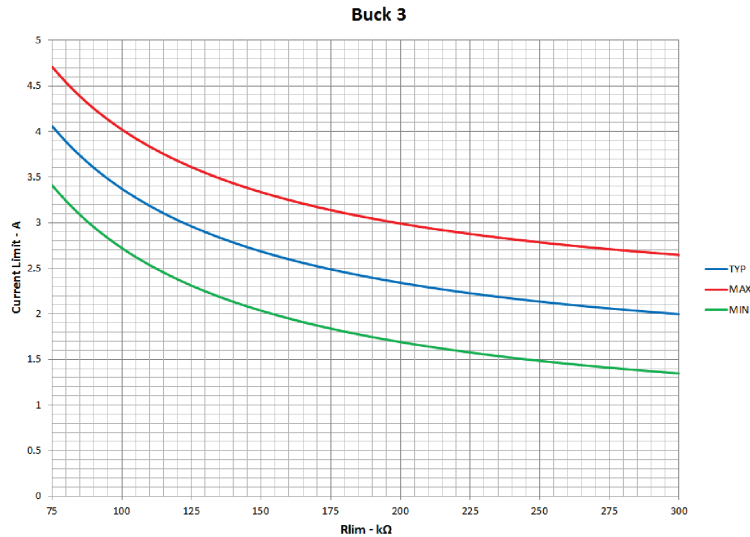


Figure 38. Buck 3

The current limit should be set by using either the TYP or MIN line. If using the TYP line, ensure that limit trips at the MIN line are acceptable for your application. When setting high-side current limit to large current values, ensure that the additional load immediately prior to an overcurrent condition will not cause the switching node voltage to exceed 20 V. Additionally, ensure during worst case operation, with all bucks loaded immediately prior to current limit, the maximum virtual junction temperature of the device does not exceed 125°C.

All converters operate in hiccup mode: Once an over-current lasting more than 10 ms is sensed in any of the converters, they will shut down for 10 ms and then the start-up sequencing will be tried again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case the converter will see another over-current event and shuts-down again repeating the cycle (hiccup) until the failure is cleared.

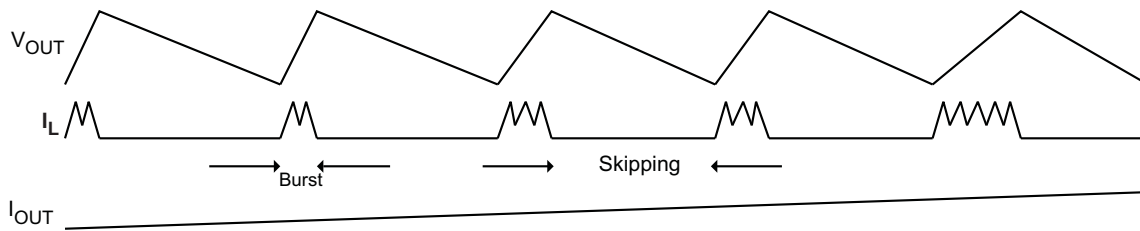
If an overload condition lasts for less than 10 ms, only the relevant converter affected will shut-down and re-start and no global hiccup mode will occur.

### Overvoltage Transient Protection

The device incorporates an overvoltage transient protection (OVP) circuit to minimize voltage overshoot. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVTP threshold which is 109% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold which is 107%, the high side MOSFET is allowed to turn on the next clock cycle.

### Low Power/Pulse Skipping Operation

When a buck synchronous converter operates at light load or standby conditions, the switching losses are the dominant source of power losses. Under these load conditions, TPS652510 uses a pulse skipping modulation technique to reduce the switching losses by keeping the power transistors in the off-state for several switching cycles, while maintaining a regulated output voltage. Figure 39 shows the output voltage and load plus the inductor current.



**Figure 39. Low Power/Pulse Skipping**

During the burst mode, the converter continuously charges up the output capacitor until the output voltage reaches a certain limit threshold. The operation of the converter in this interval is equivalent to the peak inductor current mode control. In each switch period, the main switch is turned on until the inductor current reaches the peak current limit threshold. As the load increases the number of pulses increases to make sure that the output voltage stays within regulation limits. When the load is very light the low power controller has a zero crossing detector to allow the low side mosfet to operate even in light load conditions. The transistor is not disabled at light loads. A zero crossing detection circuit will disable it when inductor current reverses. During the whole process the body diode does not conduct but is used as blocking diode only.

During the skipping interval, the upper and lower transistors are turned off and the converter stays in idle mode. The output capacitors are discharged by the load current until the moment when the output voltage drops to a low threshold.

The choice of output filter will influence the performance of the low power circuit. The maximum ripple during low power mode can be calculated as:

$$V_{OUT\_RIPPLE} = \frac{K_{RIP} T_S}{C_{OUT}} \quad (9)$$

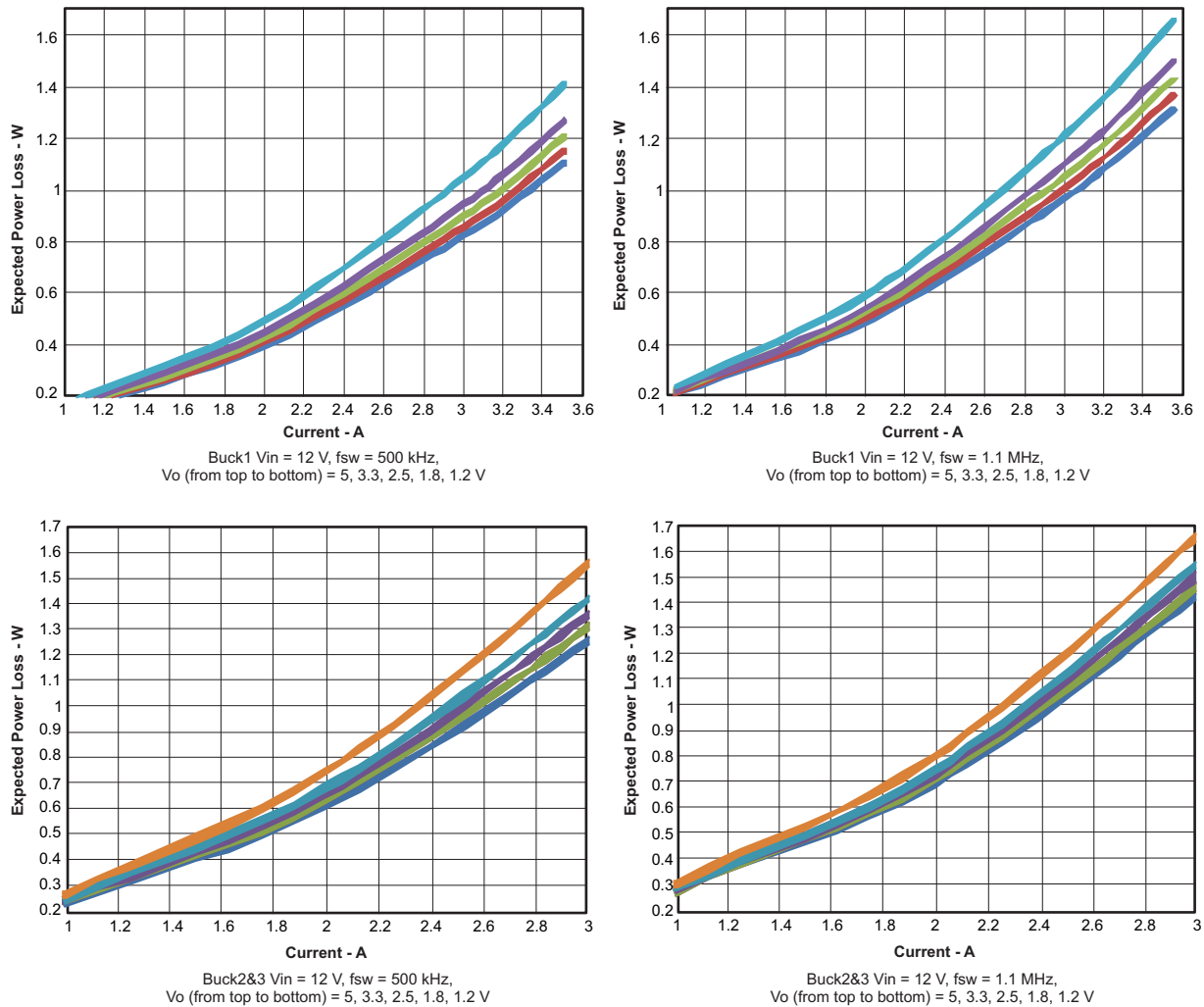
Where  $K_{RIP}$  is 1.4 for Buck1 and 0.7 for Buck2 and Buck3.  $T_S$  can be calculated as:

$$T_S = \frac{0.35}{\left[ \left( \frac{V_{IN} - V_{OUT}}{L} \right) V_{OUT} \right] V_{IN}} \quad (10)$$

## Power Dissipation

The total power dissipation inside TPS652510 should not to exceed the maximum allowable junction temperature of 125°C. The maximum allowable power dissipation is a function of the thermal resistance of the package ( $R_{JA}$ ) and ambient temperature. To calculate the temperature inside the device under continuous loading use the following procedure:

1. Define the set voltage for each converter.
2. Define the continuous loading on each converter. Make sure do not exceed the converter maximum loading.
3. Determine from the graphs below the expected losses in watts per converter inside the device. The losses depend on the input supply, the selected switching frequency, the output voltage and the converter chosen.



**Figure 40. Power Dissipation Curves**

4. To calculate the maximum temperature inside the IC use the following formula:

$$T_{HOT\_SPOT} = T_A + P_{DIS} \times \Theta_{JA} \tag{11}$$

Where:

$T_A$  is the ambient temperature

$P_{DIS}$  is the sum of losses in all converters

$\Theta_{JA}$  is the junction to ambient thermal impedance of the device and it is heavily dependant on board layout

### Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

### 3.3-V and 6.5 LDO Regulators

The following ceramic capacitor (X7R/X5R) should be connected as close as possible to the described pins:

- 4.7  $\mu$ F to 10  $\mu$ F for V7V pin 28
- 3.3  $\mu$ F to 10  $\mu$ F for V3V pin 29

## Layout Recommendation

Layout is a critical portion of PMIC designs.

- Place tracing for output voltage and LX on the top layer and an inner power plane for VIN.
- Fit also on the top layer connections for the remaining pins of the PMIC and a large top side area filled with ground.
- The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS652510 device to provide a thermal path from the PowerPad land to ground.
- For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- The compensation should be as close as possible to the CMPx pins. The CMPx and ROOSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace.

## REVISION HISTORY

Changes from Revision A (September 2011) to Revision B	Page
• Changed Functional Block Diagram image .....	3
• Changed Terminal Function descriptions for V7V and V3V .....	5
• Added F_PWM to Absolute Maximum Ratings .....	6
• Changed INPUT SUPPLY UVLO AND INTERNAL SUPPLY VOLTAGE parameters .....	7
• Added $I_{3V}$ and $I_{7V}$ limits .....	7
• Changed $V_{IH}$ and $V_{IL}$ limits .....	7
• Changed FEEDBACK, REGULATION, OUTPUT STAGE parameters .....	7
• Changed <a href="#">Equation 5</a> .....	15
• Changed Type III Circuit description for first row .....	18
• Changed .....	18
• Changed Current Limit Protection section .....	19
• Changed <a href="#">Figure 36</a> .....	19
• Changed <a href="#">Figure 37</a> .....	19
• Changed <a href="#">Figure 38</a> .....	20
• Changed current limit description .....	20
• Changed <a href="#">Figure 40</a> .....	22
• Changed 3.3-V and 6.5 LDO Regulators section .....	22



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS652510RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 652510	<a href="#">Samples</a>
TPS652510RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 652510	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS652510RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS652510RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

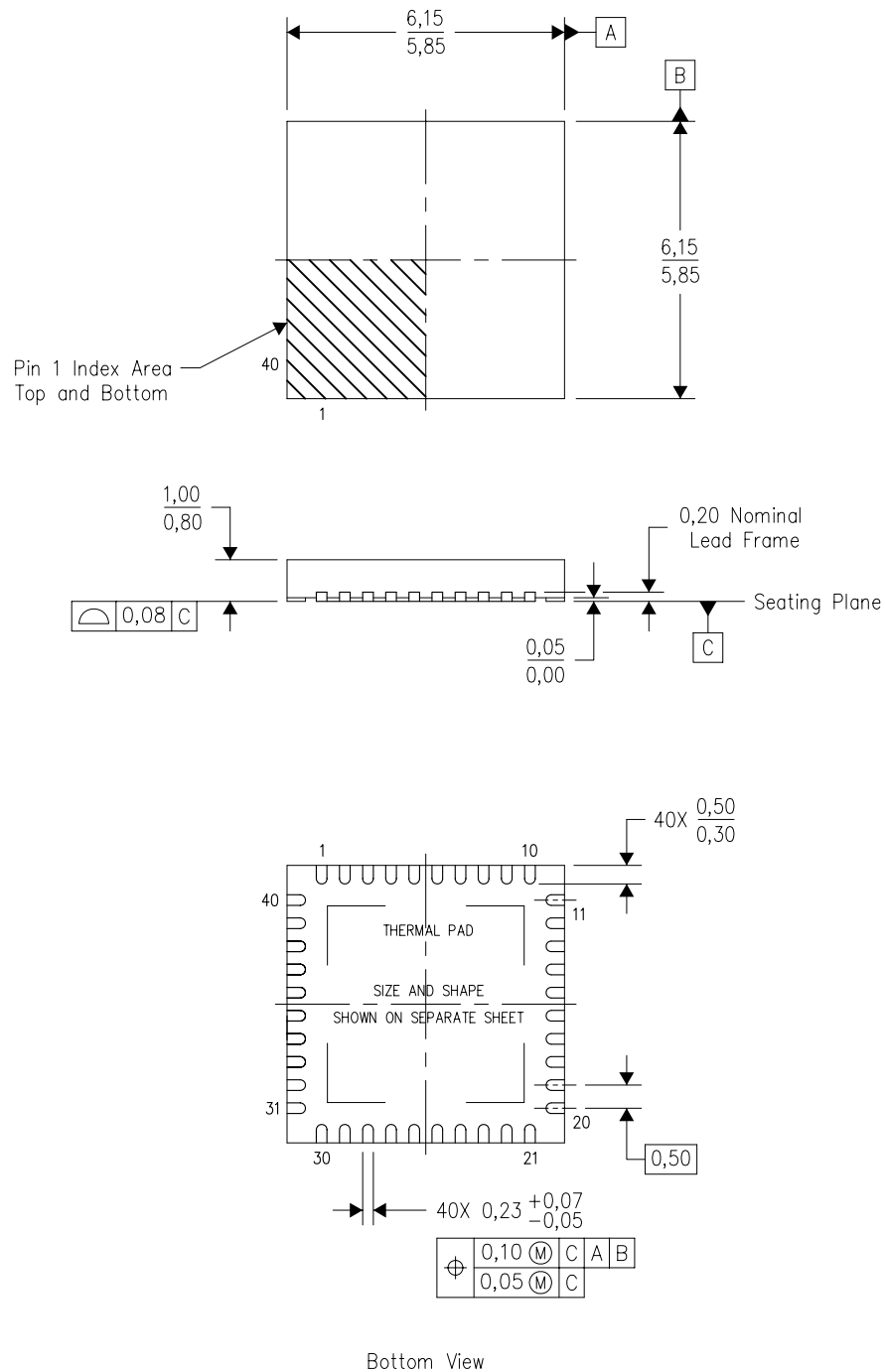
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS652510RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS652510RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4204276/E 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Package complies to JEDEC MO-220 variation VJJD-2.

## THERMAL PAD MECHANICAL DATA

RHA (S-PVQFN-N40)

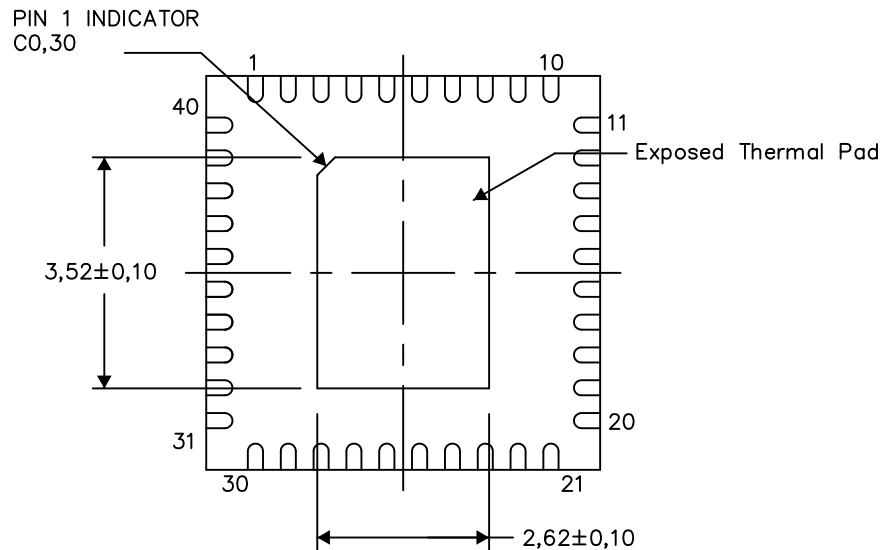
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

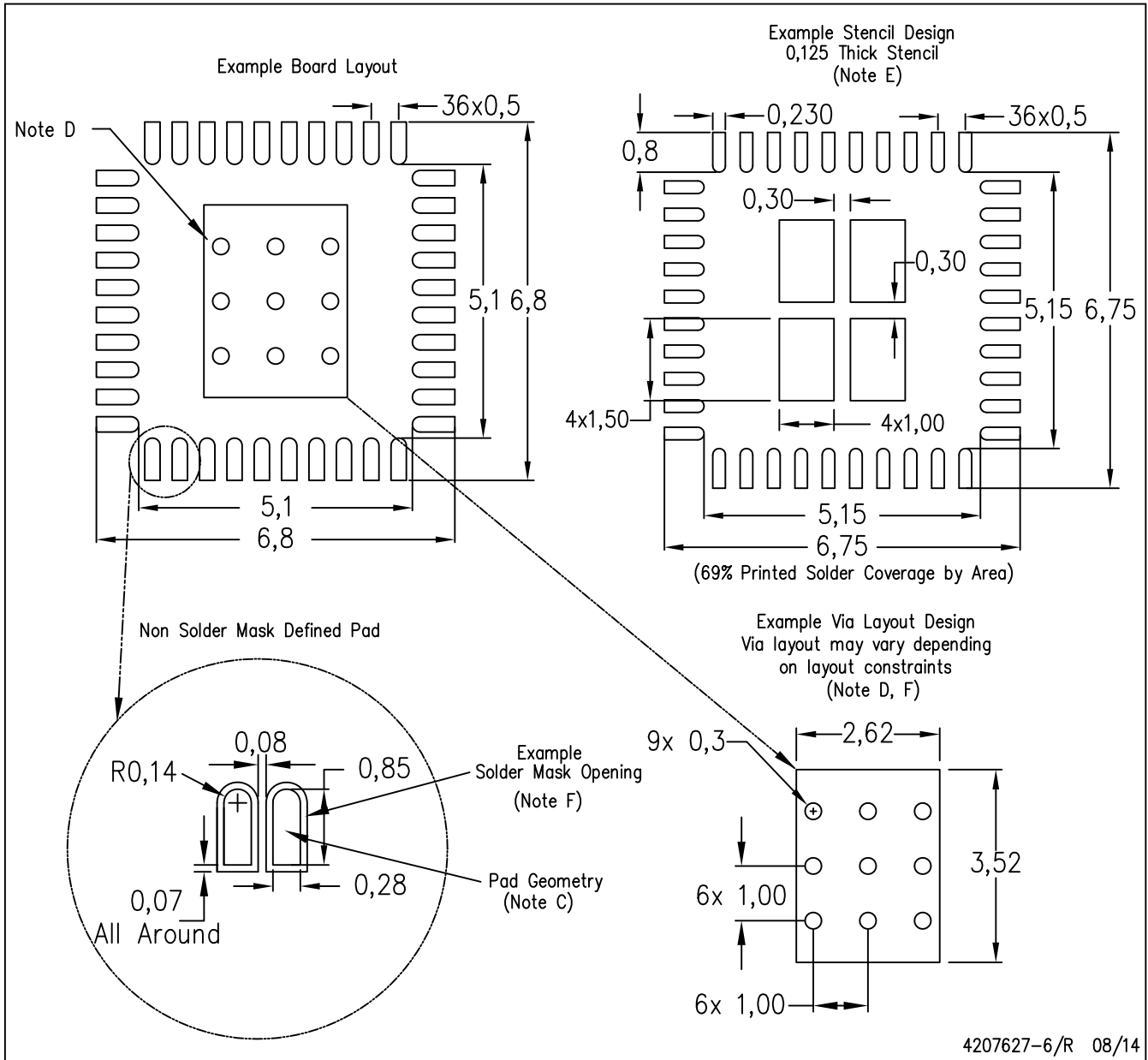
Exposed Thermal Pad Dimensions

4206355-9/X 08/14

NOTES: A. All linear dimensions are in millimeters

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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