Semiconductor Corporation

CS8401 CS8402

T-75-45-05

Digital Audio Interface Transmitter

Features

- Monolithic Digital Audio Interface Transmitter
- Supports: AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 Professional and Consumer Formats
- Host Mode and Stand Alone Modes
- Generates CRC Codes and Parity Bits
- On-Chip RS422 Line Driver
- Configurable Buffer Memory (CS8401)

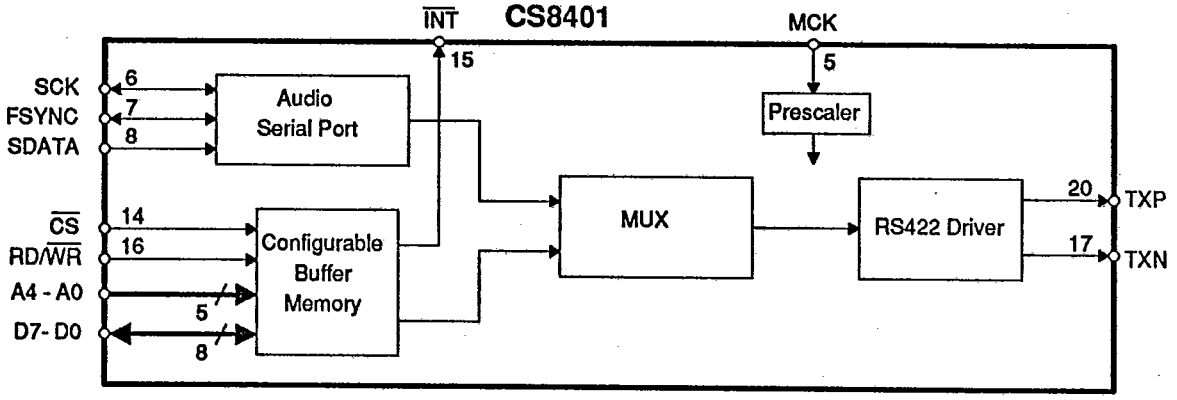
General Description

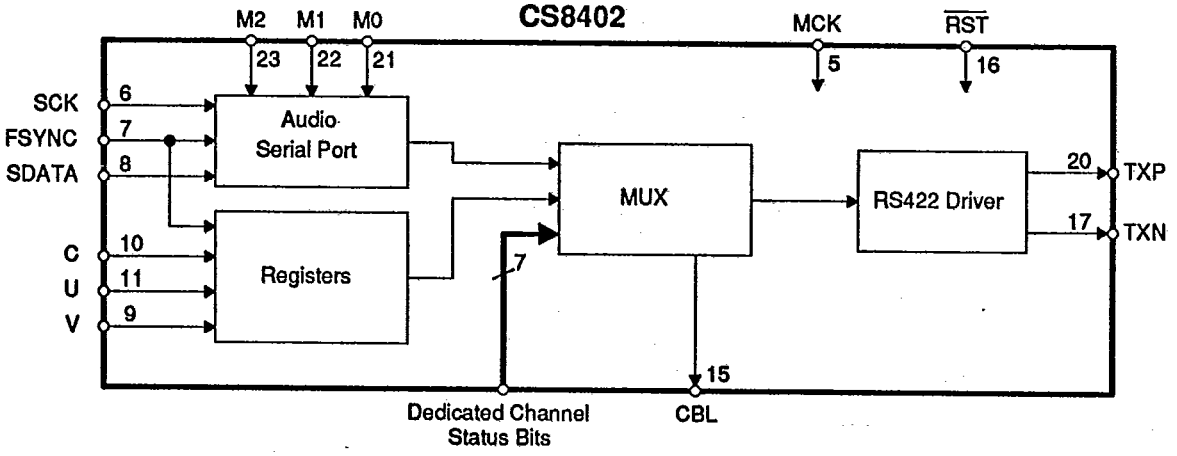
The CS8401/2 are monolithic CMOS devices which encode and transmit audio data according to the AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 interface standards. The CS8401/2 accept audio and digital data, which is then multiplexed, encoded and driven onto a cable. The audio serial port is double buffered and capable of supporting a wide variety of formats.

The CS8401 has a configurable internal buffer memory, loaded via a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

The CS8402 multiplexes the channel, user, and validity data directly from serial input pins with dedicated input pins for the most important channel status bits.

ORDERING INFORMATION: Page 39





Preliminary Product Information This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ABSOLUTE MAXIMUM RATINGS (GND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supply		VD+		6.0	V
Input Current, Any Pin Except Supply	Note 1	I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	VD+	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(GND = 0V; all voltages with respect to ground)

Parameter			Symbol	Min	Typ	Max	Units
DC Voltage			VD+	4.5	5.0	5.5	V
Supply Current		Note 2	I_{DD}		1.5	5	mA
Ambient Operating Temperature:	CS8401/2-CP or -CS	Note 3	T_A	0	25	70	°C
	CS8401/2-IP or -IS			-40		85	°C
Power Consumption		Note 2	P_D		7.5	25	mW

Notes: 2. Drivers open (unloaded). The majority of power is used in the load connected to the drivers.
3. The '-CP' and '-CS' parts are specified to operate over 0 to 70 °C but are tested at 25 °C only. The '-IP' and '-IS' parts are tested over the full -40 to 85 °C temperature range.

DIGITAL CHARACTERISTICS

(T_A = 25 °C for suffixes 'CP' & 'CS', T_A = -40 to 85 °C for 'IP' & 'IS'; VD+ = 5V ± 10%)

Parameter			Symbol	Min	Typ	Max	Units
High-Level Input Voltage			V_{IH}	2.0		V_{DD}+0.3	V
Low-Level Input Voltage			V_{IL}	-0.3		+0.8	V
High-Level Output Voltage	(I_O = 200µA)		V_{OH}	V_{DD}-1.0			V
Low-Level Output Voltage	(I_O = 3.2mA)		V_{OL}			0.4	V
Input Leakage Current				I_{in}		1.0	10µA
Master Clock Frequency:	CS8401	Note 4	MCK			22	MHz
	CS8402	Note 4				7.1	MHz
Master Clock Duty Cycle	CS8401/2			40		60	%

Notes: 4. MCK for the CS8401 must be 128, 192, 256, or 384× the input word rate based on M0 and M1 in control register 2. MCK for the CS8402 must be 128× the input word rate.

Specifications are subject to change without notice.

DIGITAL CHARACTERISTICS - RS422 DRIVERS

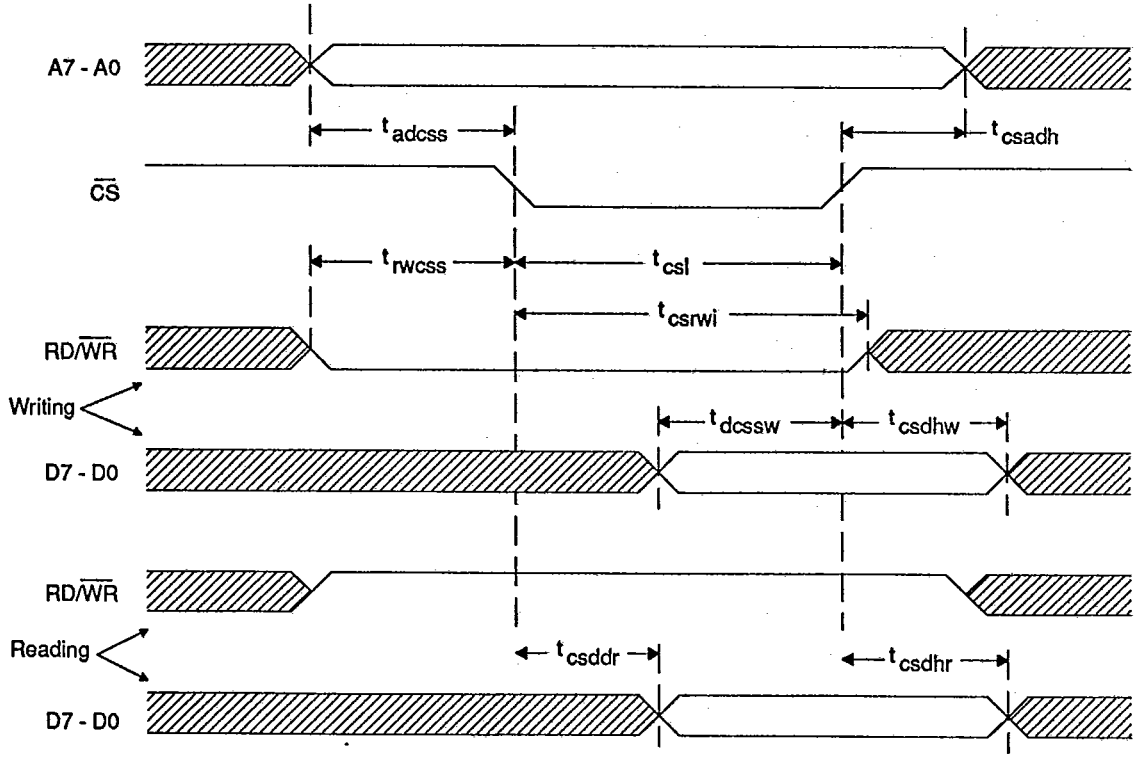
(TXP, TXN pins only; VD+ = 5V ±10%)

Parameter		Symbol	Min	Typ	Max	Units
Output High Voltage	I_{OH} = -30 mA	V_{OH}	VD+- 0.7	VD+ - 0.4		V
Output Low Voltage	I_{OL} = 30 mA	V_{OL}		0.4	0.7	V

SWITCHING CHARACTERISTICS - CS8401 PARALLEL PORT

(T_A = 25 °C for suffixes '-CP' and '-CS'; T_A = -40 to 85 °C for suffixes '-IP' and '-IS')

Parameter		Symbol	Min	Typ	Max	Units
ADDRESS valid to $\overline{CS}$ low		t_{adcss}	0			ns
$\overline{CS}$ high to ADDRESS invalid		t_{csadh}	15			ns
RD/$\overline{WR}$ valid to $\overline{CS}$ low		t_{rwcss}	5			ns
$\overline{CS}$ low to RD/$\overline{WR}$ invalid		t_{csrwi}	35			ns
$\overline{CS}$ low		t_{csl}	35			ns
DATA valid to $\overline{CS}$ rising	RD/$\overline{WR}$ low (writing)	t_{dcssw}	20			ns
$\overline{CS}$ high to DATA invalid	RD/$\overline{WR}$ low (writing)	t_{csdhw}	15			ns
$\overline{CS}$ falling to DATA valid	RD/$\overline{WR}$ high (reading)	t_{csddr}			35	ns
$\overline{CS}$ rising to DATA invalid	RD/$\overline{WR}$ high (reading)	t_{csdhr}	0			ns



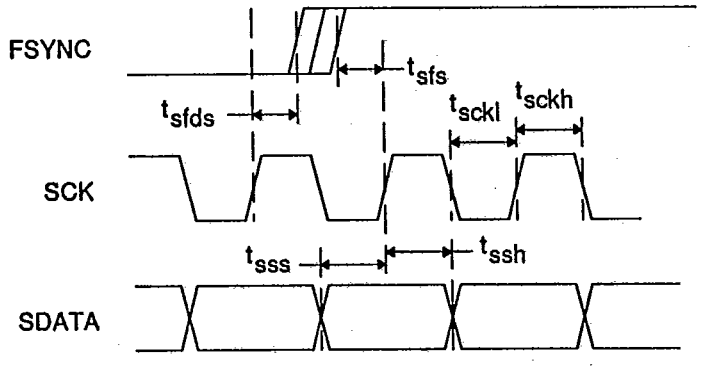
CS8401 Parallel Port Timing

SWITCHING CHARACTERISTICS - SERIAL PORTS

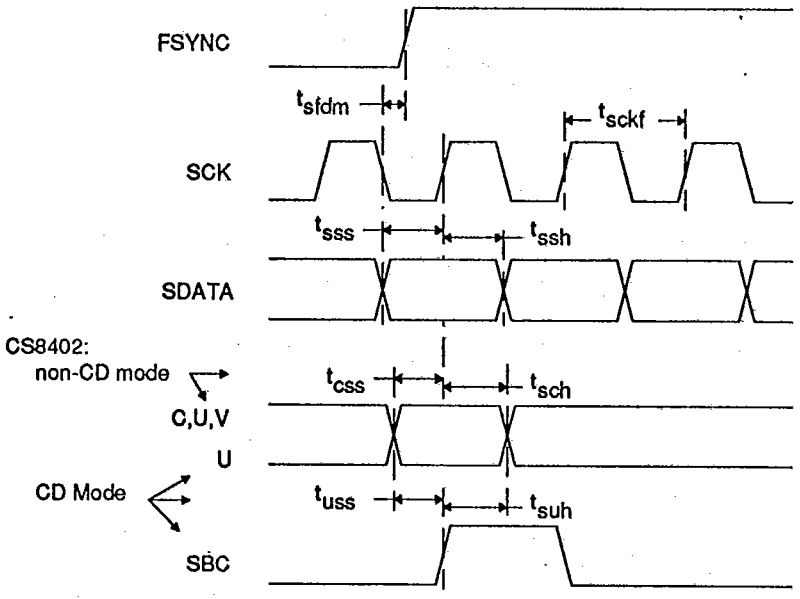
(T_A = 25 °C for suffixes '-CP' and '-CS'; T_A = -40 to 85 °C for suffixes '-IP' and '-IS';
Inputs: Logic 0 = GND, logic 1 = VD+; C_L = 20 pF)

Parameter			Symbol	Min	Typ	Max	Units
SCK Frequency	Master Mode	Notes 5,6	t_{sckf}		IWRx64		Hz
	Slave Mode	Note 6				15	MHz
SCK falling to FSYNC delay	Master Mode	Notes 6,7	t_{sfdm}	-10		15	ns
SCK Pulse Width Low	Slave Mode	Note 6	t_{sckl}	25			ns
SCK Pulse Width High	Slave Mode	Note 6	t_{sckh}	25			ns
SCK rising to FSYNC edge delay	Slave Mode	Notes 6,7	t_{sfds}	20			ns
SCK rising to FSYNC edge setup	Slave Mode	Notes 6,7	t_{sfs}	20			ns
SDATA valid to SCK rising setup		Note 7	t_{sss}	20			ns
SCK rising to SDATA hold time		Note 7	t_{ssh}	20			ns
C, U, V valid to SCK rising setup	CS8402 non-CD Mode	Notes, 7,8	t_{css}	0			ns
SCK rising to C, U, V hold time	CS8402 non-CD mode	Notes 7, 8	t_{scs}	50			ns
U valid to SBF rising setup	CS8402, CD mode	Note 8	t_{uss}	0			ns
SBF rising to U hold time	CS8402, CD mode	Note 8	t_{suh}	80			ns

Notes:
5. The input word rate, IWR, refers to the frequency at which audio input samples are input to the part. (A stereo pair is two audio samples.) Therefore, in Master mode, there are always 32 SCK periods in one audio sample.
6. Master mode is defined as SCK and FSYNC being outputs. In Slave mode they are inputs. In the CS8401, control reg. 3 bit 1, MSTR, selects master. In the CS8402, only format 0 is master.
7. The table above assumes data is output on the falling edge and latched on the rising edge. In both parts the edge is selectable. The table is defined for the CS8401 with control reg. 3 bit 0, SCED, set to one, and for the CS8402 in formats 4 through 7. For the other formats, the table and figure edges must be reversed (ie. "rising" to "falling" and vice versa).
8. The diagrams show SBC rising coincedent with the first rising edge of SCK after FSYNC transitions. This is true for all modes except FSF0 & 1 both equal 1 in the CS8401, and format 4 in the CS8402. In these modes SBC is delayed one full SCK period.



Serial Input Timing - Slave Mode



Serial Input Timing - Master Mode & C, U, V Port

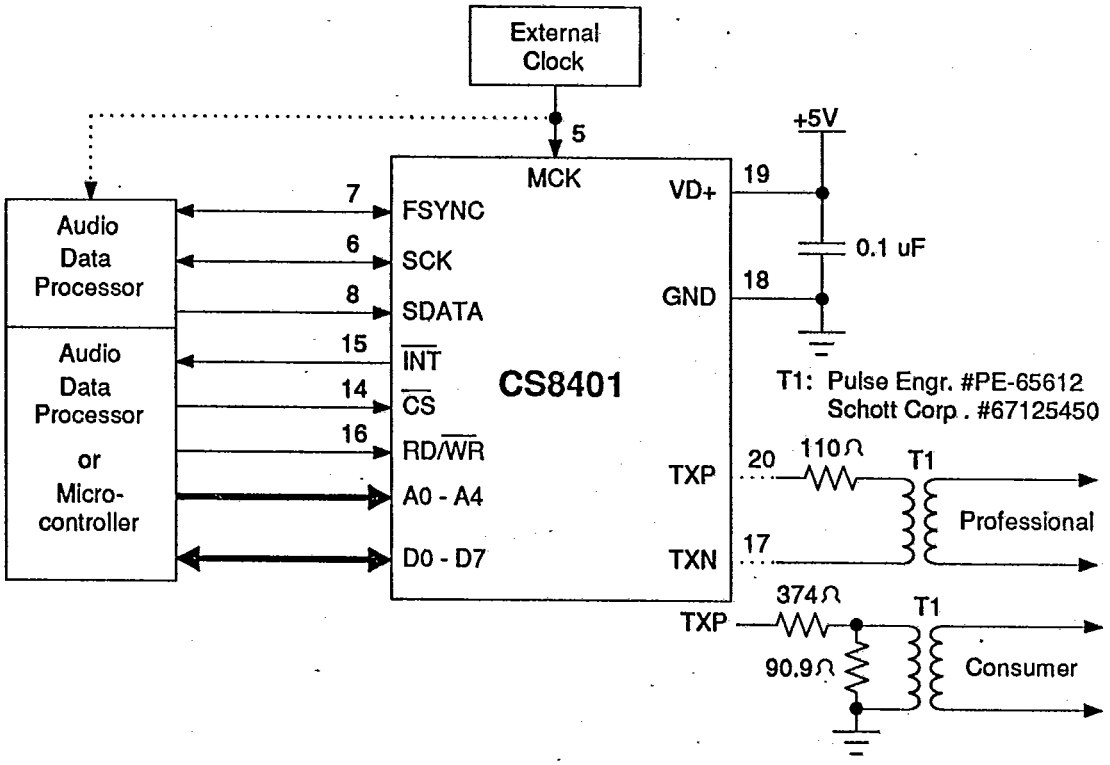


Figure 1. CS8401 Typical Connection Diagram

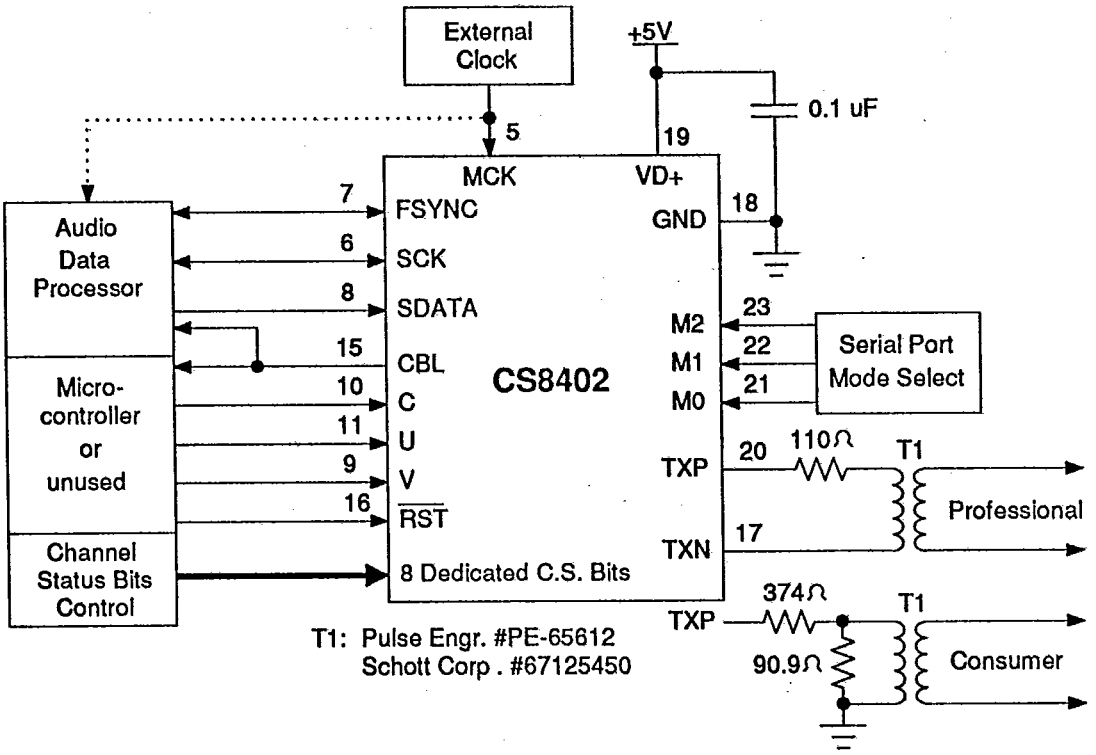


Figure 2. CS8402 Professional & Consumer Modes Typical Connection Diagram

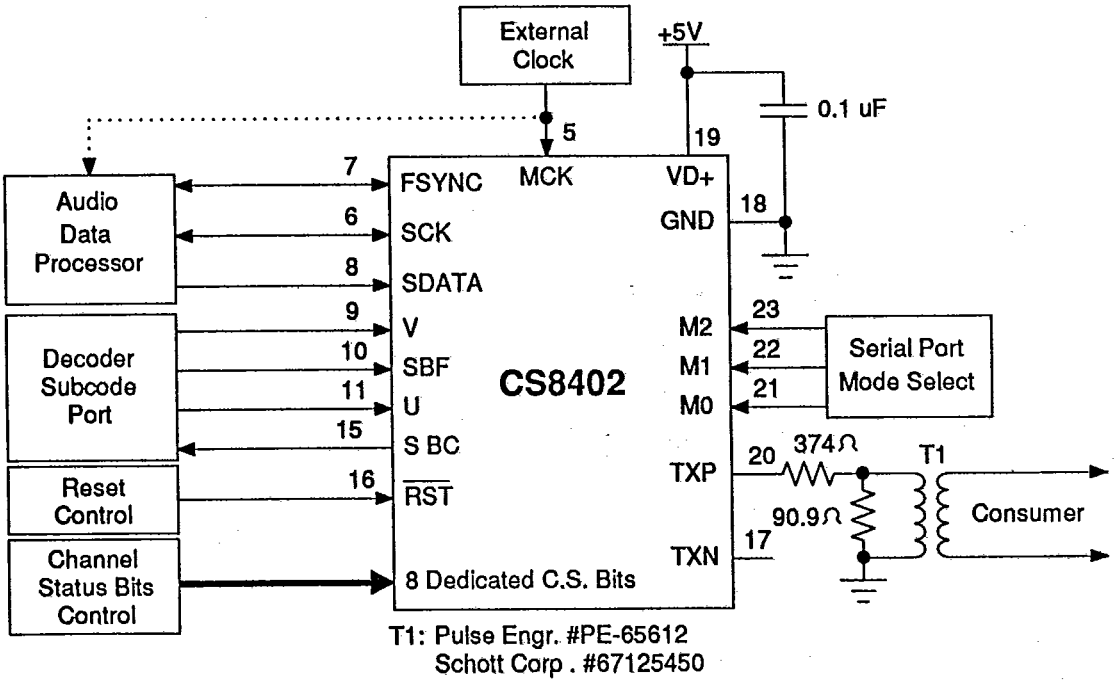


Figure 3. Consumer CD Submode Typical Connection Diagram

GENERAL DESCRIPTION

The CS8401/2 are monolithic CMOS circuits that encode and transmit audio and digital data according to the AES/EBU, IEC 958, S/PDIF, and EIAJ CP-340 interface standards. Both chips accept audio and control data separately; multiplex and biphase-mark encode the data internally; and drive it, directly or through a transformer, to a transmission line. The CS8401 is fully software programmable through a parallel port and contains buffer memory for control data, while the CS8402 has dedicated pins for the most important control bits and a serial input port for the C, U, and V bits. This document is organized as follows:

Familiarity with the AES/EBU and IEC 958 specifications are assumed throughout this data sheet. Many terms such as channel status, user data, auxiliary data, professional mode, etc. are not defined. Appendix A provides an overview of the AES/EBU and IEC 958 specifications and is included for clarity; however, it is not meant to be a complete reference, and the complete standards should be obtained from the Audio Engineering Society or ANSI for the AES/EBU document, and the International Electrotechnical Commission for the IEC document.

Line Drivers

The RS422 line drivers for both the CS8401 and CS8402 are low skew, low impedance, differential outputs capable of driving 110 Ohm transmission lines with an 8 volt peak-to-peak signal. To prevent possible short circuits, both drivers are set to ground when no master clock (MCK) is provided. They can also be disabled by resetting the device ($\overline{RST}$ = low). Appendix B contains more information on the line drivers. Due to the drive capabilities of the parts, a 0.1 µF capacitor, with short leads, should be placed as close as possible to the VD+ and GND pins.

CS8401 DESCRIPTION

The CS8401 accepts 16- to 24-bit audio samples through a configurable serial port, and channel status, user, and auxiliary data through an 8-bit parallel port. The parallel port allows access to 32 bytes of internal memory which is used to store control information and buffer channel status, user, and auxiliary data. This data is multiplexed with the audio data from the serial port, the parity bit is generated, and the bit stream is biphase-mark encoded and driven through an RS422 line driver. A block diagram of the CS8401 is shown in figure 4. In accordance with the professional definition of channel status, the local sample address (channel status, C.S., bytes 14-17), the reliability flag (C.S. byte 22), and the CRCC code (C.S. byte 23) can be internally generated.

Parallel Port

The parallel port accesses one status register, three control registers, and 28 bytes of dual port buffer memory. The address bus, and RD/$\overline{WR}$ line must be valid when $\overline{CS}$ goes low. If RD/$\overline{WR}$ is low, the value on the data bus will be written into the buffer memory at the specified address. If RD/$\overline{WR}$ is high, the value in the buffer memory, at the specified address, is placed on the data bus. The detailed timing for reading and writing the CS8401 can be found in the Digital Switching Characteristics table. The memory space is allocated as shown in figure 5. There are three defined buffer memory modes selectable by two bits in control register 2.

Status and Control Registers

Upon power up the CS8401 control registers contain all zeros. Therefore, the part is initially in reset and is muted. One's must be written to

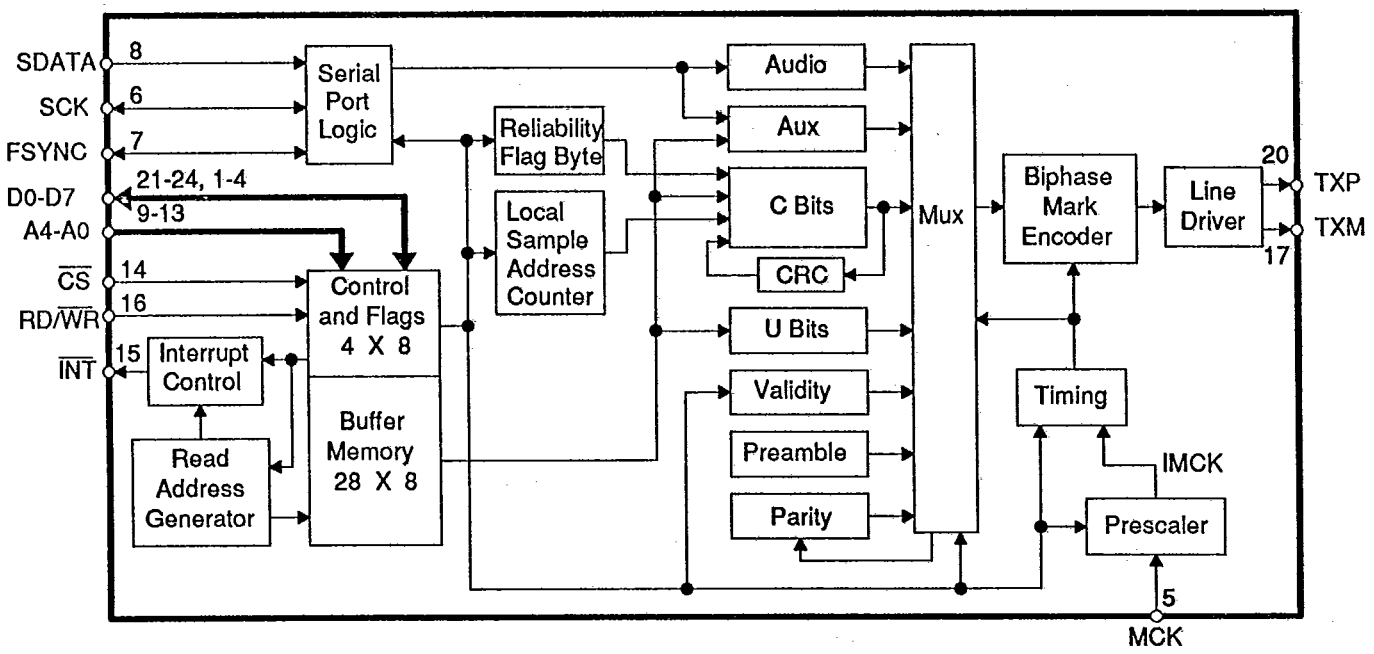


Figure 4. CS8401 Block Diagram

control register 2, bits $\overline{RST}$ and $\overline{MUTE}$, before the part will transmit data.

The first register, shown in figure 6, is the status register in which only three bits are valid. The lower three bits contain flags indicating the position of the transmit pointer in the buffer memory. These flags may be used to avoid contention between the transmit pointer reading the data and the user updating the buffer memory. Besides indicating the byte location being transmitted, the flags indicate the block of memory the part is currently addressing, thereby telling the user which block is free to be written to. Each flag has a corresponding mask bit (control register 1) which, when set, allows a transition on the flag to generate a pulse on the interrupt pin. Flag 0 and flag 1 cause interrupts on both edges whereas flag 2 causes an interrupt only on the rising edge. Timing and further explanation of the flags can be found in the buffer memory section.

In addition to the flag mask bits previously described, control register 1 contains two other bits that are only valid in professional mode: LSAE, local sample address enable, and RLFR, reliability flag byte enable. Professional/consumer mode is determined by bit 0 of byte 0 in the channel status block. If in consumer mode, LSAE and RLFR must be set to zero. The local sample address counter is reset and disabled when LSAE is low. When high, the contents of the counter are transmitted during channel status bytes 14 to 17, and the counter is incremented at the end of each block. When RLFR is high, bits 5 and 7 of channel status byte 22, the reliability flag byte, are set high.

Control register 2, shown in figure 8, contains various system level functions. The two most significant bits, M1 and M0, select the frequency at the MCK pin as shown in Table 1. As an example, if the audio sample frequency is 44.1 kHz and M0 and M1 are both zero, MCK would then be 128× the audio sample rate or 5.6448 MHz. The next bit (5) in control register 2, V, indicates the validity of the current audio sample. B1 and B0 select one of three modes for the buffer memory. The different modes are shown in figure 5 and the bit combinations in table 2. More information on the different modes can be found in the buffer memory section. Bit 2, CRCE, is the channel status CRCC enable and should only be used in professional mode. When CRCE is high, the channel status data cyclic redundancy check characters are

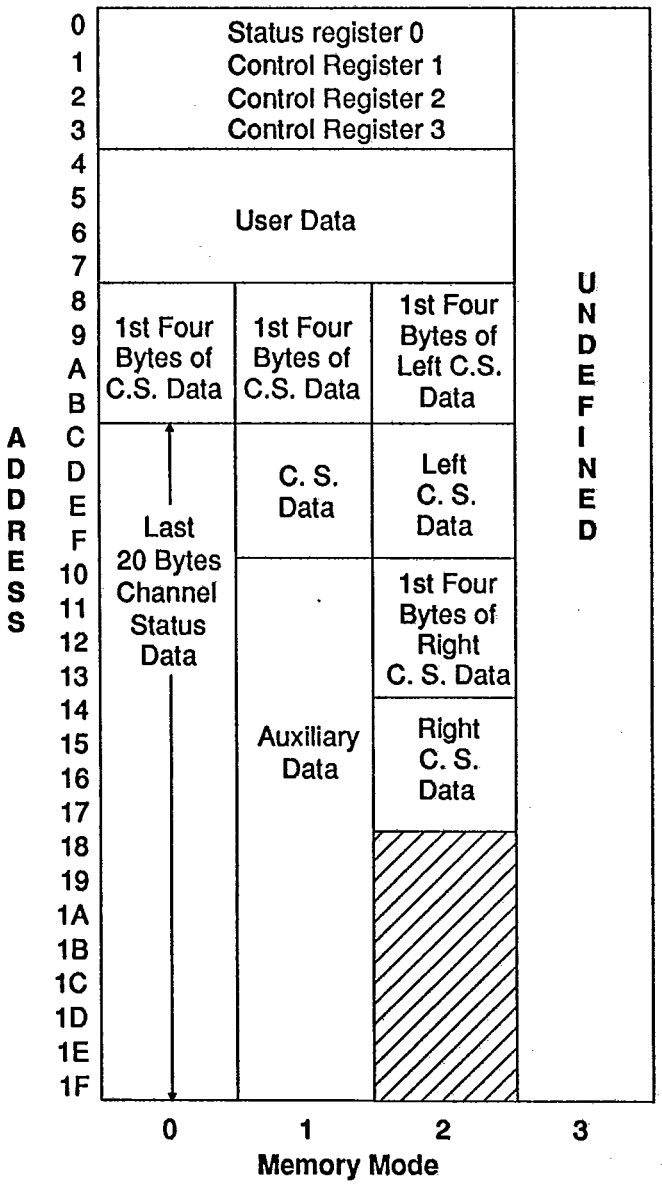
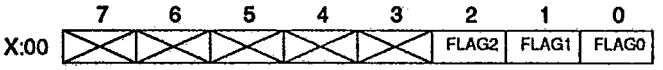
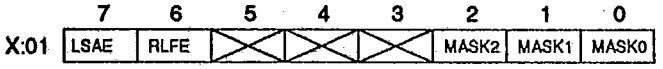


Figure 5. CS8401 Buffer Memory Modes



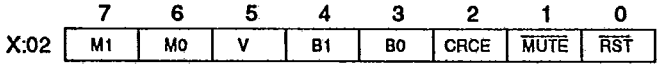
FLAG2: High for first four bytes of channel status
FLAG1: Memory mode dependent - See figure 11
FLAG0: High for last two bytes of user data.

Figure 6. Status Register



LSAE: Local Sample Address Enable. Professional mode only.
RLFE: Reliability Flag Enable. Professional mode only.
MASK2: Interrupt mask for FLAG2. A "1" enables the interrupt.
MASK1: Interrupt mask for FLAG1.
MASK0: Interrupt mask for FLAG0.

Figure 7. Control Register 1



M1: with M0, selects MCK frequency.
M0: with M1, selects MCK frequency.
V: Validity bit of current sample.
B1: with B0, selects the buffer memory mode.
B0: with B1, selects the buffer memory mode.
CRCE: Channel status CRC Enable. Professional mode only.
$\overline{\text{MUTE}}$: When clear, transmitted audio data is set to zero.
$\overline{\text{RST}}$: When clear, drivers are disabled, frame counters cleared.

Figure 8. Control Register 2

M1	M0	MCLK
0	0	128x Input Word Rate
0	1	192x Input Word Rate
1	0	256x Input Word Rate
1	1	384x Input Word Rate

Table 1. MCLK Frequencies

B1	B0	Mode	Buffer Memory Contents
0	0	0	Channel Status
0	1	1	Auxiliary Data
1	0	2	Independent Channel Status
1	1	3	Reserved

Table 2. Buffer Memory Modes

generated independently for channels A and B and are transmitted at the end of the channel status block. When $\overline{\text{MUTE}}$ (bit 1) is low, the transmitted audio data is forced to zero. As noted earlier, both $\overline{\text{RST}}$ and $\overline{\text{MUTE}}$ are set to zero upon power up.

When $\overline{\text{RST}}$ is low, the differential line drivers are set to ground and the block counters are reset to the beginning of the first block. In order to properly synchronize the rest of the CS8401 to the audio serial port, the transmit timing counters, which include the flags in the status register, are not enabled after $\overline{\text{RST}}$ is set high until eight and one half SCK periods after the active edge of FSYNC. When FSYNC is configured as a left/right signal (FSF1 = 1), the counters and flags are not enabled until the right sample is being entered (during which the previous left sample is being transmitted). This guarantees that channel A is left and Channel B is right as per the digital audio interface specs.

Control register 3 contains format information for the serial audio input channel. The MSB is unused and the next three bits, SDF2-SDF0, select the format for the serial input data with respect to FSYNC. There are five valid combinations of these bits as shown in figure 10. The next two bits, FSF1 and FSF0, select the format of FSYNC. Two of the formats delineate each channel's data and do not indicate the particular channel. The other two formats also indicate the specific channel. The formats are shown in figure 10. Bit 1, MSTR, determines whether FSYNC and SCK are inputs, MSTR low, or outputs, MSTR high. Bit 0, serial clock edge select, SCED, selects the edge that audio data gets latched on. When SCED is low, the falling edge of SCK latches data in the chip and when SCED is high, the rising edge is used.

	7	6	5	4	3	2	1	0
X:03		SDF2	SDF1	SDF0	FSF1	FSF0	MSTR	SCED

SDF2: with SDF0 & SDF1, select serial data format.
SDF1: with SDF0 & SDF2, select serial data format.
SDF0: with SDF1 & SDF2, select serial data format.
FSF1: with FSF0, select FSYNC format.
FSF0: with FSF1, select FSYNC format.
MSTR: When set, SCK and FSYNC are outputs.
SCED: When set, rising edge of SCK latches data.
When clear, falling edge of SCK latches data.

Figure 9. Control Register 3

The multitude of combinations allow for a zero glue logic interface to almost all DSP's, encoder chips, and standard serial data formats.

Serial Port

The serial port is used to enter audio data and consists of three pins: SCK, SDATA, and FSYNC. The serial port is double buffered with SCK clocking in the data from SDATA, and FSYNC delineating audio samples and may define the particular channel, left or right. Control register 3, shown in figure 9, configures the serial port. All the various formats are illustrated in figure 10. When FSF1 is low, FSYNC only delineates audio samples. When FSF1 is high, it delineates audio samples and specifies the channel. When FSF1 is low and the port is a master (MSTR = 1), FSYNC is a square wave output. When FSF1 is low and the port is a slave (input), FSYNC can be a square wave or a pulse provided the active edge, as defined in figure 10, is properly positioned with respect to SDATA. Bits 4, 5, and 6, SDF0-SDF2, define the format of SDATA and is also described in figure 10. The five allowable formats are MSB first, MSB last, 16-bit LSB last, 18-bit LSB last, and 20-bit LSB last. The MSB first and MSB last formats accept any word length from 16 to 24 bits. The word length is controlled by providing trailing zeros in MSB first mode and leading zeros in MSB last mode, or by restricting the number of SCK periods between samples to the sample word length. The 16-, 18-, and 20-bit LSB-last modes require at least 16, 18, or 20 SCK periods per sample respectively. As a master, 32 SCK periods are output per sample.

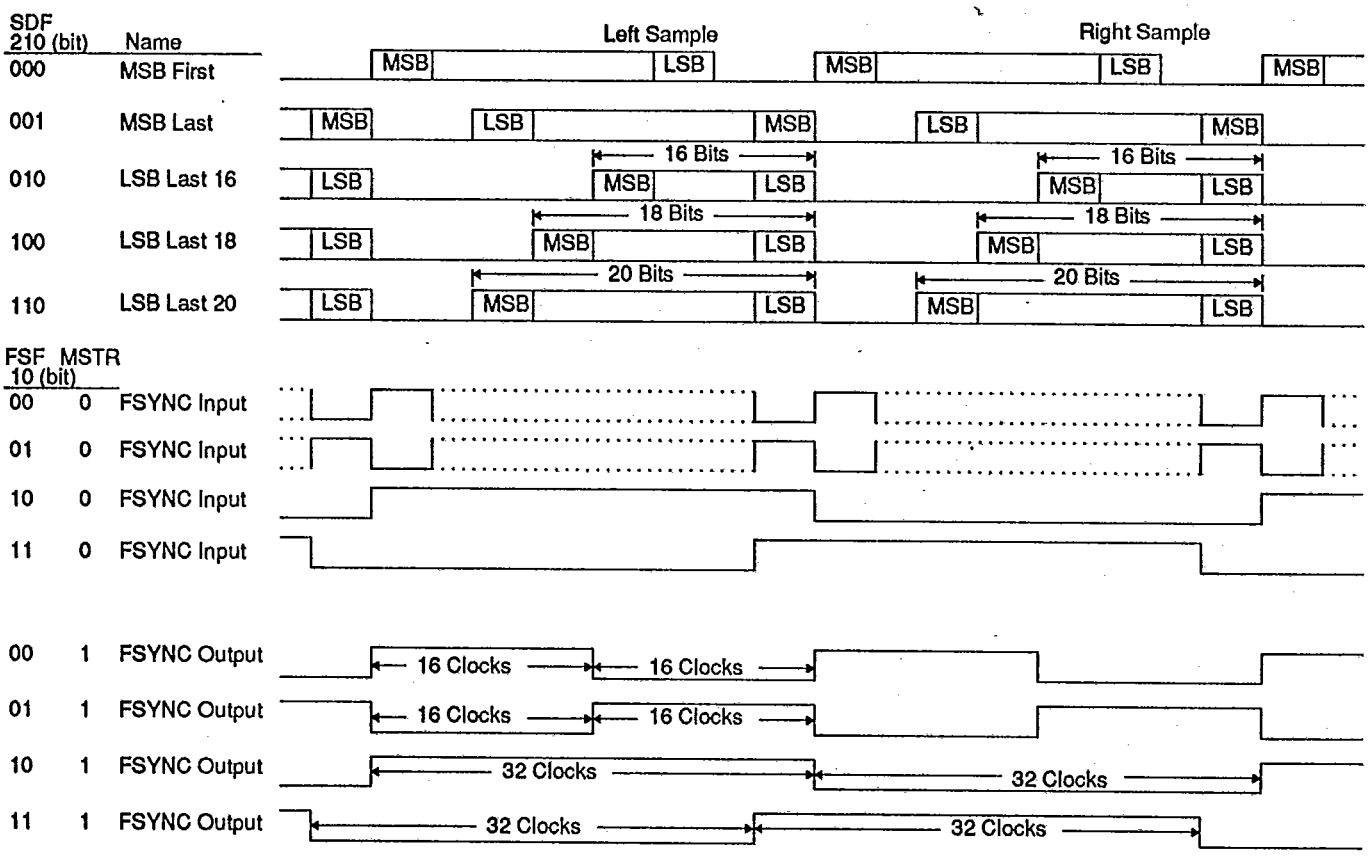


Figure 10. CS8401 Serial Port SDATA and FSYNC Timing

FSYNC must be derived from MCK via a DSP using the same clock or by external counters. If FSYNC moves (jitters) with respect to MCK by more than 4 MCK periods, the CS8401 may reset the channel status block and flags. Appendix C contains more information on the relationship of FSYNC and MCK.

Buffer Memory

In all buffer modes, the status register and control registers are located at addresses 0-3 respectively, and the user data is buffered in locations 4-7. The parallel port can access any location in the user data buffer at any time; however, care must be taken not to modify a location when that location is being read internally. This internal reading is done through the second port of the buffer and is done in a cyclic manner. Reset initializes the internal pointer to 04H (Hex). Data is read from this location and stored in an 8-bit shift register which is shifted once per audio sample. (An audio sample is defined as a single channel, not a stereo pair.) The byte is transmitted LSB first, D0 being the first bit. After transmitting 8 samples, i.e. 8 user bits, the address pointer is incremented and the next byte of user data is loaded into the shift register. After transmitting all four bytes, 32 audio samples, the user read pointer is reset to 04H (Hex) and the cycle repeats. Flag 0 in the status register monitors the position of the internal user data read pointer. When the first byte, location 04H, is read, flag 0 is set low and when the third byte, location 06H, is read, flag 0 is set high. If mask 0 in control register 1 is set, a transition of flag 0 will generate a low pulse on the interrupt pin. The value of flag 0 indicates which two

bytes the part will read next, thereby indicating which two bytes are free to be updated.

Flag 1 is mode dependent, changing with buffer memory configuration, and is discussed in the individual buffer mode sections.

Flag 2 is set high when byte 0 of the channel status, address 08H, is read, and set low when byte 4, address 0BH, is read. Therefore, flag 2 high indicates the part is reading the first four bytes of channel status, and the last 20 bytes are free to update. If the interrupt mask bit for flag 2 is set, the rising edge will cause an interrupt indicating the beginning of a channel status block as shown in figure 11. Although a falling edge on flag 0 and flag 1 may cause an interrupt, the falling edge of flag 2 will not.

Figure 11 illustrates the flag timing for an entire channel status block which includes 24 bytes of channel status data and 384 audio samples. (This

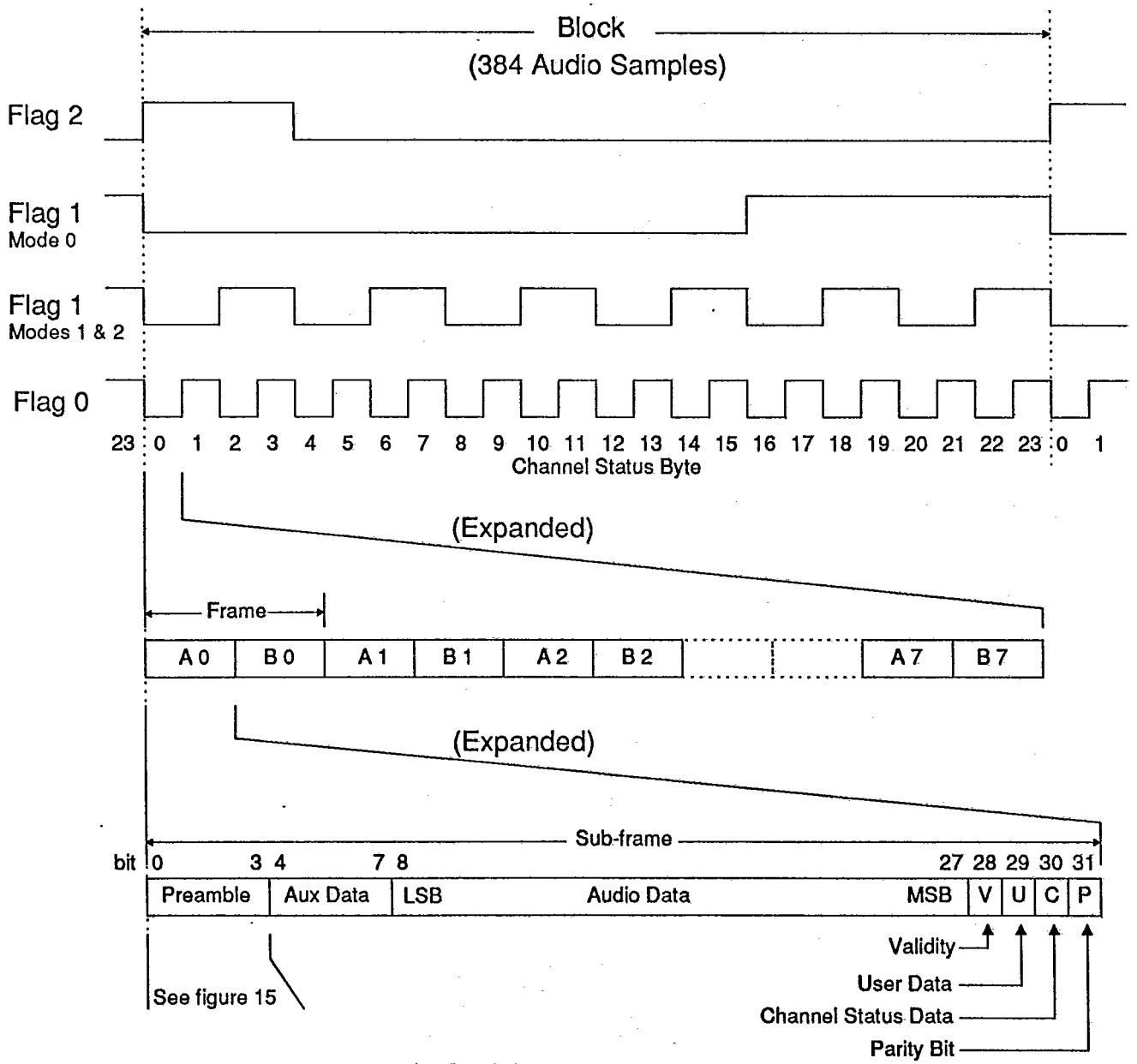


Figure 11. CS8401 Status Register Flag Timing

figure assumes the channel status bit is the same for the audio pair.) The lower portion of figure 11 expands the first byte of channel status showing eight pairs of data with a pair defined as a frame. This is further expanded showing the first sub-frame (A0) to contain 32 bits as per the AES/EBU specifications (see Appendix A). When transmitting stereo, channel A is left and channel B is right. The preamble at the bottom of figure 11 is expanded in figure 15 to show the exact timing between flags, the interrupt pin, and internal buffer-read timing.

Buffer Mode 0

In buffer mode 0, in addition to the user-data buffer previously discussed, one entire block of channel status data is buffered in 24 memory locations from address 08H to 1FH. This block will be transmitted in both channel A and channel B, one bit per frame. Like the user-data buffer, the parallel port can access any location in this buffer at any time. The transmitter section reads this buffer in a cyclic non-destructive manner and stores the byte in an 8-bit shift register that is shifted once per two transmitted audio samples (once per frame). Flag 1 in the status register can be used to monitor the channel status buffer. In mode 0, flag 1 is set low when byte 0, location 08H, is read, and set high when byte 16, location 18H, is read. If mask 1 in control register 1 is set, a transition on flag 1 will generate a pulse on the interrupt pin. Figure 12 illustrates the memory read sequence for buffer mode 0 along with the flag timing. The arrows on the flags indicate an interrupt if the appropriate mask bit is set. Flag 0 can cause an interrupt on either edge, which is shown only in the expanded portion of the figure for clarity. The expanded section also shows that the user buffer is reread when location 0AH of the channel status is read.

Buffer Mode 1

In buffer mode 1, eight bytes are allocated for channel status data and 16 bytes for auxiliary data as shown in figure 5. The channel status buffer, locations 08H to 0FH, is divided into two sections. The first four locations always contain the first four bytes of channel status, identical to mode 0, and are read once per channel status

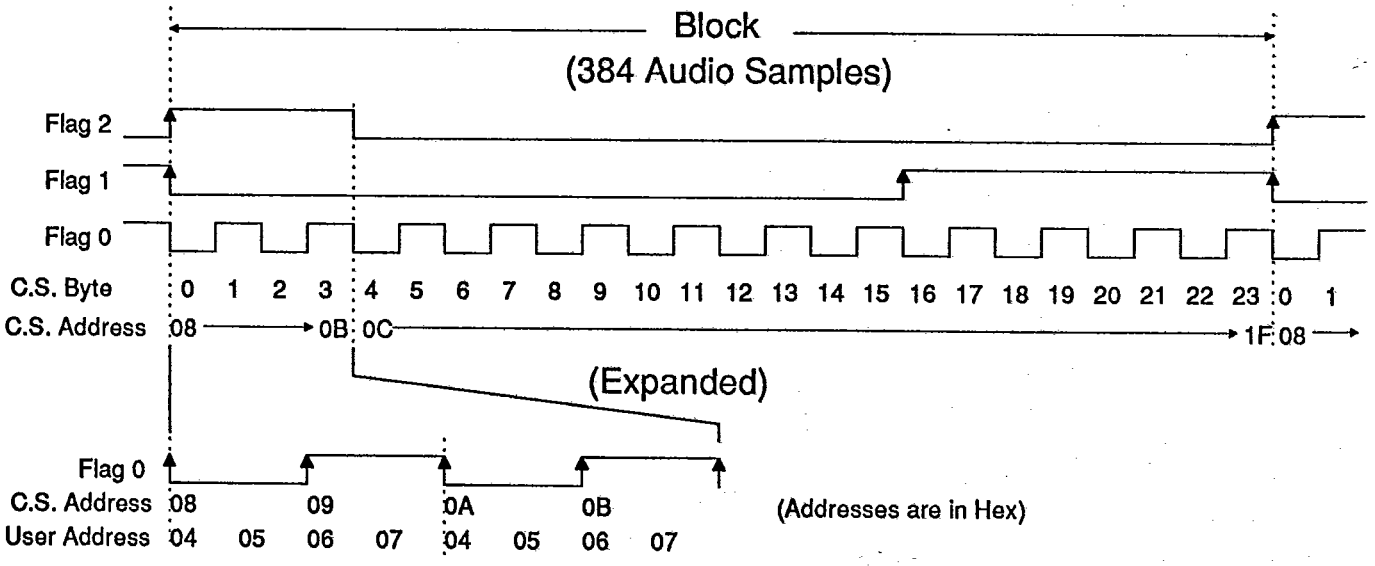


Figure 12. CS8401 Buffer Memory Read Sequence - MODE 0

block. The second four locations, addresses 0CH to 0FH, provide a cyclic buffer for the last 20 bytes of channel status data. Similar to mode 0, transmitted channel status data will be the same for channel A and channel B (one channel status bit per frame). Flag 1 and flag 2 can be used to monitor this buffer. Flag 1 is set low when byte 0 of channel status data, location 08H, is read and is toggled when every other byte is read. As shown in figure 13, flag 2 is set high when byte 0, location 08H, is read and set low when byte 4, location 0CH, is read. Flag 2 determines whether the channel status pointer is reading the first four-byte section or the second four-byte section, while flag 1 indicates which two bytes of the section are free to update.

The auxiliary data buffer, locations 10H to 1FH, is read in a cyclic manner similar to the data buffer; however, four auxiliary data bits are transmitted per audio sample (sub-frame). Since the auxiliary buffer must be read four times as often as the user data buffer and is four times as large, flag 0 can be used to monitor both.

Buffer Mode 2

In buffer mode 2, two 8-byte buffers are available for buffering both channel A and channel B channel status data independently. Both buffers are identical to the channel status buffer in mode 1 except that each channel can have unique channel status data. The two buffers are read simultaneously with locations 08H to 0FH transmitted in channel A and locations 10H to 17H transmitted in channel B. Figure 5 contains the buffer memory modes and figure 14 illustrates the buffer read sequence for mode 2.

Buffer-Read and Interrupt Timing

As mentioned previously in the buffer mode sections, conflicts between externally writing to the buffer ram and the CS8401 internally reading bytes of ram for transmission may be averted by using the flag levels to avoid the section current-

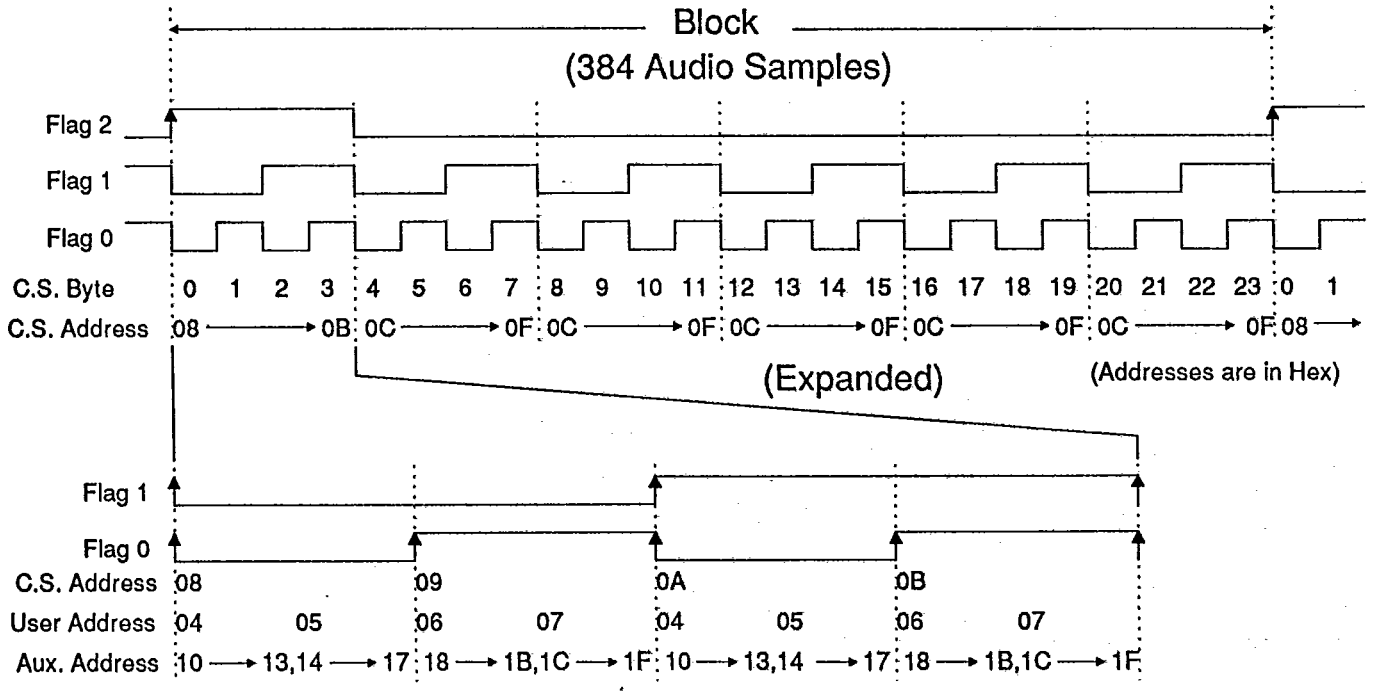


Figure 13. CS8401 Buffer Memory Read Sequence - MODE 1

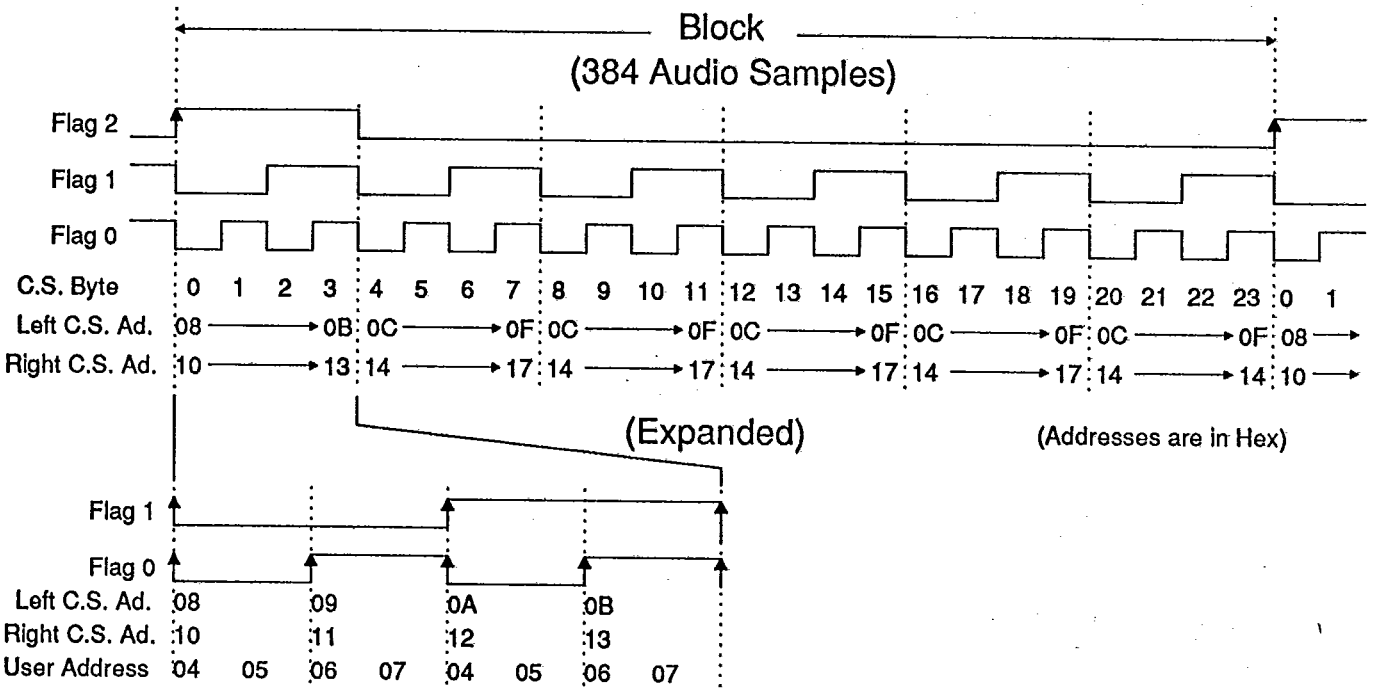


Figure 14. CS8401 Buffer Memory Read Sequence - MODE 2

ly being addressed by the part. Interrupts occur at flag edges indicating the exact byte that the part is currently reading. Utilizing $\overline{INT}$ along with the flags, the byte currently being read by the part can be avoided allowing access to all other bytes instead of just a section. Figure 15 illustrates the timing between flags, $\overline{INT}$, and the internal reading of the buffer for transmission. The master clock IMCK is shown as 128×Fs. Other MCK frequencies are initially divided to obtain 128×Fs, defined as IMCK (internal MCK), which is then used for all internal timing, so the timing in figure 15 is valid for all MCK frequencies. When the parity bit (P) is transmitted, a transition on a flag causes $\overline{INT}$ to go low if the appropriate mask bit is set. Concurrently, the part starts reading from the internal buffer. Writing to the buffer ram location being read by the part should be avoided while the internal "ram read" signal is high.

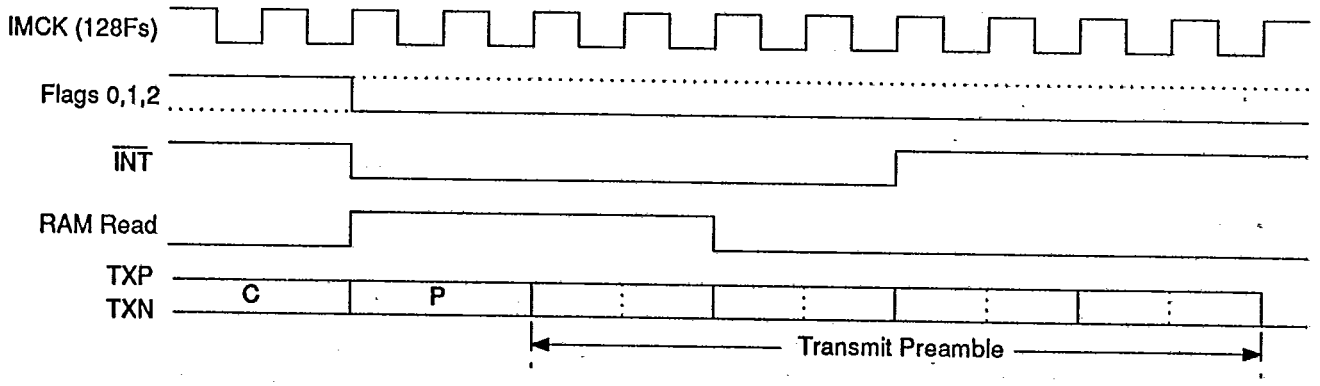
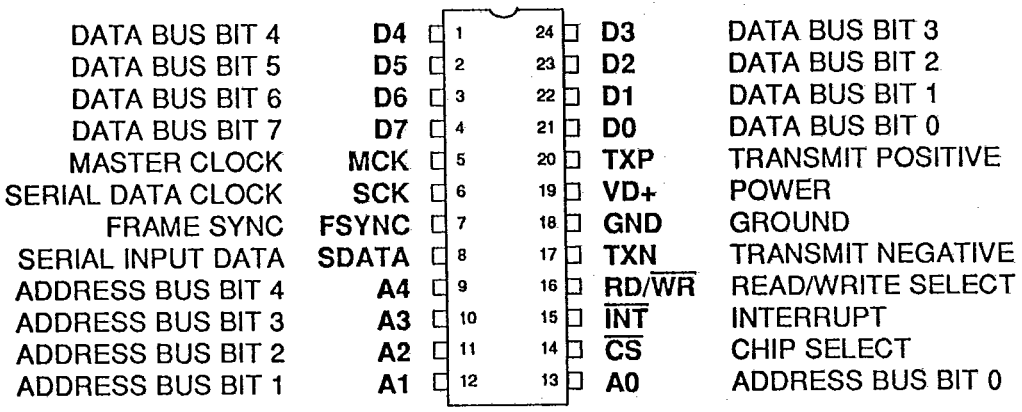


Figure 15. RAM/Buffer-Read and Interrupt Timing

PIN DESCRIPTIONS

CS8401



Power Supply Connections

VD+ - Positive Digital Power, PIN 19.
Positive supply for the digital section. Nominally +5 volts.

GND - Ground, PIN 18.
Ground for the digital section.

Audio Input Interface

SCK - Serial Clock, PIN 6.
Serial clock for SDATA pin which can be configured (via control register 3) as an input or output, and can sample data on the rising or falling edge. As an output, SCK will contain 32 clocks for every audio sample. As an input, it does not need to be continuous and can be up to 15 MHz.

FSYNC - Frame Sync, PIN 7.
Delineates the serial data and may indicate the particular channel, left or right. Also, FSYNC may be configured as an input or output. The format is based on bits in control register 3.

SDATA - Serial Data, PIN 8.
Audio data serial input pin.

Parallel Interface

$\overline{CS}$ - Chip Select, PIN 14.
This input is active low and allows access to the 32 bytes of internal memory. The address bus and RD/$\overline{WR}$ must be valid while $\overline{CS}$ is low.

RD/$\overline{WR}$ - Read/Write, PIN 16.

If RD/$\overline{WR}$ is low when $\overline{CS}$ goes active (low), the data on the data bus is written to internal memory. If RD/$\overline{WR}$ is high when $\overline{CS}$ goes active, the data in the internal memory is placed on the data bus.

A4-A0 - Address Bus, PINS 9-13.

Parallel port address bus that selects the internal memory location to be read from or written to.

D0-D7 - Data Bus, PINS 21-24, 1-4.

Parallel port data bus used to check status, write control words, or write internal buffer memory.

$\overline{INT}$ - Interrupt, PIN 15.

Open drain output that can signal the state of the internal buffer memory.

Transmitter Interface

MCK - Master Clock, PIN 5.

Clock input which defines the transmit timing. It can be configured, via control register 2, for 128, 192, 256, or 384 times the sample rate.

TXP, TXN - Differential Line Drivers, PINS 20, 17.

RS422 compatible line drivers.

CS8402 DESCRIPTION

The CS8402 accepts 16- to 24-bit audio samples through a serial port configured in one of seven formats; provides several pins dedicated to particular channel status bits; and allows all channel status, user, and validity bits to be serially input through port pins. This data is multiplexed, the parity bit is generated, and the bit stream is biphase-mark encoded and driven through an RS422 line driver. The CS8402 operates as a professional or consumer interface transmitter selectable by pin 2, $\overline{PRO}$. As a professional interface device, the dedicated channel status input pins are defined according to the professional standard, and the local sample address (channel status, C.S., bytes 14-17), the reliability flag (C.S. byte 22), and the CRCC code (C.S. byte 23) can be internally generated. As a consumer device, the dedicated channel status input pins are defined according to the consumer standard. A submode provided under the consumer mode is compact disk, CD, mode. When transmitting data from a compact disk, the CD subcode port can accept CD subcode data, extract channel status information from it, and transmit it as user data.

The master clock, MCK, controls timing for the entire chip and must be 128×Fs. As an example, if stereo data is input to the CS8402 at 44.1 kHz, MCK input must be 128 times that or 5.6448 MHz.

Audio Serial Port

The audio serial port is used to enter audio data and consist of three pins: SCK, SDATA, and FSYNC. SCK clocks in SDATA, which is double buffered, while FSYNC delineates the audio samples and may indicate the particular channel, left or right. To support many different interfaces, M2, M1, and M0 select one of seven different formats for the serial port. The coding is shown in table 3 while the formats are shown in figure 16. Format 0 and 1 are designed to interface with Crystal ADCs. Format 2 communicates with Motorola and TI DSPs. Format 3 is reserved. Format 4 is compatible with the I^2S standard. Formats 5 and 6 make the CS8402 look similar to existing 16- and 18-bit DACs, and interpolation filters. Format 7 is an MSB-last format and is conducive to serial arithmetic. SCK and FSYNC are outputs in format 0 and inputs in all other formats. In format 2, the rising edge of FSYNC delineates samples and the falling edge must occur a minimum of one bit period before or after the rising edge. In all formats except 2, FSYNC contains left/right information requiring both edges of FSYNC to delineate samples. Formats 5 and 6 require a minimum of 16- or 18-bit audio words respectively. In all formats other than 5 and 6, the CS8402 can accept any word length from 16 to 24 bits by adding leading zeros in format 7 and trailing zeros in the other formats, or by restricting the number of SCK periods between active edges of FSYNC to the sample word length.

M2	M1	M0	Format
0	0	0	0 - FSYNC & SCK Output
0	0	1	1 - Left/Right, 16-24 Bits
0	1	0	2 - Word Sync, 16-24 Bits
0	1	1	3 - Reserved
1	0	0	4 - Left/Right, I^2S Compatible
1	0	1	5 - LSB Justified, 16 Bits
1	1	0	6 - LSB Justified, 18 Bits
1	1	1	7 - MSB Last, 16-24 Bits

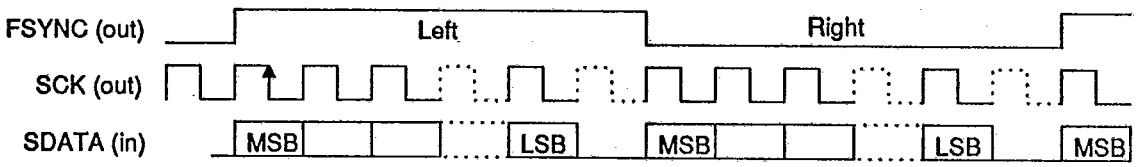
Table 3. CS8402 Audio Port Modes

FSYNC must be derived from MCK, either thru a DSP using the same clock, or using counters. If FSYNC moves (jitters) with respect to MCK by four MCK periods, the internal counters and CBL may be reset. Appendix C contains more information on the relationship between FSYNC and MCK.

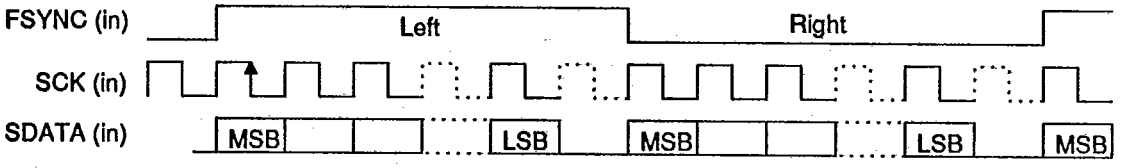
C, U, V Serial Port

The serial input pins for channel status (C) , user (U), and validity (V) are sampled during the first

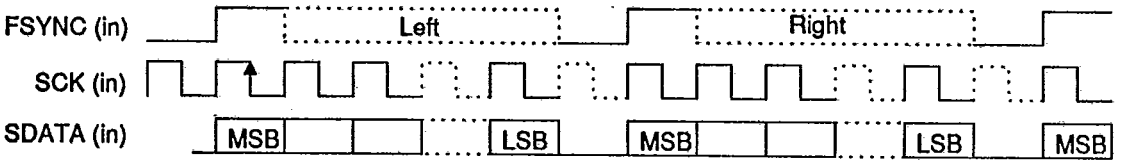
FORMAT 0:



FORMAT 1:



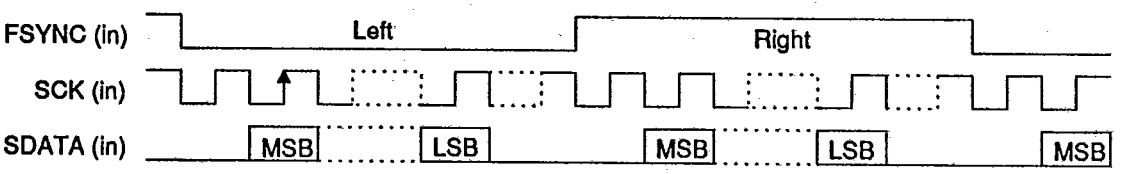
FORMAT 2:



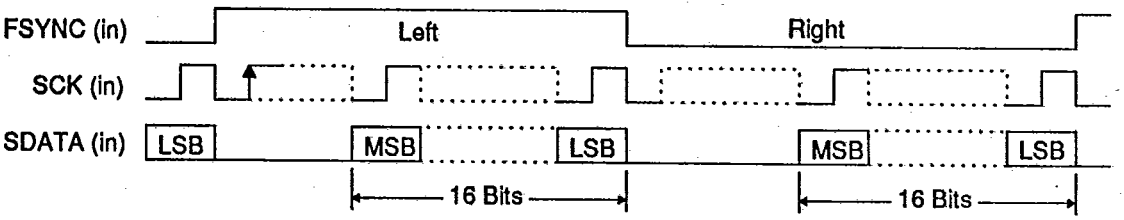
FORMAT 3:

(RESERVED)

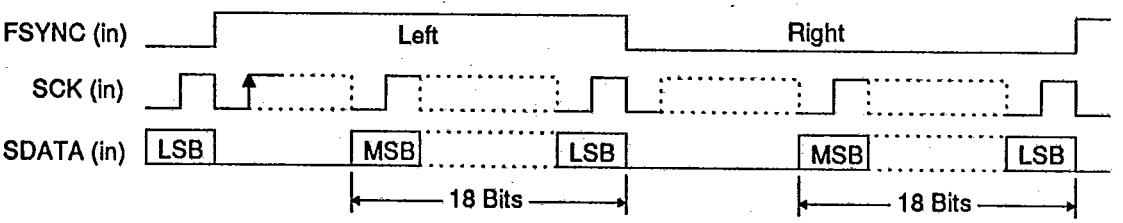
FORMAT 4:



FORMAT 5:



FORMAT 6:



FORMAT 7:

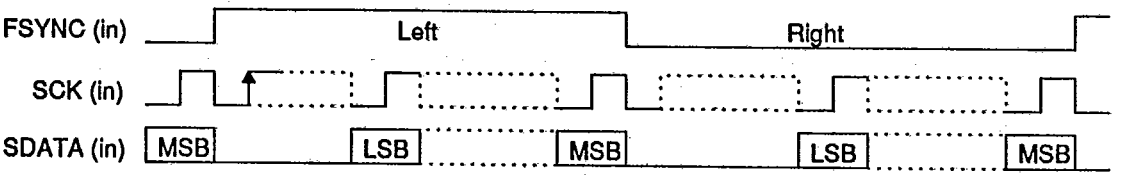


Figure 16. CS8402 Audio Serial Port Formats

bit period after the active edge of FSYNC for all formats except format 4, which is sampled during the second bit period (coincident with the MSB). In figure 16, the arrows on SCK indicate when the C, U, and V bits are sampled. The C, U, and V bits are transmitted with the audio sample entered before the FSYNC edge that sampled it. The channel status serial input pin (C) is not available in consumer mode when the CD subcode port is enabled (FC1 = FC0 = high). Any channel status data entered through the channel status serial input (C) is logically OR'ed with the data entered through the dedicated pins or internally generated.

$\overline{RST}$ and CBL

When $\overline{RST}$ goes low, the differential line drivers are set to ground and the block counters are reset to the beginning of the first block. In order to properly synchronize the CS8402 to the audio serial port, the transmit timing counters, which include CBL, are not enabled after $\overline{RST}$ goes high until eight and one half SCK periods after the active edge of FSYNC. When FSYNC is configured as a left/right signal (all defined formats except 2), the counters and CBL are not enabled until the right sample is being entered (during which the previous left sample is being transmitted). This guarantees that channel A is left and channel B is right as per the digital audio interface specs.

As shown in figure 17, CBL, channel block start output, can assist in serially inputting the C, U and V bits as CBL goes high one bit period before the first bit of the preamble of the first sub-frame of the channel status block is transmitted. This sub-frame contains channel status byte 0, bit 0. CBL returns low one bit period before the start of the frame that contains bit 0 of channel status byte 16. CBL is not available when the CD subcode port is enabled.

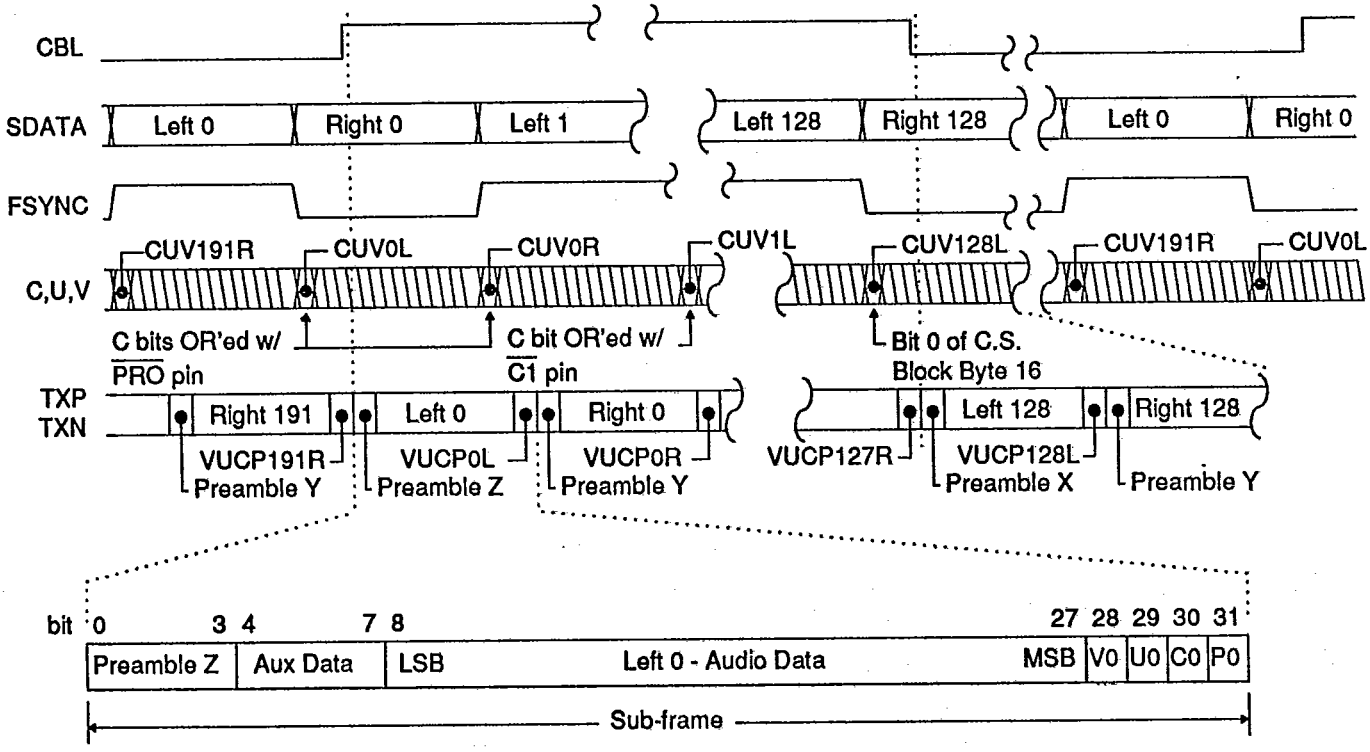


Figure 17. CBL and Transmitter Timing

Figure 17 illustrates timing for stereo data input on the audio port. Notice how CBL rises while the right channel data (Right 0) is input, but the previous left channel data (Left 0) is being transmitted as the first sub-frame of the channel status block (starting with preamble Z). The C, U, and V input ports only need to be valid for a short period after FSYNC changes. A sub-frame includes one audio sample while a frame includes a stereo pair. A channel status (C.S.) block contains 24 bytes of channel status and 384 audio samples (or 192 stereo pairs, or frames, of samples). Figure 17 shows the CUV ports as having left and right bits (e.g. CUV0L, CUV0R). Since the C.S. block is defined as 192 bits, or one bit per frame, there are actually 2 C.S. blocks, one for channel A (left) and one for channel B (right). When inputting stereo audio data, both blocks normally contain the same information, so C0L and C0R from the input port pin are both channel status bit 0 of byte 0, which is defined as professional/consumer. These first two bits from the port, C0L and C0R, are logically OR'ed with the inverse of $\overline{PRO}$, since $\overline{PRO}$ is a dedicated channel status pin defined as C.S. bit 0. Also, if in professional mode, $\overline{C1}$ is a dedicated C.S. pin and the inverse of $\overline{C1}$ is logically OR'ed with channel status input port bits C1L and C1R. Also, the C bits in CUV128L and CUV128R are both channel status block bit 128, which is bit 0 of channel status byte 16.

Professional Mode

Setting $\overline{PRO}$ low places the CS8402 in professional mode as shown in figure 18. In professional mode, channel status bit 0 is transmitted as a one and bits 1, 2, 3, 4, 6, 7, and 9 can be controlled via dedicated pins. The pins are actually the inverse of the identified bit. For example, tying the $\overline{C1}$ pin low places a one in

EM1	EM0	C2	C3	C4
0	0	1	1	1
0	1	1	1	0
1	0	1	0	0
1	1	0	0	0

Table 4. Emphasis Encoding

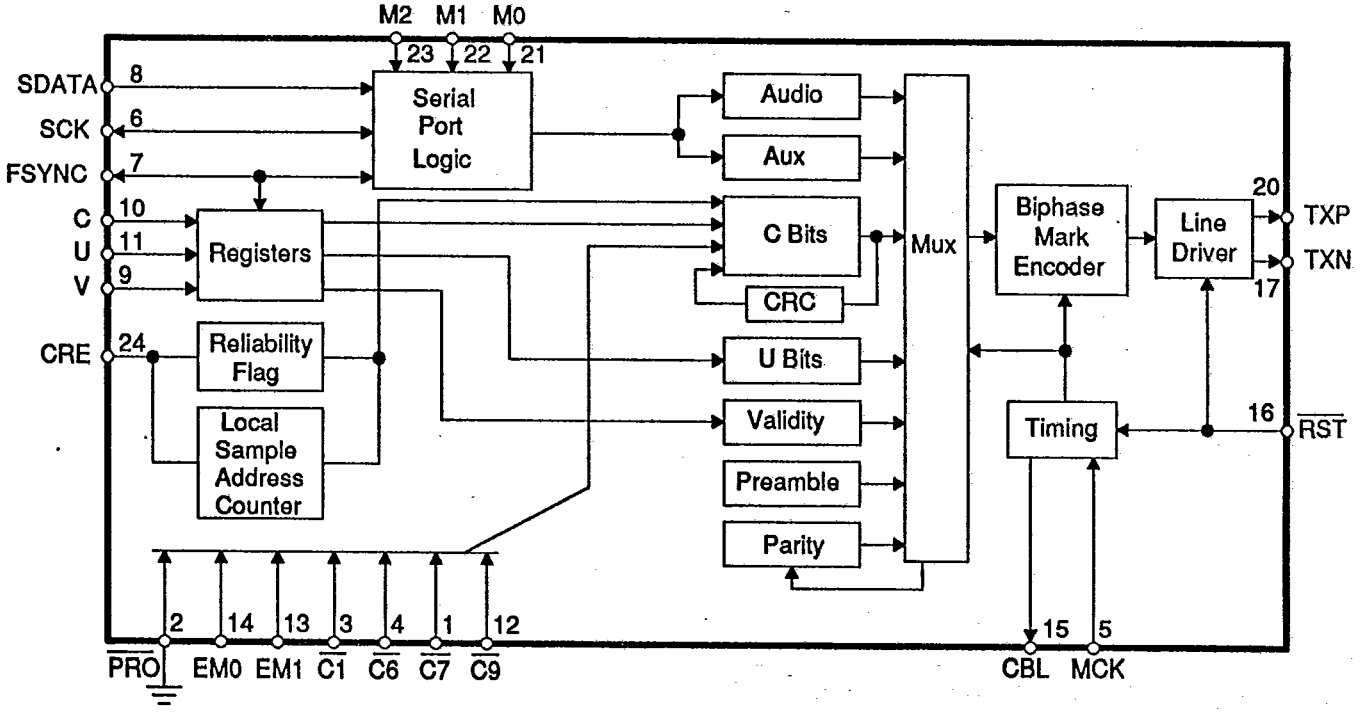


Figure 18. CS8402 Block Diagram - Professional Mode

channel status bit 1. As shown in Appendix A, C1 indicates audio/non-audio; C6 and C7 determine the sample frequency; and C9 allows the encoded channel mode to be stereophonic. EM1 and EM0 determine emphasis and encode C2, C3, C4 as shown in Table 4. The dedicated channel status pins are read at the appropriate time and are logically OR'ed with data input on the channel status port, C.

When CRE, pin 24, is high, the local sample address (channel status, C.S., bytes 14-17) and the reliability flag (C.S. byte 22) are internally generated. The local sample address counter can be reset by holding CRE low for a minimum of 5 MCK periods. When CRE is high, the reliability flag byte, bits 5 and 7 are transmitted as ones, and the local sample address counter is incremented at the end of each channel status block.

The channel status data cyclic redundancy check character (C.S. byte 23) is always generated independently for channels A and B and is transmitted at the end of the channel status block.

Data should not be input thru the channel status port, C, during the CRCC byte time frame, or, if CRE is high, during the local sample address and reliability bytes, since inputs on C are logically OR'ed with internally generated data.

Consumer Mode

Setting $\overline{\text{PRO}}$ high places the CS8402 in consumer mode which redefines the pins as shown in figure 19. In consumer mode, channel status bit 0 is transmitted as a zero and channel status bits 2, 3, 8, 9, 15, 24, and 25 are controlled via dedicated pins. The pins are actually the inverse of the bit so if pin

FC1	FC0	C24	C25	Comments
0	0	0	0	44.1 kHz
0	1	0	1	48 kHz
1	0	1	1	32 kHz
1	1	0	0	44.1 kHz, CD Mode

Table 5. Sample Frequency Encoding

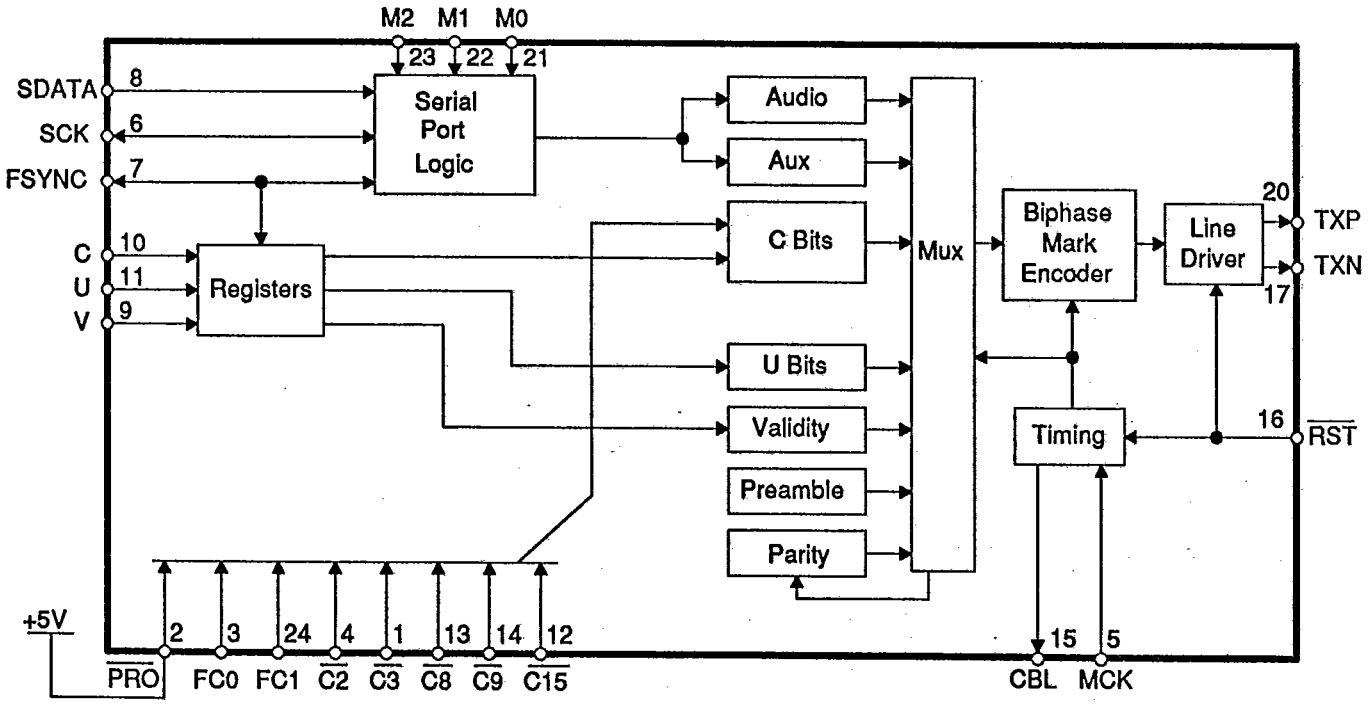


Figure 19. CS8402 Block Diagram - Consumer Mode

$\overline{C2}$ is tied high, channel status bit 2 will be transmitted as a zero. Also, FC0 and FC1 are encoded versions of channel status bits 24 and 25, which define the sample frequency. When FC0 and FC1 are both high, the part is placed in a CD submode which activates the CD subcode port. This submode is described in detail in the next section. Table 5 describes the encoding of C24 and C25 through the FC1 and FC0 pins. As shown in Appendix A, C2 is copy prohibit/permit, C3 specifies pre-emphasis, C8 and C9 define the category code, and C15 identifies the generation status of the transmitted material (ie. first generation, second generation).

Consumer - CD Submode

The consumer CD submode is invoked by placing the part in consumer mode ($\overline{PRO}$ = high) and setting both FC1 and FC0 high. This mode redefines some of the pins for a CD subcode port as shown in figure 20. The CD subcode port pins, SBF and SBC, replace the channel status serial input, C, and the channel status block start output, CBL. The user data serial input, U, becomes the subcode input. Figure 21 describes the timing for the CD subcode port. When SBF is low, SBC goes high one and a half SCK periods after the active edge of FSYNC for audio serial input port format 4, and one half SCK period after the active edge of FSYNC for all other formats. SBC stays high for one SCK period. SBF high for more than 16 SCK periods indicates the start of a subcode block. The first, third, and fourth Q bits after the start of a subcode block become channel status bits 5, 2, and 3 respectively.

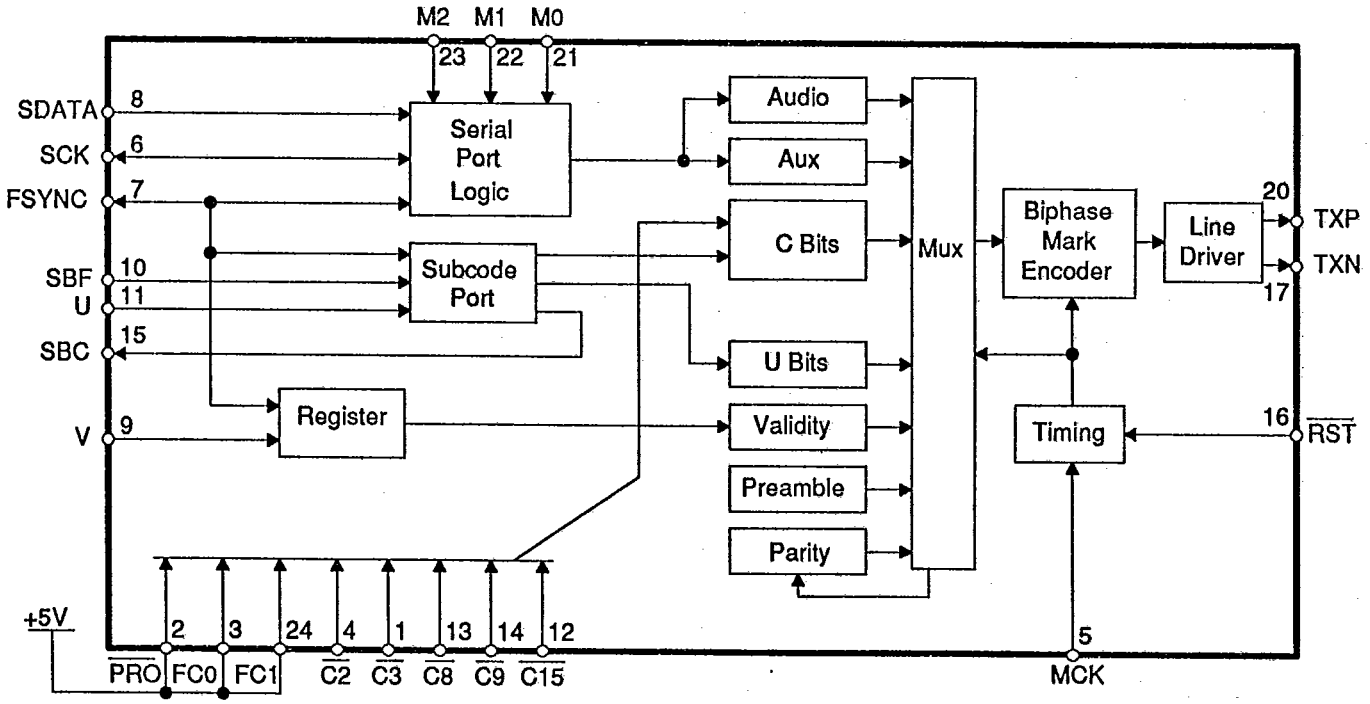


Figure 20. CS8402 Block Diagram - Consumer Mode, CD Submode

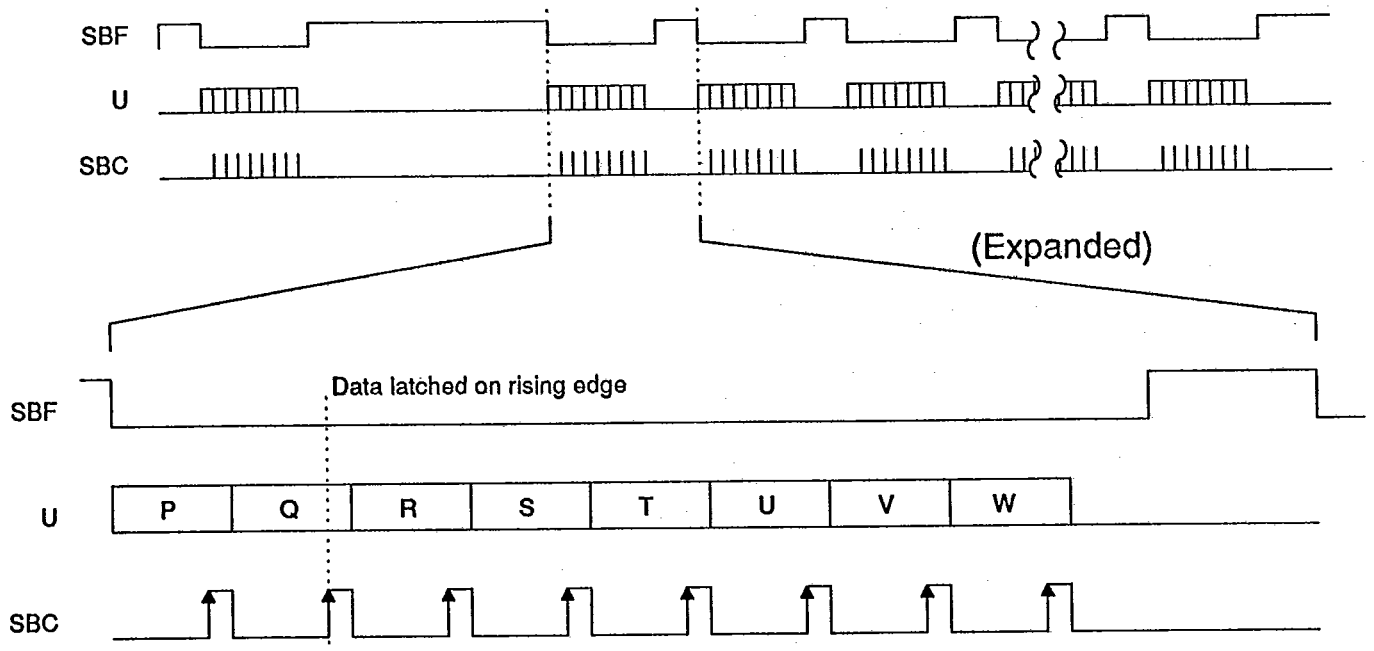
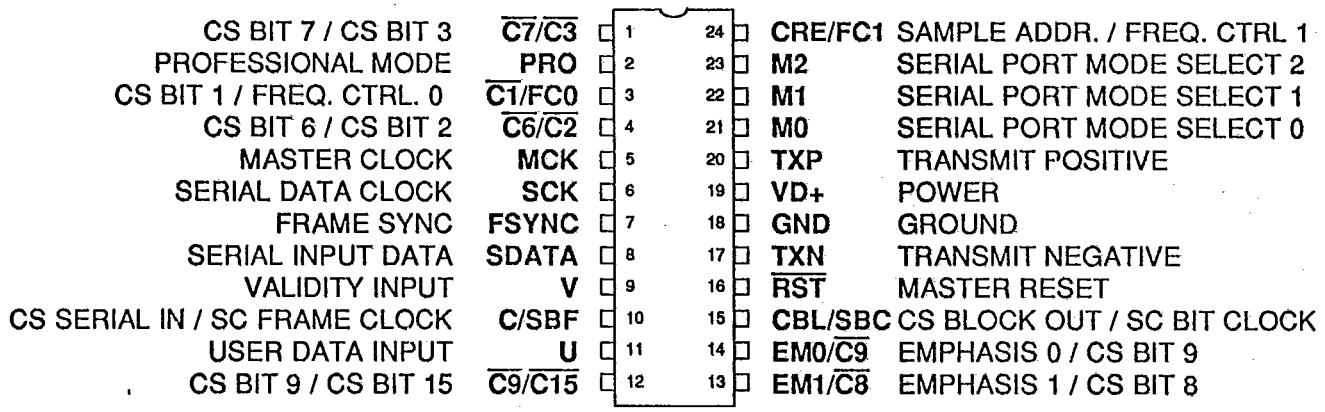


Figure 21. CD Subcode Port Timing

PIN DESCRIPTIONS

CS8402



Power Supply Connections

VD+ - Positive Digital Power, PIN 19.

Positive supply for the digital section. Nominally +5 volts.

GND - Ground, PIN 18.

Ground for the digital section.

Audio Input Interface

SCK - Serial Clock, PIN 6.

Serial clock for SDATA pin which can be configured (via the M0, M1, and M2 pins) as an input or output, and can sample data on the rising or falling edge. As an output, SCK will contain 32 clocks for every audio sample. As an input, it does not need to be continuous and can be up to 15 MHz.

FSYNC - Frame Sync, PIN 7.

Delineates the serial data and may indicate the particular channel, left or right, and may be an input or output. The format is based on M0, M1, and M2 pins.

SDATA - Serial Data, PIN 8.

Audio data serial input pin.

M0, M1, M2 - Serial Port Mode Select, PINS 21, 22, 23.

Selects the format of FSYNC and the sample edge of SCK with respect to SDATA.

Control Pins

$\overline{\text{RST}}$ - Master Reset, PIN 16.
When low, all internal counters are reset and the line drivers are disabled.

V - Validity, PIN 9.
Validity bit serial input port.

U - User Bit, PIN 11.
User bit serial input port.

$\overline{\text{PRO}}$ - Professional/Consumer Select, PIN 2.
Selects between professional mode ($\overline{\text{PRO}}$ low) and consumer mode ($\overline{\text{PRO}}$ high). This pin defines the functionality of the next seven pins.

$\overline{\text{C9}}$/$\overline{\text{C15}}$ - Channel Status Bit 9 / Channel Status Bit 15, PIN 12.
In professional mode, $\overline{\text{C9}}$ is the inverse of channel status bit 9 (bit 1 of byte 1). In consumer mode, $\overline{\text{C15}}$ is the inverse of channel status bit 15 (bit 7 of byte 1).

EM0/$\overline{\text{C9}}$ - Emphasis 0 / Channel Status Bit 9, PIN 14.
In professional mode, EM0 and EM1 encode channel status bits 2, 3, and 4. In consumer mode, $\overline{\text{C9}}$ is the inverse of channel status bit 9 (bit 1 or byte 1).

EM1/$\overline{\text{C8}}$ - Emphasis 1 / Channel Status Bit 8, PIN 13.
In professional mode, EM0 and EM1 encode channel status bits 2, 3, and 4. In consumer mode, $\overline{\text{C8}}$ is the inverse of channel status bit 8 (bit 0 of byte 1).

$\overline{\text{C7}}$/$\overline{\text{C3}}$ - Channel Status Bit 7 / Channel Status Bit 3, PIN 1.
In professional mode, $\overline{\text{C7}}$ is the inverse of channel status bit 7. In consumer mode, $\overline{\text{C3}}$ is the inverse of channel status bit 3.

$\overline{\text{C6}}$/$\overline{\text{C2}}$ - Channel Status Bit 6 / Channel Status Bit 2, PIN 4.
In professional mode, $\overline{\text{C6}}$ is the inverse of channel status bit 6. In consumer mode, $\overline{\text{C2}}$ is the inverse of channel status bit 2.

$\overline{\text{C1}}$/FC0 - Channel Status Bit 1 / Frequency Control 0, PIN 3.
In professional mode, C1 is the inverse of channel status bit 1. In consumer mode, FC0 and FC1 are encoded versions of channel status bits 24 and 25 (bits 0 and 1 of byte 3). When FC0 and FC1 are both high, CD mode is selected.

CRE/FC1 - Local Sample Addr. & Reliability Flag Reset & Enable / Frequency Control 1, PIN 24.

In professional mode, when CRE is high, the channel status local sample address and reliability flag are internally generated. In consumer mode, FC0 and FC1 are encoded versions of channel status bits 24 and 25. When FC0 and FC1 are both high, CD mode is selected.

C/SBF - Channel Status Serial Input / Subcode Frame Clock, PIN 10.

In professional and consumer modes this pin is the channel status serial input port. In CD mode this pin inputs the CD subcode frame clock.

CBL/SBC - Channel Status Block Output / Subcode Bit Clock, PIN 15.

In professional and consumer modes, the channel status block output is high for the first four bytes of channel status. In CD mode, this pin outputs the subcode bit clock.

Transmitter Interface

MCK - Master Clock, PIN 5.

Clock input at 128× the sample frequency which defines the transmit timing.

TXP, TXN - Differential Line Drivers, PINS 20, 17.

RS422 compatible line drivers.

Appendix A: AES/EBU Reference

The following information is provided for convenience, but by no means constitutes the entire specification. Also included is information from the IEC-958 and the new AES3-199x and TC84 documents. The AES3-199x and TC84 documents have not received approval as of the printing of this data sheet. To guarantee conformance, a copy of the actual specification should be obtained from the Audio Engineering Society or ANSI (ANSI S4.40-1985) for the AES3 document, and the International Electrotechnical Commission for the IEC-958 document.

The AES/EBU interface is a means for serially communicating digital audio data through a single transmission line. It provides two channels for audio data, a method for communicating control information, and some error detection capabilities. The control information is transmitted as one bit per sample and accumulates in a block structure. The data is biphase encoded, which enables the receiver to extract a clock from the data. Coding violations, defined as preambles, are used to identify sample and block boundaries.

An audio sample is placed in a structure known as a sub-frame. The sub-frame, shown in figure A1, consists of 4 bits of preamble, 4 bits of auxiliary data, 20 bits of audio data, 3 bits called validity, user, and channel status, and a parity bit. The preamble contains biphase coding violations and identifies the start of a sub-frame. The audio sample word length can vary up to 24 bits and is transmitted LSB first. If the word length is greater than 20 bits, the sample occupies both the audio and auxiliary data fields. If it is 20 bits or less, the auxiliary field can be used for other applications such as voice. The parity bit generates even parity and can detect an odd number of transmission errors in the sub-frame. The validity bit indicates the audio sample is fit for conversion to analog. The user and channel status bits are sent once per sample and, when accumulated over a number of samples, define a block of data. The user bit channel is undefined and available to the user for any purpose. The channel status bit conveys, over an entire block, important information about the audio data and transmission link. Each of the two audio channels has its own channel status data with a block structure that repeats every 192 samples.

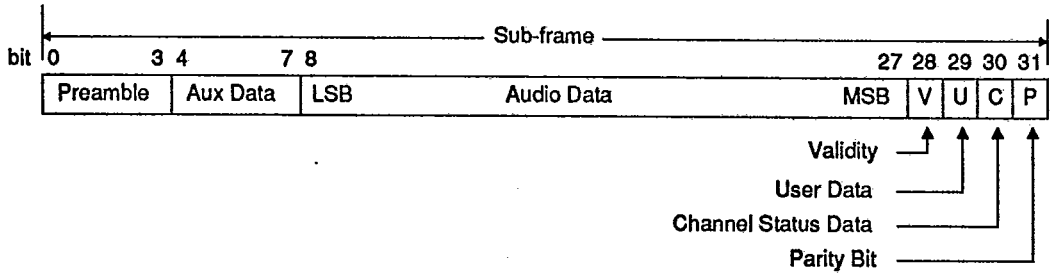


Figure A1. Sub-frame Format

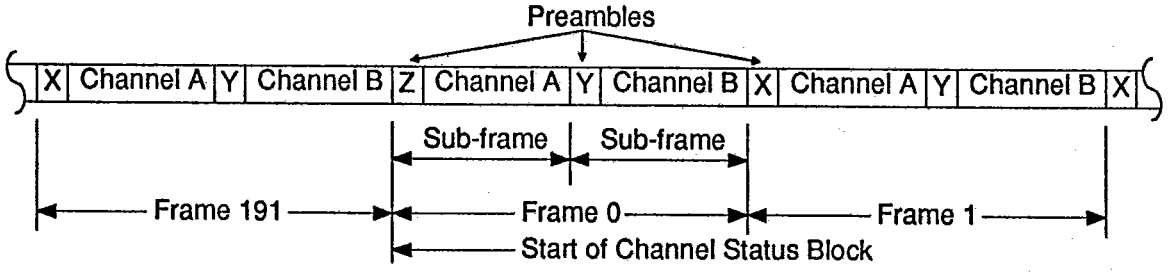


Figure A2. Frame/Block Format

As shown in figure A2, two consecutive sub-frames are defined as a frame, containing channels A and B, and 192 frames define a block. The preambles that identify the start of a sub-frame are different for each of the two channels with another unique one identifying the beginning of a channel status block.

Modulation and Preambles

The data is transmitted with biphase-mark encoding to minimize the DC component and to allow clock recovery from the data. As illustrated in figure A3, the 1's in the data have transitions in the center, and the 0's do not, after biphase-mark encoding. Also, the biphase-mark data switches polarity at every data bit boundary. Since the value of the data bit is determined by whether their is a transition in the center of the bit, the actual polarity of the signal is irrelevant.

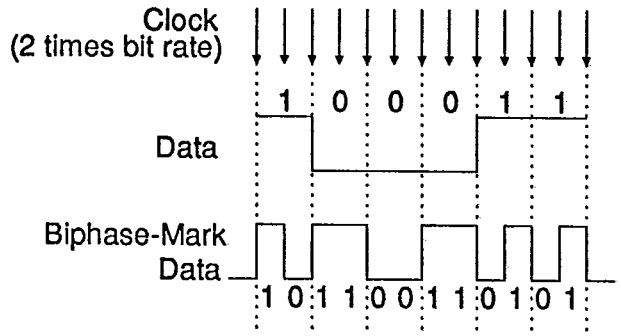


Figure A3. Biphase-Mark Encoding

Each sub-frame starts with a preamble. This allows a receiver to lock on to the data within one sub-frame. There are three defined preambles: one for each channel and one to indicate the beginning of a channel status block (which is also channel A). To distinguish the preambles from arbitrary data patterns, the preambles contain two biphase-mark violations. Biphase-mark data is required to transition at every bit period, but each preamble violates that requirement twice. In figure A3 each bit boundary, indicated by the dashed lines, contains a transition in the biphase data. Each preamble shown in figure A4 has two bit boundaries with no transition, which

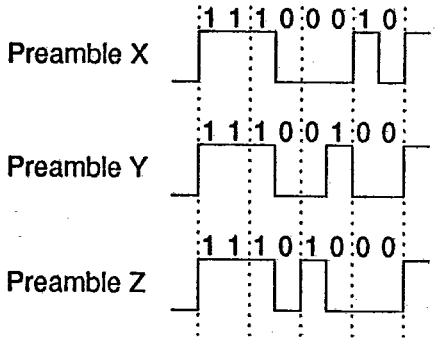


Figure A4. Preamble Forms

enables the receiver to recognize the data as a preamble. Table A1 lists the preamble biphase-mark data patterns and what each designates. Since biphase-mark encoding is not polarity conscious, both phases are shown in the table. Preambles "X" and "Y" indicate a sub-frame containing channels A and B respectively. Preamble "Z" replaces preamble "X" once every 192 frames to indicate the start of a channel

	Biphase Patterns	Channel
X	11100010 or 00011101	Ch. A
Y	11100100 or 00011011	Ch. B
Z	11101000 or 00010111	Ch. A & C.S. Block Start

Table A1. Preambles

status block.

Their are two channel status blocks, one for channel A and one for channel B. Since there are 192 frames in a block, each channel has a channel status block 192 bits long. These 192 channel status bits in a block can be arranged as 24 bytes. The blocks have one of two formats, professional or consumer. The first bit of the channel status block defines the format with 0 indicating consumer and 1 indicating professional.

Channel Status Block - Professional Format

Setting the first bit of channel status high designates the professional or broadcast format. The channel status block structure for the professional format is illustrated in figure A5 and shows bit 0 of byte 0, PRO, to contain a one. Table A2 lists the bits in each byte and their meaning. The areas designated "reserved" in the figures and tables, are currently not specified and must be set to 0 when transmitting. Most of the professional format data was obtained from the AES3-1985 document, and information from AES3-199x which has not received approval as of the printing of this data sheet. Since the AES specification is currently being upgraded, the accuracy of this data is not guaranteed.

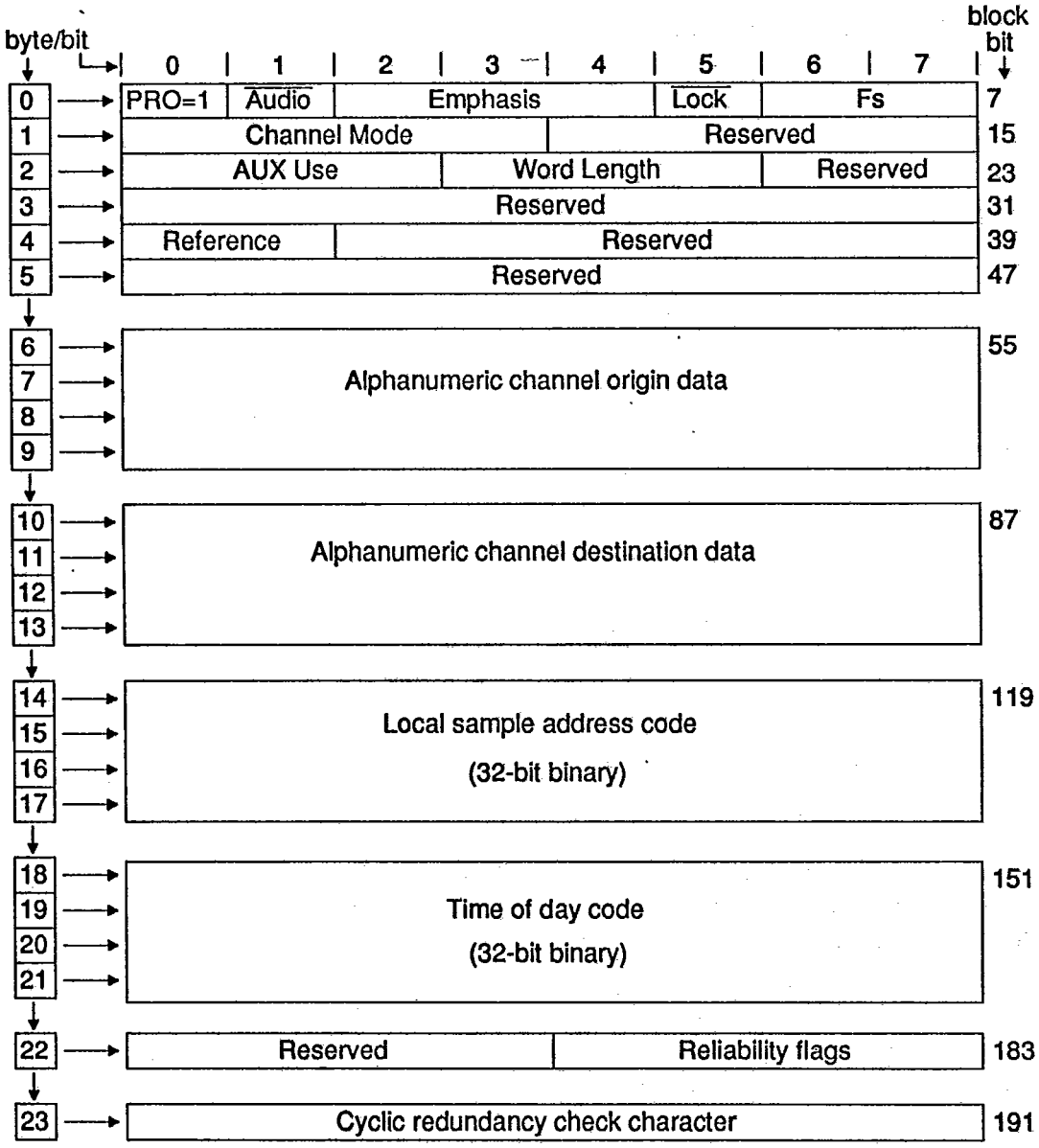


Figure A5. Professional Channel Status Block Structure

BYTE 0	
bit 0	PRO = 1
0	Consumer use of channel status block
1	Professional use of channel status block
bit 1	$\overline{\text{Audio}}$
0	Normal Audio
1	Non-Audio
bits 2 3 4	Encoded audio signal emphasis
0 0 0	Emphasis not indicated. Receiver defaults to no emphasis with manual override enabled
1 0 0	None. Rec. manual override disabled
1 1 0	50/15 µS. Rec. manual override disabled
1 1 1	CCITT J.17 . Rec. man. override disabled
X X X	All other states of bits 2-4 are reserved
bit 5	$\overline{\text{Lock}}$: Source Sample Frequency
0	Locked - default
1	Unlocked
bits 6 7	Fs: Sample Frequency
0 0	Not indicated. Receiver default to 48 kHz and manual override or auto set enabled
0 1	48 kHz. Man. override or auto disabled
1 0	44.1 kHz. Man. override or auto disabled
1 1	32 kHz. Man. override or auto disabled

BYTE 1	
bits 0 1 2 3	Channel Mode
0 0 0 0	Mode not indicated. Receiver default to 2-channel mode. Manual override enabled
0 0 0 1	Two-channels. Man. override disabled
0 0 1 0	Single channel. Man. override disabled
0 0 1 1	Primary/Secondary (Ch. A is primary). Manual override disabled
0 1 0 0	Stereophonic. (Ch. A is left) Manual override disabled.
† 0 1 0 1	Reserved for user defined applications
† 0 1 1 0	Reserved for user defined applications
1 1 1 1	Vector to byte 3. Reserved
X X X X	All other states of bits 0-3 are reserved.
bits 4 5 6 7	Encoded user bits management
X X X X	Reserved.

BYTE 2		
bits 0 1 2	AUX: Use of auxiliary sample bits	
0 0 0	Not defined. Maximum audio word length is 20 bits	
0 0 1	Used for main audio. Maximum audio word length is 24 bits	
† 0 1 0	Used for voice channel. Max. audio word length is 20 bits	
X X X	All other states of bits 0-2 are reserved	
bits 3 4 5	Source word length Max. audio based on bits 0-2 above	
	Max audio 24 bits	Max audio 20 bits
† 0 0 0	24 bits	20 bits (default)
† 0 0 1	23 bits	19 bits
† 0 1 0	22 bits	18 bits
† 0 1 1	21 bits	17 bits
† 1 0 0	20 bits	16 bits
X X X	All other states of bits 3-5 are reserved	
bits 6 7		
X X	Reserved	

Table A2-1. Professional Channel Status Bytes 0-2

BYTE 3	
bits 0-7	Vectored target byte
XXXXXXX	Reserved

BYTE 4	
bits 0 1	Digital audio reference signal per AES11-1990
† 0 0	Default
† 0 1	Grade 1 reference signal
† 1 0	Grade 2 reference signal
† 1 1	Reserved
bits 2-7	
XXXXXX	Reserved

BYTE 5	
bits 0-7	
XXXXXXX	Reserved

BYTES 6 - 9
Alphanumeric channel origin data
7-bit ISO 646 (ASCII) data with odd parity bit. First character in message is byte 6. LSB's are transmitted first.

BYTES 10 - 13
Alphanumeric channel destination data
7-bit ISO 646 (ASCII) data with odd parity bit. First character in message is byte 10. LSB's are transmitted first.

BYTES 14 - 17
Local sample address code (32-bit binary)
Value is of first sample of current block. LSBs are transmitted first.

BYTES 18 - 21
Time-of-day sample address code (32-bit binary)
Value is of first sample of current block. LSBs are transmitted first.

BYTE 22	
bits 0 1 2 3	
X X X X	Reserved
bit 4	Channel status bytes 0 to 5
0	Reliable
1	Unreliable
bit 5	Channel status bytes 6 to 13
0	Reliable
1	Unreliable
bit 6	Channel status bytes 14 to 17
0	Reliable
1	Unreliable
bit 7	Channel status bytes 18 to 21
0	Reliable
1	Unreliable

BYTE 23
CRCC: Cyclic redundancy check character
CRCC for channel status data block that uses bytes 0 to 22 inclusive. Generating polynominal is $G(x) = X^8 + X^4 + X^3 + X^2 + 1$ with an initial state of all ones.

† - Data from draft of AES3-199x. Has not received approval yet.

Table A2-2. Professional Channel Status Bytes 3-23

Channel Status Block - Consumer Format

Setting the first bit of channel status low designates the consumer format. The channel status block structure for the consumer format is illustrated in figure A6 with the bit descriptions in table A3. All areas listed as "reserved" must be transmitted as a 0. The data for this format was obtained from the EIAJ CP-340 and the IEC 958 with some information from TC84 which is a proposed amendment to IEC 958 and has not received approval yet. As with the professional format, since this format is currently changing, the accuracy of the data listed cannot be guaranteed.

In the consumer format, the first byte is always defined. Bit 0 must be 0. If bit 1 is set to 1 defining the data as non-audio, then bits 3-5 are redefined (see table A3, byte 0). Bits 6 and 7 of byte 0 define the mode, and only one mode is presently defined, mode = 00. This mode defines the next three bytes as listed in figure A6. Most of byte 1 defines the category code. The first 3 to 5 bits define the general category. Under the laser-optical category is compact disk (cat. code 1000000). This format defines some of the U channel bits and the CD subcode port. More information can be obtained from the CP-340 or IEC-958 documents.

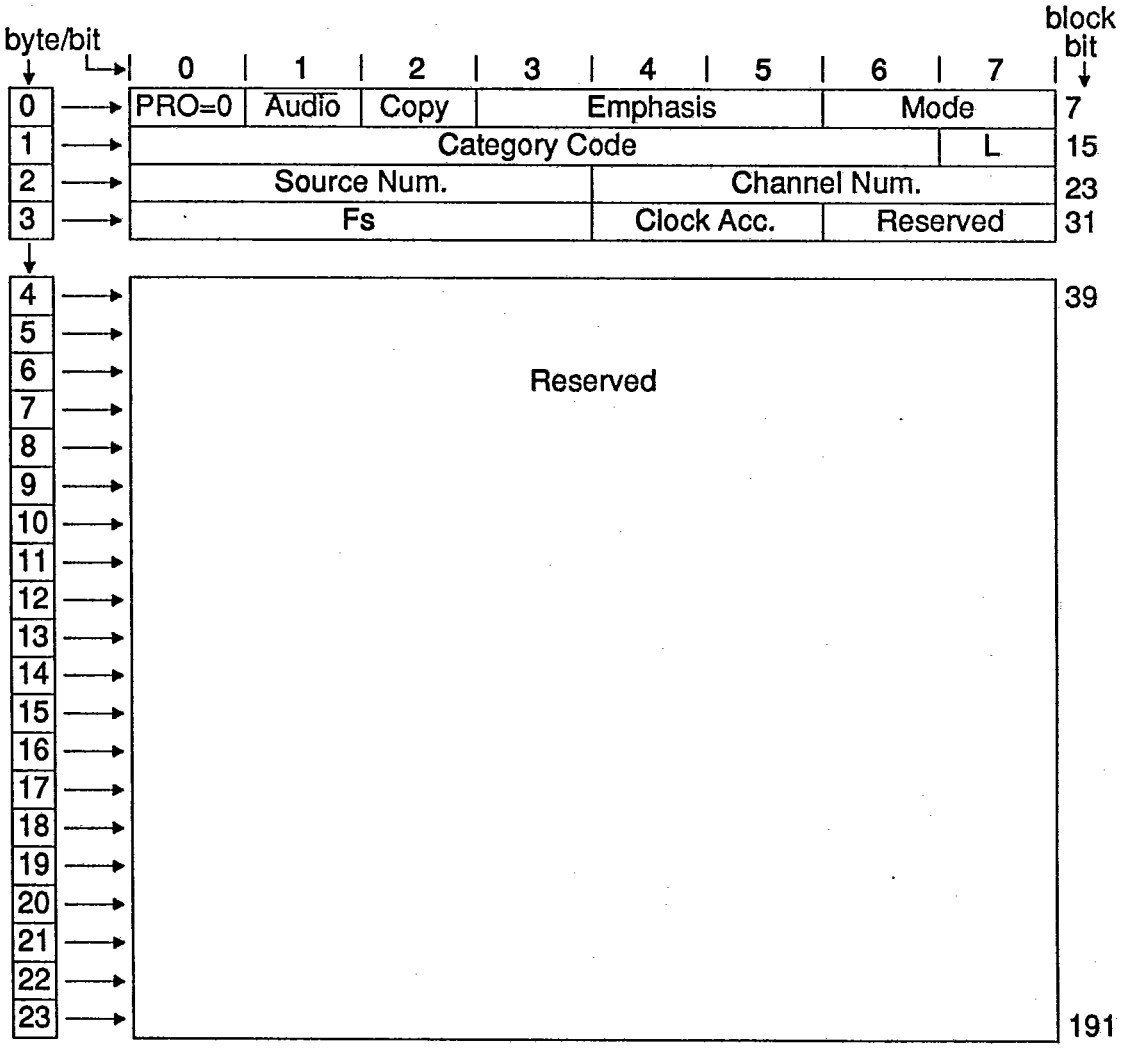


Figure A6. Consumer Channel Status Block Structure

BYTE 0	
bit 0	PRO = 0 (consumer)
0	Consumer use of channel status block
1	Professional use of channel status block
bit 1	$\overline{\text{Audio}}$
0	Digital Audio
1	Non-audio
bit 2	Copy / Copyright
0	Copy inhibited / copyright asserted
1	Copy permitted / copyright not asserted
bits 3 4 5	Pre-emphasis - if bit 1 is 0 (dig. audio)
0 0 0	None - 2 channel audio
1 0 0	50/15 µs - 2 channel audio
0 1 0	Reserved - 2 channel audio
1 1 0	Reserved - 2 channel audio
X X 1	Reserved - 4 channel audio
bits 3 4 5	if bit 1 is 1 (non-audio)
0 0 0	Digital data
X X X	All other states of bits 3-5 are reserved
bits 6 7	Mode
0 0	Mode 0 (defines bytes 1-3)
X X	All other states of bits 6-7 are reserved

BYTE 1 - Category Code 001	
bits 3 4 5 6	Broadcast reception of digital audio
* 0 0 0 0	Japan
* 0 0 1 1	United States
* 1 0 0 0	Europe
* 0 0 0 1	Electronic software delivery
X X X X	All other states are reserved

BYTE 1 - Category Code 100	
bits 3 4 5 6	Laser Optical
0 0 0 0	CD - compatible with IEC-908
* 1 0 0 0	CD - not comp. with IEC-908 (magneto-optical)
X X X X	All other states are reserved

BYTE 1	
bits 0 1 2 3	4 5 6 Category Code
0 0 0 0	0 0 0 General
*	0 0 1 Experimental
	X X X Reserved
* 0 0 0 1	X X X Solid state memory
* 0 0 1 X	X X X Broadcast recep. of digital audio
0 1 0 X	X X X Digital/digital converters
* 0 1 1 0	0 X X A/D converters w/o copyright
*	1 X X A/D converters w/ copyright (using Copy and L bits)
* 0 1 1 1	X X X Broadcast recep. of digital audio
1 0 0 X	X X X Laser-optical
* 1 0 1 X	X X X Musical Instruments, mics, etc.
1 1 0 X	X X X Magnetic tape or disk
1 1 1 X	X X X Reserved
bit 7	L: Generation Status.
	Only category codes: 001XXXX, 0111XXX, 100XXXX
* 0	Original/Commercially pre-recorded data
* 1	No indication or 1st generation or higher
	All other category codes
* 0	No indication or 1st generation or higher
* 1	Original/Commercially pre-recorded data
The subgroups under the category code groups listed above are described in tables below. Those not listed are reserved.	
The Copy and L bits form a copy protection scheme for original works. Further explanations can be found in the proposed amendment (TC84) to IEC-958.	

BYTE 1 - Category Code 010	
bits 3 4 5 6	Digital/digital conv. & signal processing
0 0 0 0	PCM encoder/decoder
* 0 0 1 0	Digital sound sampler
* 0 1 0 0	Digital signal mixer
* 1 1 0 0	Sample-rate converter
X X X X	All other states are reserved

Table A3-1. Consumer Channel Status Bytes 0 and 1

Currently the standards committees are trying to define a minimum implementation as well as levels of implementation of channel status data.

A scheme for providing copy protection is also currently being developed. It includes knowing the category code and then utilizing the Copy and L bits to determine if a copy should be allowed. Digital processing of data should pass through the copy and L bits as defined by their particular category code. If mixing inputs, the highest level of protection of any one of the sources should be passed through. If the copy bit indicates no copy protection (copy = 1), then multiple copies can be made. If recording audio data to tape or disk, and any source has copy protection asserted, then the L bit must be used to determine whether the data can be recorded.

The L bit determines whether the source is an original (or prerecorded) work, or is a copy of an original work (first generation or higher). The actual meaning of the L bit can only be determined by looking at the category code since certain category codes reverse the meaning.

If the category code is CD (1000000) and the copy bit alternates at a 4 to 10 Hz rate, the CD is a copy of an original work that has copy protection asserted and no recording is permitted.

BYTE 1 - Category Code 101		
bits	3 4 5 6	Musical Instruments, mics, etc.
*	0 0 0 0	Synthesizer
*	1 0 0 0	Microphone
	X X X X	All other states are reserved

BYTE 2		
bit	0 1 2 3	Source Number
	0 0 0 0	Unspecified
	1 0 0 0	1
	0 1 0 0	2
	1 1 0 0	3
	0 0 1 0	4 to
	0 1 1 1	14 (binary - 0 is LSB, 3 is MSB)
	1 1 1 1	15
bit	4 5 6 7	Channel Number
	0 0 0 0	Unspecified
	1 0 0 0	A (Left in 2 channel format)
	0 1 0 0	B (Right in 2 channel format)
	1 1 0 0	C to
	0 1 1 1	N (binary - 4 is LSB, 7 is MSB)
	1 1 1 1	O

BYTE 1 - Category Code 110		
bits	3 4 5 6	Magnetic tape or disk
	0 0 0 0	DAT
*	1 0 0 0	Digital audio sound VCR
	X X X X	All other states are reserved

BYTE 3		
bits	0 1 2 3	Fs: Sample Frequency
	0 0 0 0	44.1 kHz
	0 1 0 0	48 kHz
	1 1 0 0	32 kHz
	X X X X	All other states of bits 0-3 are reserved
bits	4 5	Clock Accuracy
	0 0	Level II, ±1000 ppm (default)
	0 1	Level III, variable pitch
	1 0	Level I, ±50 ppm - high accuracy
	1 1	Reserved
bits	6 7	
	X X	Reserved

BYTES 4 - 23
Reserved

* - Data from draft of IEC 958 proposed amendment (from TC84). Has not received approval yet.

Table A3-2. Consumer Channel Status Bytes 1-23

Appendix B: RS422 Driver Information

The RS422 drivers on the CS8401 and CS8402 are designed to drive both the professional and consumer interfaces. The AES/EBU specification for professional/broadcast use calls for a 110Ω source impedance and a balanced drive capability. Since the transmitter impedance is very low, a 110Ω resistor should be placed in series with one of the transmit pins. (A 110Ω resistor in parallel with the transformer would, with the receiver impedance of 110Ω, provide a 55Ω load to the part which is too low.) The specifications call for a balanced output drive of 3-10 volts peak-to-peak into a 110Ω load with no cable attached. Using the circuit in figure B1, the output of the transformer is short-circuit protected, has the proper source impedance, and provides a 5 volt peak-to-peak signal into a 110Ω load. Lastly, the two output pins should be attached to an XLR connector with male pins and a female shell, and with pin 1 of the connector grounded.

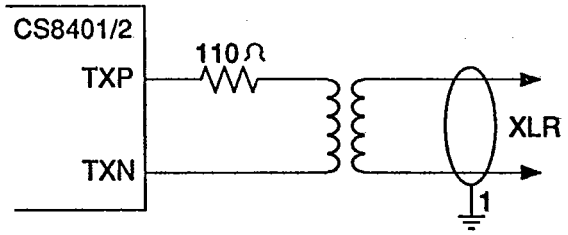


Figure B1. Professional Output Circuit

In the case of consumer use, the specifications call for an unbalanced drive circuit with an output impedance of 75Ω and a output drive level of 0.5 volts peak-to-peak ±20% when measured across a 75Ω load using no cable. The circuit shown in figure B2 only uses the TXP pin and provides the proper output impedance and drive level using standard 1% resistors. The connector for consumer would be an RCA phono socket. This circuit is also short circuit protected.

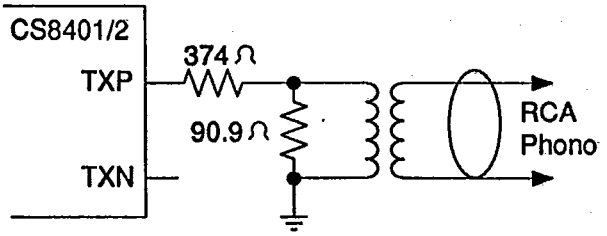


Figure B2. Consumer Output Circuit

The transformer should be capable of operating from 1.5 to 7 MHz, which is the audio data rate of 25 kHz to 55 kHz after biphase-mark encoding. The following are two typical transformers:

Schott Corporation
1000 Parkers Lane Rd.
Wayzata, MN 55391
(615) 889-8800
Part Number: 67125450

Pulse Engineering
Telecom Products Group
7250 Convoy Ct.
San Diego, CA 92111
(619) 268-2400
Part Number: PE65612

Some specifications are listed in figure B3 for convenience; however, the actual specs. should be obtained from the manufacturer to guarantee accuracy.

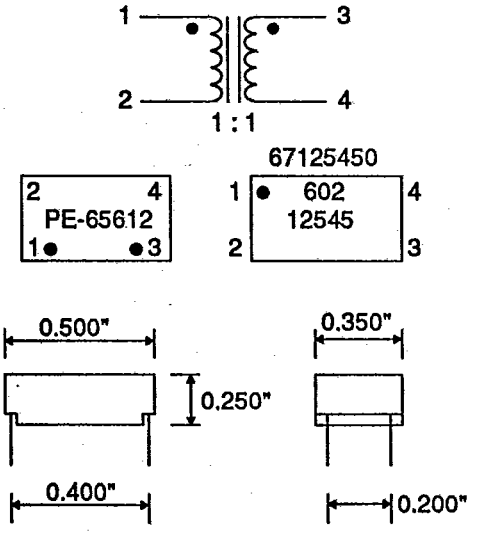


Figure B3. Typical AES/EBU Line Transformers

Optical Connectors

The AES/EBU specifications do not currently address optical connectors. The CS8401 and CS8402 can drive LEDs by using only one of driver pins, either TXP or TXN, and the appropriate current limiting resistor. Each pin is driven from 0 to 5 volts and is capable of driving at least 30 mA. Many fiber optic connectors contain driver modules that have TTL compatible inputs. For these modules, one of the driver pins would be connected directly to connector input. The fiber optic transmitter must have a bandwidth of 6 to 7 MHz.

The Electronic Industry Association of Japan, EIAJ does mention optical connectors in their CP-340 specification. The actual specification that addresses optical connectors is the EIAJ RC-5720 titled *Connectors for Optical Fiber Cables for Digital Audio Equipment.* A manufacturer for these connectors is Toshiba Corp from their TOSLINK™ line of fiber optic connectors. Their connectors are modules that have TTL compatible inputs so the TXP (or TXN) pin would be connected directly to the module. As of the printing of this data sheet, these parts were difficult to obtain in the United States. The following are the part numbers:

TOTX174 - Transmitting Module
TORX174 - Receiving Module
TOCP174 - Optical Fiber w/ Connectors.

Appendix C: MCK and FSYNC Relationship

FSYNC should be derived either directly or indirectly from MCK. The indirect case could be a DSP, providing FSYNC through its serial port, using the same master oscillator that generates MCK. In either case, FSYNC's relationship to MCK is fixed and does not move. Since this appendix provides information on what would happen if FSYNC did move with respect to MCK, it does not apply to the majority of users.

All internal timing is derived from MCK. On the CS8402, MCK is always 128×Fs. On the CS8401, the external MCK is programmable and is initially divided to 128×Fs before being used by the part. The internal clock IMCK used in the following discussion is always 128×Fs regardless of the external MCK pin.

After $\overline{RST}$, the CS8401 and CS8402 synchronize the internal timing to the audio data port, more specifically FSYNC, to guarantee that channel A is left channel data and channel B is right channel data as per the AES/EBU specification. If FSYNC moves with respect to IMCK, the transmitter could lose synchronization, which causes an internal reset.

Figure C1 shows the structure of the serial port input, to the transmitter output. The audio data is serially shifted into R1. PLD is an internal signal that parallel loads R1 into the R2 buffer, and, at the same time, the C, U, and V bits are latched. On the CS8401, the C, U, and V bits are held in RAM, whereas on the CS8402, they are latched from external pins. The PLD signal rises on the first SCK edge that can latch data. This is coincident with the latching of the MSB of audio data in MSB-first, left-justified modes. PLD stays high for one SCK period. In the CS8402 section, the arrows on SCK in figure 16 indicate when PLD goes high. Also, SBC in the CS8402 CD submode is an external version of PLD gated by the SBF input.

When the part is finished transmitting the preamble of a sub-frame, the internal signal LDS rises to parallel-load R2 into R3 for transmission. After $\overline{RST}$, the part synchronizes the audio port to IMCK as shown in figure C2. Since PLD is based on FSYNC and LDS is based on IMCK, if FSYNC moves with respect to IMCK until PLD and LDS occur at the same time, the data would not be properly loaded into R3. If LDS and PLD overlap, an internal reset is initiated causing the timing to return to the initial state shown in figure C2.

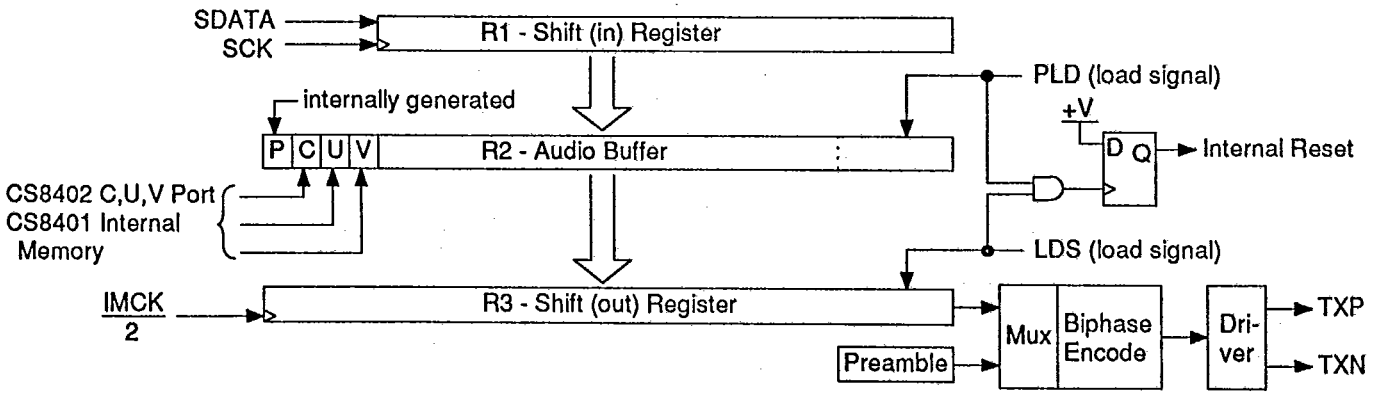


Figure C1. Serial Port-to-Transmitter Block Diagram

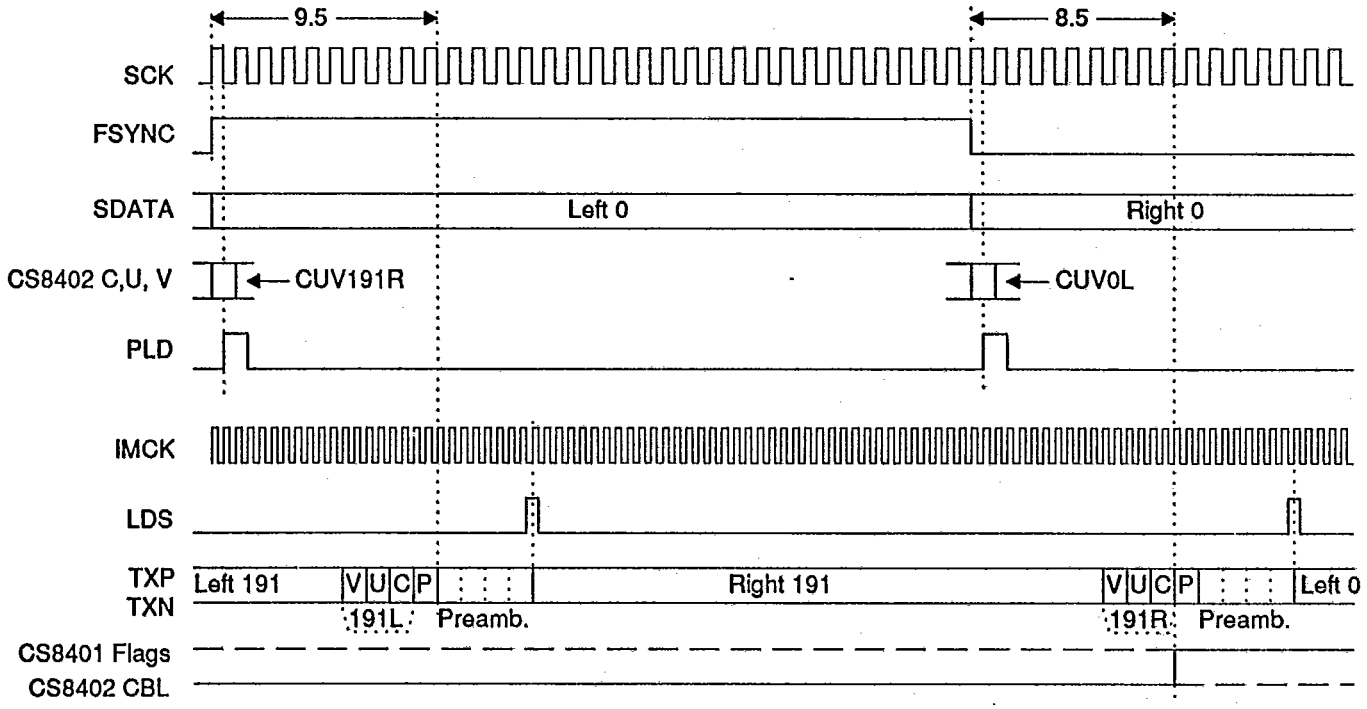


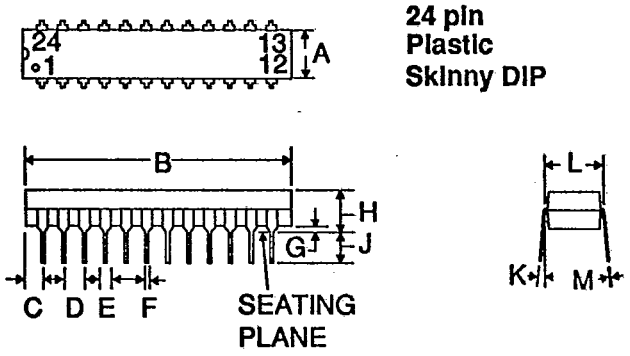
Figure C2. Serial Ports-to-Transmitter Timing

Ordering Guide

Model	Temperature Range	Package
CS8401-CP	0 to 70 °C*	24-Pin Plastic DIP
CS8401-IP	-40 to 85 °C	24-Pin Plastic DIP
CS8401-CS	0 to 70 °C*	24-Pin Plastic SOIC
CS8401-IS	-40 to 85 °C	24-Pin Plastic SOIC
CS8402-CP	0 to 70 °C*	24-Pin Plastic DIP
CS8402-IP	-40 to 85 °C	24-Pin Plastic DIP
CS8402-CS	0 to 70 °C*	24-Pin Plastic SOIC
CS8402-IS	-40 to 85 °C	24-Pin Plastic SOIC

* Although the '-CP' and '-CS' suffixed parts are guaranteed to operate over 0 to 70 °C, they are tested at 25 °C only. If testing over temperature is desired, the '-IP' and '-IS' suffixed parts are tested over their specified temperature range.

PACKAGE DIMENSIONS

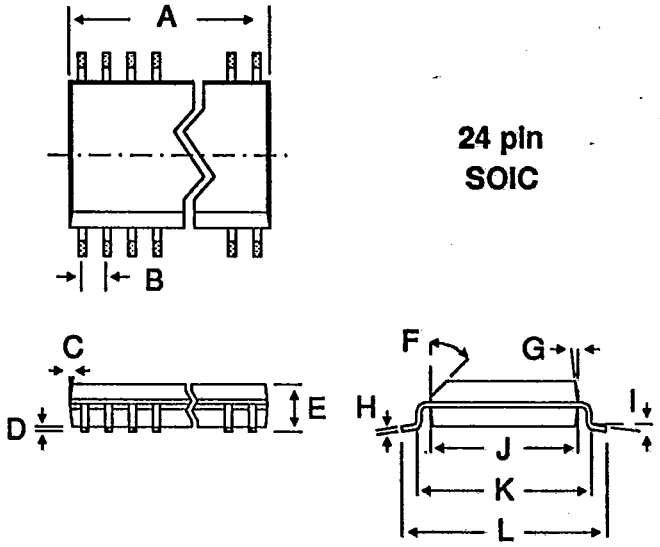


24 pin Plastic Skinny DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin SOIC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.99	15.50	0.590	0.610
B	1.27 BSC		0.050 BSC	
C	7° NOM		7° NOM	
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420