FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13741-1E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90945 Series

MB90F947, MB90F949, MB90V390H

■ DESCRIPTION

The MB90945 series with one FULL-CAN* interface and FLASH ROM is especially designed for automotive HVAC applications. Its main feature is the on board CAN* Interface, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal FULL-CAN* approach. With the new 0.35 µm CMOS technology, Fujitsu now offers on-chip FLASH-ROM program memory up to 512 K bytes. An internal voltage booster removes the necessity for a second programming voltage.

An on board voltage regulator provides 3 V to the internal MCU core. This creates a major advantage in terms of EMI and power consumption.

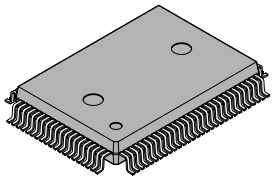
The internal PLL clock frequency multiplier provides an internal 42 ns instruction cycle time from an external 4 MHz clock.

The unit features a 4-channel Output Compare Unit and a 6-channel Input Capture Unit with two separate 16-bit free running timers. 2 UARTs, one Serial I/O and one I²C constitute additional functionality for communication purposes.

* : Controller Area Network (CAN) - License of Robert Bosch GmbH

■ PACKAGE

100-pin Plastic QFP



(FPT-100P-M06)

FUJITSU

■ FEATURES

- 16-bit core CPU; 4 MHz external clock (24 MHz internal, 42 ns instr. cycle time)
- New 0.35 µm CMOS Process Technology
- Internal voltage regulator supports 3 V MCU core, offering low EMI and low power consumption figures
- Phase Modulator for reducing EMI
- One FULL-CAN* interface; conforming to Version 2.0 Part A and Part B, flexible message buffering (mailbox and FIFO buffering can be mixed)
- Powerful interrupt functions (8 progr. priority levels; 8 external interrupts)
- EI^{2}OS - Automatic transfer function independant of CPU; 16 channels of intelligent I/O Services
- 18-bit Time-base counter
- Watchdog Timer
- 1 full duplex UARTs; support 10.4 KBaud (USA standard)
- 1 full duplex UART (LIN/SCI/SPI)
- 1 Serial I/O (SPI)
- 1 I^{2}C
- A/D Converter : 15 channels analog inputs (Resolution 10-bit or 8-bit)
- 16-bit reload timer × 1channel
- ICU (Input capture) 16-bit × 6 channels
- OCU (Output compare) 16-bit × 4 channels
- 16-bit free running timer × 2 channels (FRT0 : ICU 0/1, OCU 0/1/2/3, FRT1 : ICU 2/3/4/5)
- 8/16-bit Programmable Pulse Generator 6 channels × 8/16-bit
- Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
- 4-byte instruction execution queue
- signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
- Program Patch Function (3 address match registers)
- Fast Interrupt processing
- Low Power Consumption mode
  Sleep mode
  Timebase timer mode
  Stop mode
  CPU intermittent mode
- Automotive input levels
- Package : 100-pin plastic QFP

* : Controller Area Network (CAN) - License of Robert Bosch GmbH

■ PRODUCT LINEUP

Parameter \ Part Number	MB90F949	MB90F947	MB90V390H
CPU	F²MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz oscillation clock, PLL cloclk multiplied by 6)		
ROM	Boot-block Flash memory 256 K bytes	Boot-block Flash memory 128 K bytes	External
RAM	12 K bytes	6 K bytes	16 K bytes
Emulator-specific power supply*1	—	—	None
Technology	0.35 µm CMOS with on-chip voltage regulator for internal power supply + Flash memory with on-chip charge pump for programming voltage		0.35 µm CMOS with on-chip voltage regulator for internal power supply
Operating voltage range	3.5 V to 5.5 V : other than conditions listed below 4.0 V to 5.5 V : when writing to Flash 4.5 V to 5.5 V : if A/D Converter is used		5 V ± 10%
Temperature range	–40 °C to +85 °C		—
Package	QFP-100P		PGA-299C
UART0	1 channel		3 channels
	Full duplex double buffer Supports asynchronous/synchronous (with start/stop bit) transfer Baud rate : 4808/9615/10417/19230/38460/62500/500000 bps (asynchronous) 500 K/1 M/2 Mbps (synchronous) at System clock = 20 MHz		
UART3 (LIN/SCI/SPI)	1 channel		
Serial I/O	1 channel Transfer can be started from MSB or LSB Supports internal clock synchronized transfer and external clock synchronized transfer Supports positive-edge and negative-edge clock synchronization Baud rate : 31.25 K/62.5 K/125 K/500 K/1 Mbps at System clock = 20 MHz		
I²C (400 Kbps)	1 channel		
A/D Converter (15 input channels)	10-bit or 8-bit resolution Conversion time : Min 4.9 µs includes sample time (per one channel, only at certain machine clock frequencies)		
16-bit Reload Timer	1 channel		2 channels
	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function		

(Continued)

Parameter \ Part Number	MB90F949	MB90F947	MB90V390H
16-bit I/O Timer (2 channels)	Signals an interrupt when overflowing Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = System clock freq.) I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1, OCU 0/1/2/3 I/O Timer 1 (clock input FRCK1) corresponds to ICU 2/3/4/5		
16-bit Input Capture (6 channels)	Rising edge, falling edge or rising & falling edge sensitive Six 16-bit Capture registers Signals an interrupt upon external event		
	—	—	ICU 3/5 inputs are shared with OCU 6/7 outputs
16-bit Output Compare	4 channels	4 channels	8 channels
	Signals an interrupt when a match with 16-bit I/O Timer Eight 16-bit compare registers. A pair of compare registers can be used to generate an output signal.		
	—	—	ICU 3/5 inputs are shared with OCU 6/7 outputs
8/16-bit Programmable Pulse Generator (6 channels)	Supports 8-bit and 16-bit operation modes Twelve 8-bit reload counters Twelve 8-bit reload registers for L pulse width Twelve 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 102.4 µs (fosc = 5 MHz) (fsys = System clock frequency, fosc = Oscillation clock frequency)		
CAN Interface	1 channel	1 channel	5 channels
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full-bit compare/Full-bit mask/Two partial bit masks Supports up to 1 Mbps		
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive		
Stepping motor controller	—	—	2 channels
Watch Timer	—	—	1 channel
Sound generator	—	—	1 channel
Machine clock output	—	—	2 channels (non-inverted and inverted)

(Continued)

(Continued)

Part Number / Parameter	MB90F949	MB90F947	MB90V390H
Program patch function	3 address match registers	3 address match registers	5 address match registers
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs Bit-wise programmable as input/output or peripheral signal		
	Automotive input level (P21/RX1, P42/SDA, P43/SCL have CMOS Schmitt input level)		Port-wise programmable as Automotive (default) or CMOS Schmitt input level
I/O Ports with 4 mA CMOS output	All ports except P42, P43		All ports except P80, P81, PA0-PA7, P42, P43
I/O Ports with 3 mA CMOS output	P42, P43		P42, P43
I/O Ports with 30 mA CMOS output with slewrate control	—	—	P80, P81, PA0 to PA7
Clock Modulator	Phase modulation mode		Frequency and phase modulation mode
	Reduces EMI by modulating the PLL clock		
Start-up time at power-on reset	3×2^{16} oscillation cycles (49.152 ms at 4 MHz oscillation) + oscillation time of oscillator*2		2^{18} oscillation cycles (65.536 ms at 4 MHz oscillation) + oscillation time of oscillator*2
Flash Memory	Supports automatic programming, Embedded Algorithm™*3 Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 20 years*4 Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory (address $FFA000_H$, mode data 00_H) Boot block configuration Erase can be performed on each block Block protection with external programming voltage Write and erase at F_{max} = 20 MHz		—

*1 : It is setting of Jumper switch SI when Emulation Pod (MB2147) is used.
Please refer to the Emulator hardware manual about details.

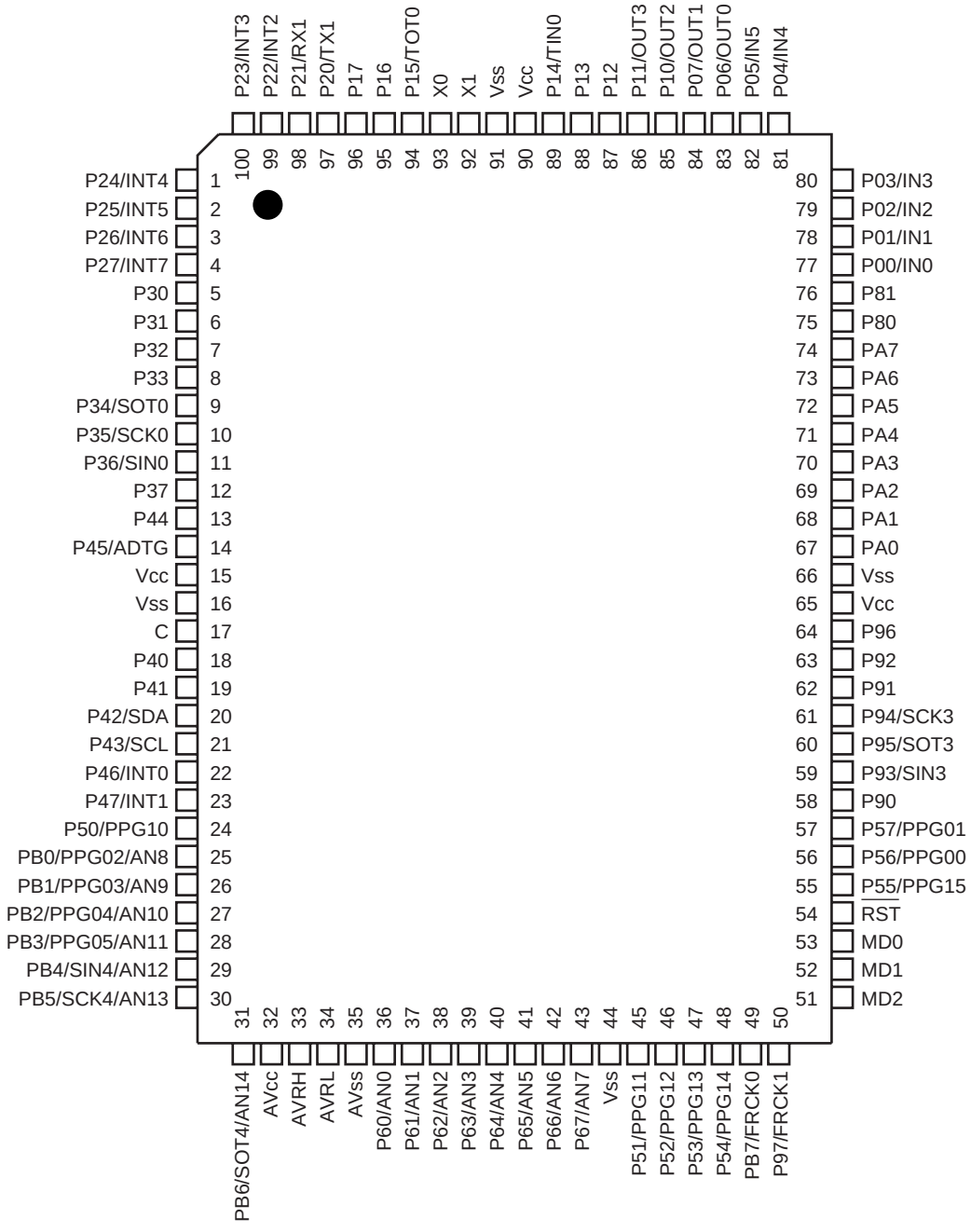
*2 : Oscillation time of the oscillator is the time that the amplitude reaches 90%.

*3 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

*4 : Data is based on reliability tests during process qualification (the value for T_A = + 85 °C is calculated via the Arrenhius formula from data of accelerated measurements at elevated temperature) .

■ PIN ASSIGNMENTS

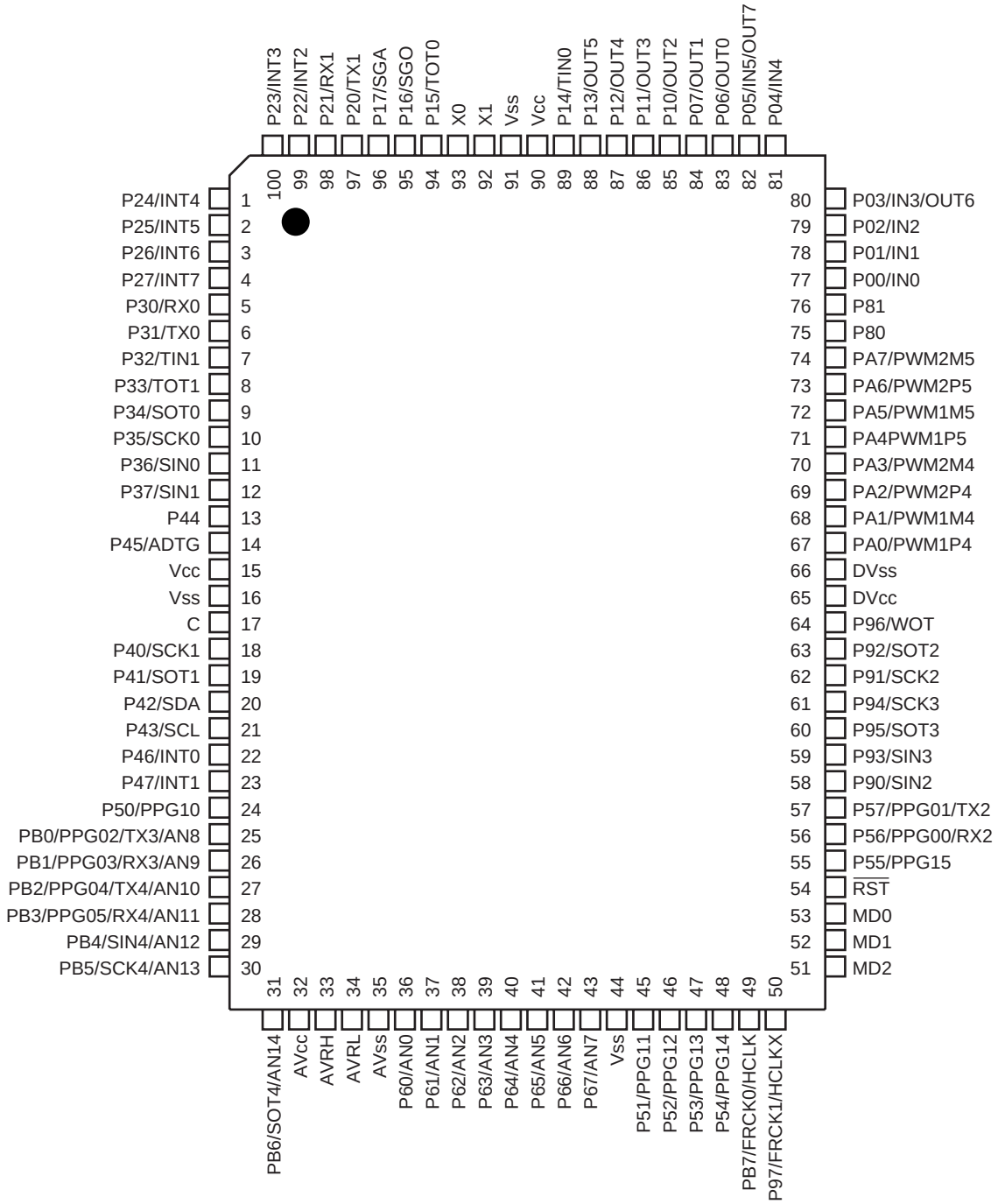
- MB90F947, MB90F949



(FPT-100P-M06)

- MB90V390H

(TOP VIEW)



(FPT-100P-M06)
As seen with QFP100 probe cable

■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Function
92	X1	A	Oscillation output
93	X0		Oscillation input
54	$\overline{RST}$	B	Reset input
77 to 82	P00 to P05	D	General purpose I/O
	IN0 to IN5		Inputs for the Input Captures 0-5
83 to 86	P06, P07 P10, P11	D	General purpose I/O
	OUT0 to OUT3		Outputs for the Output Compares
87, 88	P12, P13	D	General purpose I/O
89	P14	D	General purpose I/O
	TIN0		TIN0 input for the 16-bit Reload Timer 0
94	P15	D	General purpose I/O
	TOT0		TOT0 output for the 16-bit Reload Timer 0
95, 96	P16, P17	D	General purpose I/O
97	P20	D	General purpose I/O
	TX1		TX output for CAN Interface 1
98	P21	F	General purpose I/O
	RX1		RX input for CAN Interface 1
99, 100 1 to 4	P22 to P27	D	General purpose I/O
	INT2 to INT7		External interrupt inputs for INT2 to INT7
5 to 8	P30 to P33	D	General purpose I/O
9	P34	D	General purpose I/O
	SOT0		SOT output for UART 0
10	P35	D	General purpose I/O
	SCK0		SCK input/output for UART 0
11	P36	D	General purpose I/O
	SIN0		SIN input for UART 0
12	P37	D	General purpose I/O
13	P44	D	General purpose I/O
14	P45	D	General purpose I/O
	ADTG		External trigger input of the A/D Converter
18, 19	P40, P41	D	General purpose I/O
20	P42	F	General purpose I/O
	SDA		Serial data for I^2C interface

(Continued)

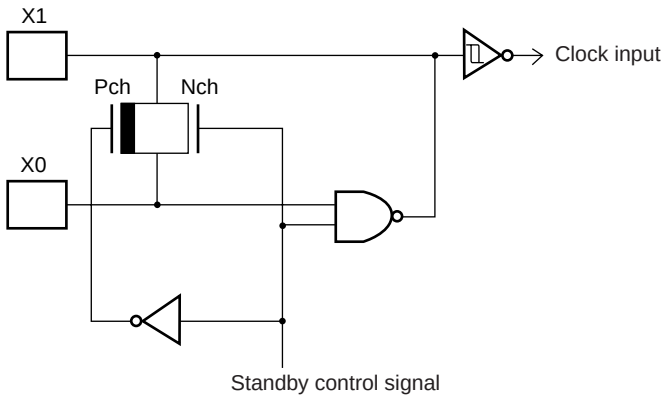
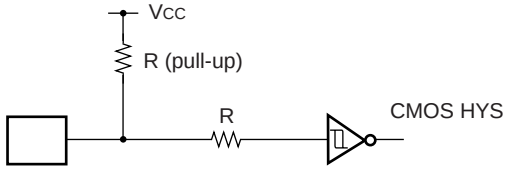
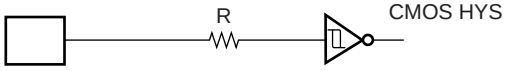
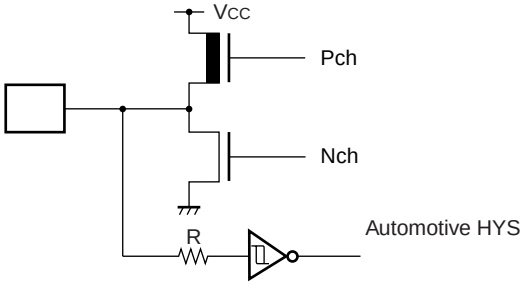
Pin no.	Pin name	Circuit type	Function
21	P43	F	General purpose I/O
	SCL		Serial clock for I²C interface
22, 23	P46, P47	D	General purpose I/O
	INT0, INT1		External interrupt inputs for INT0 to INT1
24	P50	D	General purpose I/O
	PPG10		Output for the Programmable Pulse Generator
25 to 28	PB0 to PB3	E	General purpose I/O
	PPG02 to PPG05		Outputs for the Programmable Pulse Generators
	AN8 to AN11		Inputs for the A/D Converter
29	PB4	E	General purpose I/O
	SIN4		SIN input for Serial I/O
	AN12		Input for the A/D Converter
30	PB5	E	General purpose I/O
	SCK4		SCK input/output for Serial I/O
	AN13		Input for the A/D Converter
31	PB6	E	General purpose I/O
	SOT4		SOT output for Serial I/O
	AN14		Input for the A/D Converter
36 to 43	P60 to P67	E	General purpose I/O
	AN0 to AN7		Inputs for the A/D Converter
45 to 48	P51 to P54	D	General purpose I/O
	PPG11 to PPG14		Outputs for the Programmable Pulse Generators
49	PB7	D	General purpose I/O
	FRCK0		FRCK0 input for the 16-bit I/O Timer 0
50	P97	D	General purpose I/O
	FRCK1		FRCK1 input for the 16-bit I/O Timer 1
55	P55	D	General purpose I/O
	PPG15		Outputs for the Programmable Pulse Generators
56, 57	P56, P57	D	General purpose I/O
	PPG00, PPG01		Outputs for the Programmable Pulse Generators
58	P90	D	General purpose I/O
59	P93	D	General purpose I/O
	SIN3		SIN input for UART 3 (LIN/SCI/SPI)
60	P95	D	General purpose I/O
	SOT3		SOT output for UART 3 (LIN/SCI/SPI)

(Continued)

(Continued)

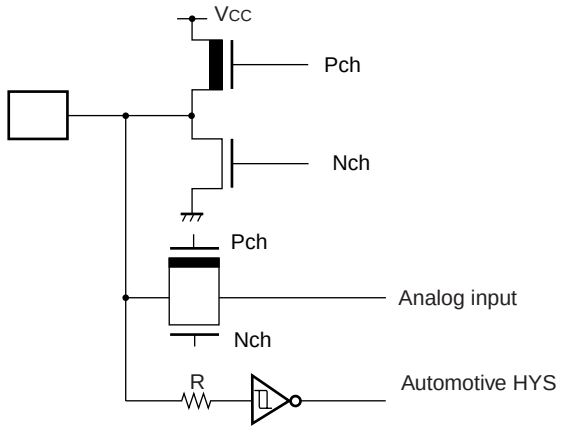
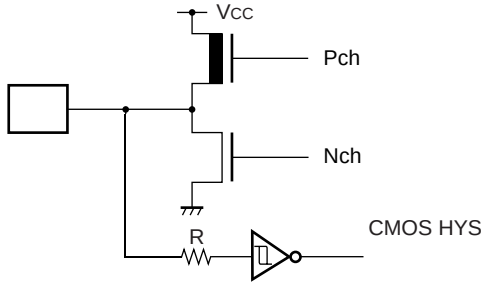
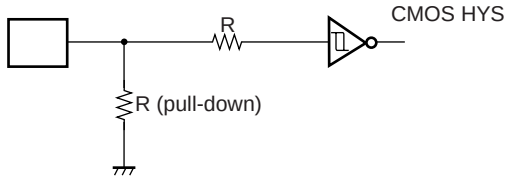
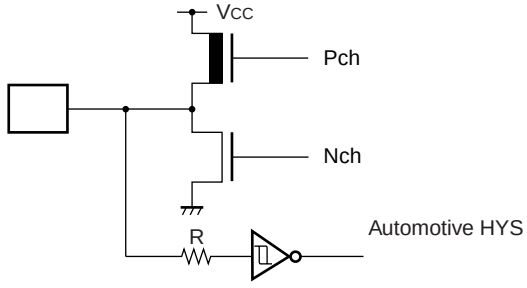
Pin no.	Pin name	Circuit type	Function
61	P94	D	General purpose I/O
	SCK3		SCK input/output for UART 3 (LIN/SCI/SPI)
62, 63	P91, P92	D	General purpose I/O
64	P96	D	General purpose I/O
67 to 74	PA0 to PA7	H	General purpose I/O. For the EVA device, these pins are high current outputs.
75, 76	P80, P81	H	General purpose I/O. For the EVA device, these pins are high current outputs.
32	AV_{CC}	—	Dedicated power supply pin (5 V) for the A/D converter
33	AVRH	—	Dedicated pos. reference voltage pin for the A/D converter
34	AVRL	—	Dedicated neg. reference voltage pin for the A/D converter
35	AVss	—	Dedicated power supply pin (0 V) for the A/D converter
52, 53	MD1, MD0	C	These are input pins used to designate the operating mode. They should be connected directly to V_{CC} or V_{SS}.
51	MD2	G	This is an input pin used to designate the operating mode. It should be connected directly to V_{CC} or V_{SS}.
15 65 90	Vcc	—	These are power supply (5 V) input pins. For the EVA device, pin 65 is the DV_{CC} supply pin for the high current outputs.
16 44 66 91	Vss	—	These are power supply (0 V) input pins. For the EVA device, pin 66 is the DV_{SS} supply pin for the high current outputs.
17	C	—	This is the power supply stabilization capacitor pin. It should be connected to higher than or equal to 0.1 µF ceramic capacitor.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistor : 1 MΩ approx.
B		• CMOS Hysteresis input with pull-up Resistor : 50 kΩ approx.
C		• EVA device : CMOS Hysteresis input • Flash device : CMOS input.
D		• CMOS output (4 mA) • Automotive Hysteresis input

(Continued)

(Continued)

Type	Circuit	Remarks
E		• CMOS output (4 mA) • Automotive Hysteresis input • Analog input
F		• CMOS output P42, P43 : 3mA P21 : 4 mA • CMOS Hysteresis input
G		• EVA device : CMOS Hysteresis input with pull-down Resistor : 50 kΩ approx. • Flash device : CMOS input without pull-down.
H		• EVA device : CMOS high current output (30 mA) with slewrate control • Flash device : CMOS output (4 mA) • Automotive Hysteresis input

■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Stabilization of supply voltage
- Treatment of unused pins
- Using external clock
- Power supply pins (V_{CC}/V_{SS})
- Pull-up/down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter if A/D Converter is unused.
- Notes on Energization
- Caution on Operations during PLL Clock Mode

1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS}.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

In using the devices, take sufficient care to avoid exceeding maximum ratings.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

2. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operation range. Therefore, the V_{CC} supply voltage should be stabilized.

For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak values) at commercial frequencies (50 Hz to 60 Hz) fall below 10 % of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

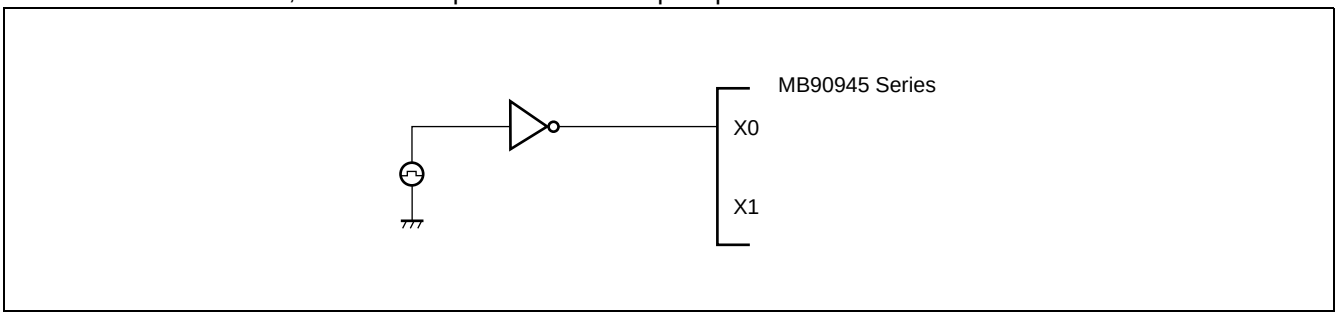
3. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

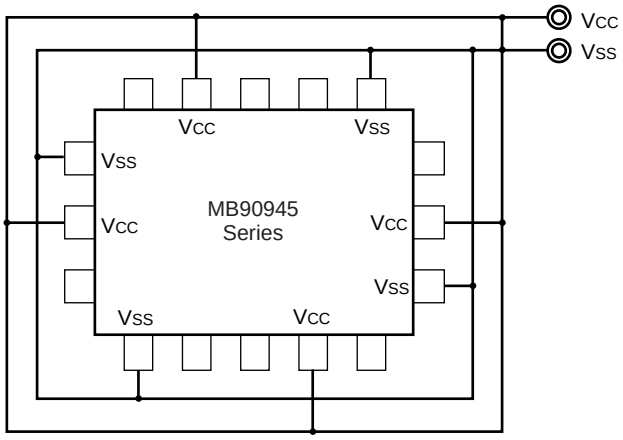
4. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



5. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
- Connect V_{CC} and V_{SS} to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} in the vicinity of V_{CC} and V_{SS} pins of the device.



6. Pull-up/down resistors

The MB90945 Series does not support internal pull-up/down resistors. Use external components where needed.

7. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits while you design a printed circuit.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

8. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN14) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

9. Connection of Unused Pins of A/D Converter if A/D Converter is unused

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

10. Notes on Energization

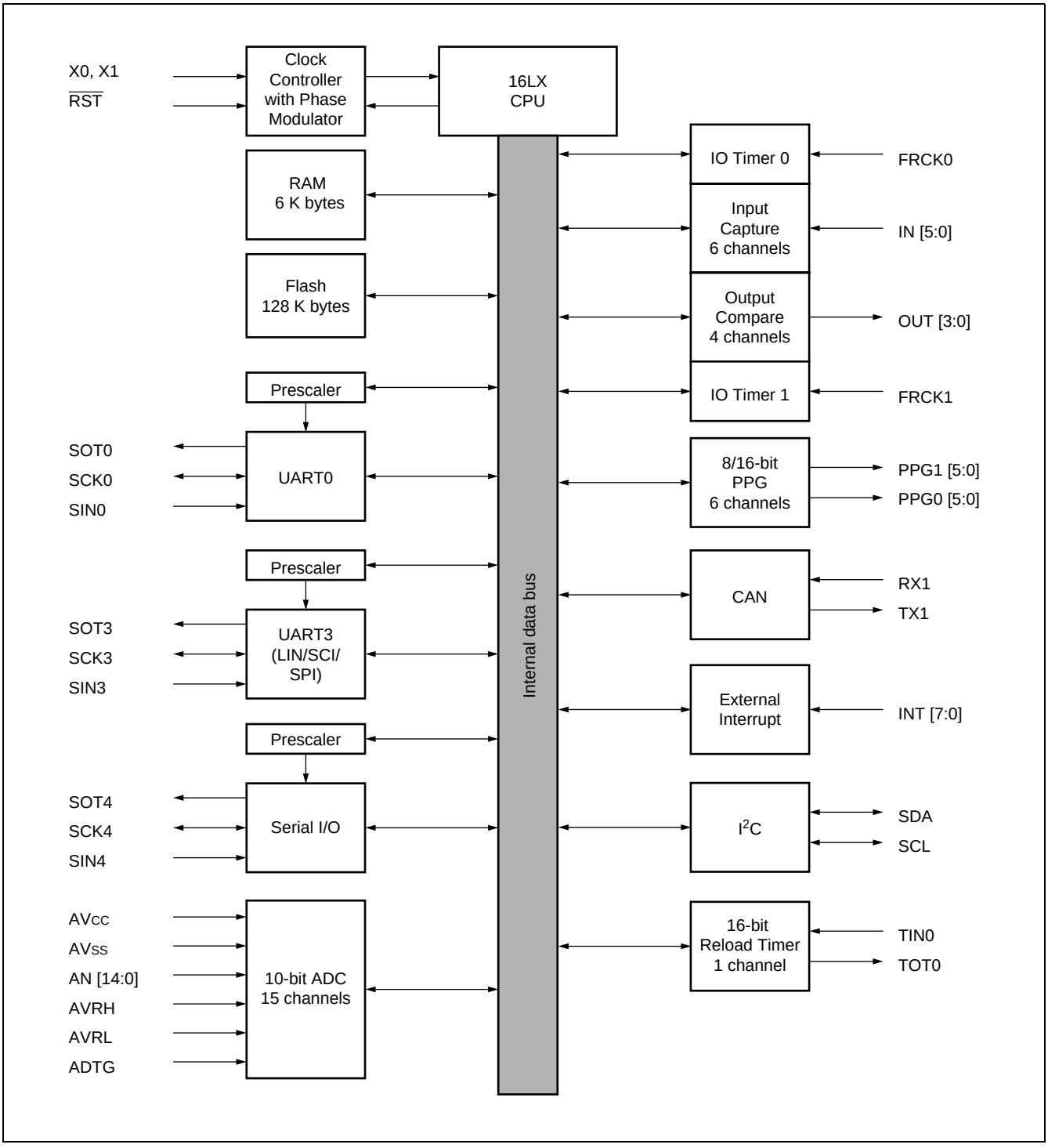
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 or more µs (0.2 V to 2.7 V)

11. Notes on During Operation of PLL Clock Mode

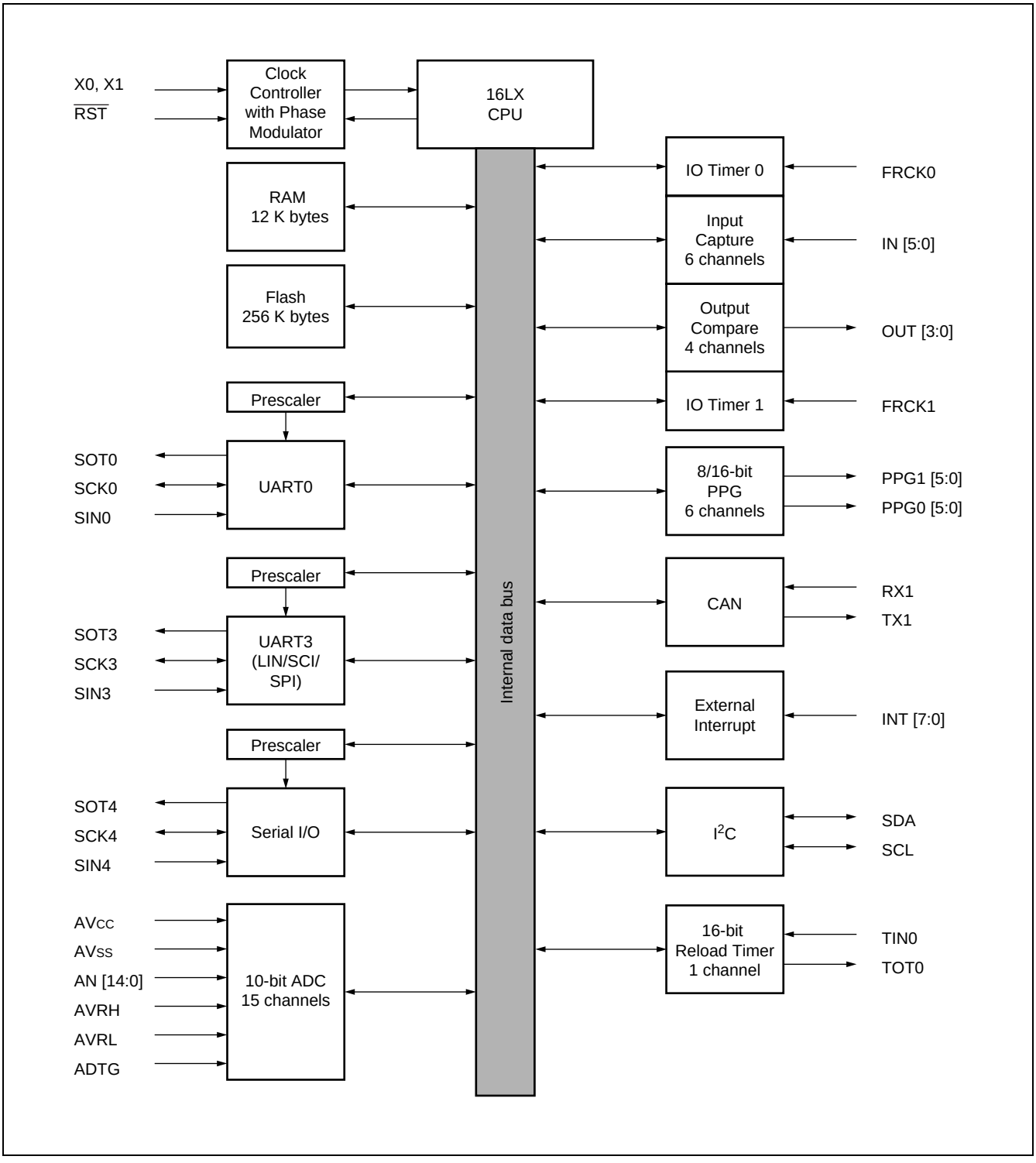
If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

■ BLOCK DIAGRAMS

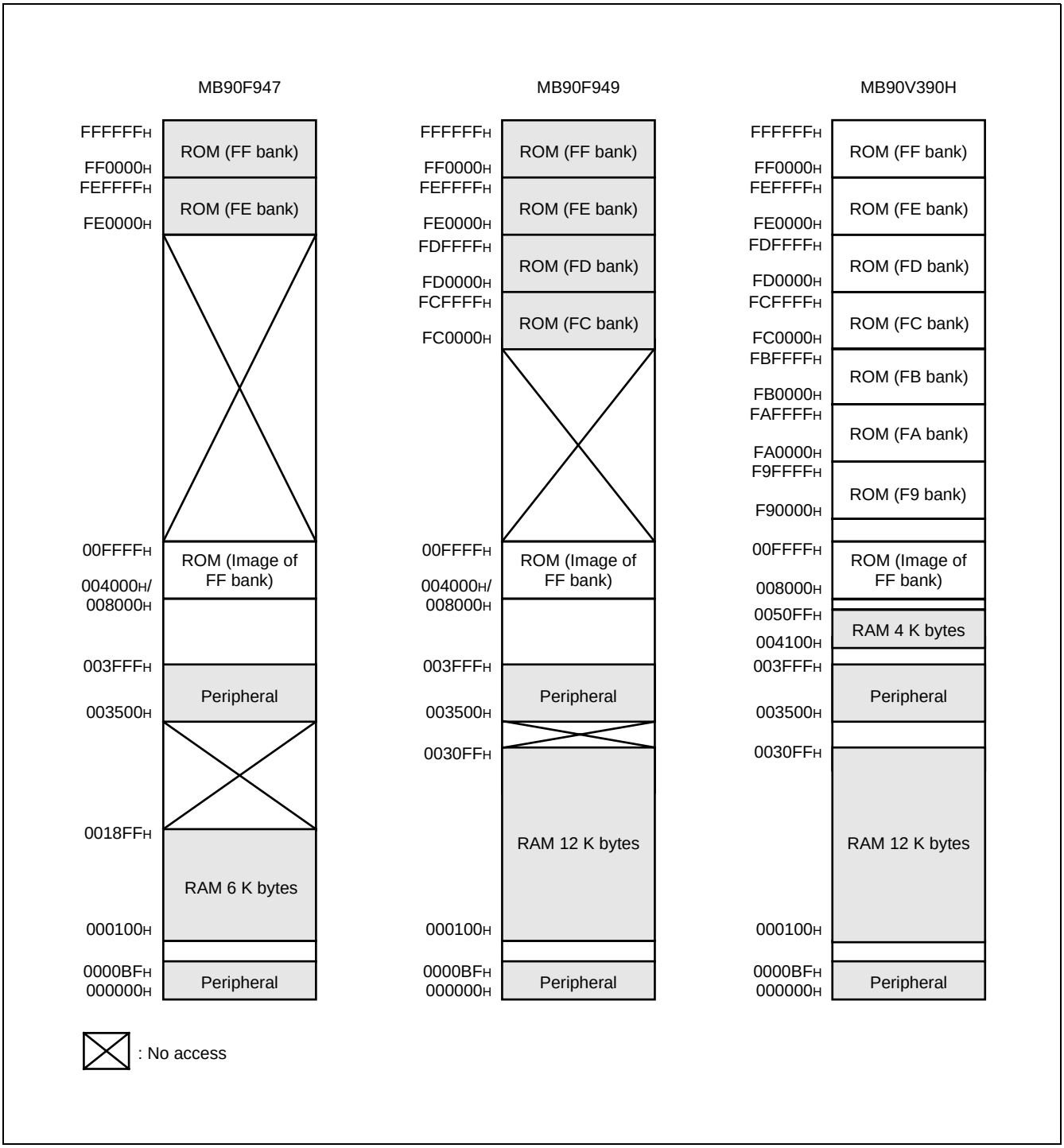
- MB90F947



- MB90F949


X0, X1
RST
Clock Controller with Phase Modulator
16LX CPU
RAM 12 K bytes
Flash 256 K bytes
Prescaler
SOT0
SCK0
SIN0
UART0
Prescaler
SOT3
SCK3
SIN3
UART3 (LIN/SCI/ SPI)
Prescaler
SOT4
SCK4
SIN4
Serial I/O
AVCC
AVSS
AN [14:0]
AVRH
AVRL
ADTG
10-bit ADC 15 channels
Internal data bus
IO Timer 0
FRCK0
Input Capture 6 channels
IN [5:0]
Output Compare 4 channels
OUT [3:0]
IO Timer 1
FRCK1
8/16-bit PPG 6 channels
PPG1 [5:0]
PPG0 [5:0]
CAN
RX1
TX1
External Interrupt
INT [7:0]
I2C
SDA
SCL
16-bit Reload Timer 1 channel
TIN0
TOT0

■ MEMORY MAP



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.
For example, an attempt to access 00C000H accesses the value at FFC000H in ROM.
The ROM area in bank FF exceeds 32/48 K bytes, and its entire image cannot be shown in bank 00.
The image between FF4000H/FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF3FFFH/FF7FFFH is visible only in bank FF.

■ I/O MAP

Address	Register	Abbrevia-tion	Access	Resource name	Initial value
00H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX
01H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX
02H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX
03H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX
04H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX
05H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX
06H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX
07H	Reserved				
08H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX
09H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX
0AH	Port A data register	PDRA	R/W	Port A	XXXXXXXX
0BH	Port B data register	PDRB	R/W	Port B	XXXXXXXX
0CH	Analog Input Enable 0	ADER0	R/W	Port 6, A/D	11111111
0DH	Analog Input Enable 1/ ADC Select	ADER1	R/W	Port B, A/D	01111111
0EH	Input Level Select Register (MB90V390H only)	ILSR	R/W	Ports	00000000
0FH	Input Level Select Register (MB90V390H only)	ILSR	R/W	Ports	00000000
10H	Port 0 direction register	DDR0	R/W	Port 0	00000000
11H	Port 1 direction register	DDR1	R/W	Port 1	00000000
12H	Port 2 direction register	DDR2	R/W	Port 2	00000000
13H	Port 3 direction register	DDR3	R/W	Port 3	00000000
14H	Port 4 direction register	DDR4	R/W	Port 4	00000000
15H	Port 5 direction register	DDR5	R/W	Port 5	00000000
16H	Port 6 direction register	DDR6	R/W	Port 6	00000000
17H	Reserved				
18H	Port 8 direction register	DDR8	R/W	Port 8	XXXXXX00
19H	Port 9 direction register	DDR9	R/W	Port 9	00000000
1AH	Port A direction register	DDRA	R/W	Port A	00000000
1BH	Port B direction register	DDRB	R/W	Port B	00000000
1CH to 1FH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
20H	Serial Mode Control 0	UMC0	R/W	UART0	00000100
21H	Status 0	USR0	R/W		00010000
22H	Input/Output Data 0	UIDR0/ UODR0	R/W		XXXXXXXX
23H	Rate and Data 0	URD0	R/W		0000000X
24H to 2BH	Reserved				
2CH	Serial Mode Control 4	SMCS4	R/W	Serial I/O	XXXX0000
2DH	Serial Mode Control 4	SMCS4	R/W		00000010
2EH	Serial Data 4	SDR4	R/W		XXXXXXXX
2FH	Serial I/O Prescaler/Edge Selector 4	CDCR4	R/W		0X0X0000
30H	External Interrupt Enable	ENIR	R/W	External Interrupt	00000000
31H	External Interrupt Request	EIRR	R/W		XXXXXXXX
32H	External Interrupt Level	ELVR	R/W		00000000
33H	External Interrupt Level	ELVR	R/W		00000000
34H	A/D Control Status 0	ADCS0	R/W	A/D Converter	00000000
35H	A/D Control Status 1	ADCS1	R/W		00000000
36H	A/D Data 0	ADCR0	R		XXXXXXXX
37H	A/D Data 1	ADCR1	R/W		000000XX
38H	PPG0 operation mode control register	PPGC0	R/W	16-bit Programable Pulse Generator 0/1	0X000XX1
39H	PPG1 operation mode control register	PPGC1	R/W		0X000001
3AH	PPG0 and PPG1 clock select register	PPG01	R/W		000000XX
3BH	Reserved				
3CH	PPG2 operation mode control register	PPGC2	R/W	16-bit Programable Pulse Generator 2/3	0X000XX1
3DH	PPG3 operation mode control register	PPGC3	R/W		0X000001
3EH	PPG2 and PPG3 clock select register	PPG23	R/W		000000XX
3FH	Reserved				
40H	PPG4 operation mode control register	PPGC4	R/W	16-bit Programable Pulse Generator 4/5	0X000XX1
41H	PPG5 operation mode control register	PPGC5	R/W		0X000001
42H	PPG4 and PPG5 clock select register	PPG45	R/W		000000XX
43H	Reserved				
44H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programable Pulse Generator 6/7	0X000XX1
45H	PPG7 operation mode control register	PPGC7	R/W		0X000001
46H	PPG6 and PPG7 clock select register	PPG67	R/W		000000XX
47H	Reserved				

(Continued)

Address	Register	Abbrevia-tion	Access	Resource name	Initial value
48H	PPG8 operation mode control register	PPGC8	R/W	16-bit Programable Pulse Generator 8/9	0X000XX1
49H	PPG9 operation mode control register	PPGC9	R/W		0X000001
4AH	PPG8 and PPG9 clock select register	PPG89	R/W		000000XX
4BH	Reserved				
4CH	PPGA operation mode control register	PPGCA	R/W	16-bit Programable Pulse Generator A/B	0X000XX1
4DH	PPGB operation mode control register	PPGCB	R/W		0X000001
4EH	PPGA and PPGB clock select register	PPGAB	R/W		000000XX
4FH	Reserved				
50H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000
51H	Timer Control Status 0	TMCSR0	R/W		XXXX0000
52H to 53H	Reserved				
54H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000
55H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000
56H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000
57H	Reserved				
58H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00
59H	Output Compare Control Status 1	OCS1	R/W		0XX00000
5AH	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00
5BH	Output Compare Control Status 3	OCS3	R/W		0XX00000
5CH to 6EH	Reserved				
6FH	ROM Mirror	ROMM	W	ROM Mirror	XXXXXXX1
70H to 7FH	Reserved				
80H to 8FH	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLER”				
90H to 9DH	Reserved				
9EH	ROM Correction Control Status 0	PACSR0	R/W	ROM Correction 0	00000000
9FH	Delayed Interrupt/release	DIRR	R/W	Delayed Interrupt	XXXXXXX0
A0H	Low-power Mode	LPMCR	R/W	Low Power Controller	00011000
A1H	Clock Selector	CKSCR	R/W	Low Power Controller	11111100
A2H to A7H	Reserved				
A8H	Watchdog Control	WDTC	R/W	Watchdog Timer	XXXXX111
A9H	Time Base Timer Control	TBTC	R/W	Time Base Timer	1XX00100
AAH to ADH	Reserved				

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
AE$_H$	Flash Control Status (Flash devices only. Otherwise reserved)	FMCS	R/W	Flash Memory	000X0000
AF$_H$	Reserved				
B0$_H$	Interrupt control register 00	ICR00	R/W	Interrupt controller	00000111
B1$_H$	Interrupt control register 01	ICR01	R/W		00000111
B2$_H$	Interrupt control register 02	ICR02	R/W		00000111
B3$_H$	Interrupt control register 03	ICR03	R/W		00000111
B4$_H$	Interrupt control register 04	ICR04	R/W		00000111
B5$_H$	Interrupt control register 05	ICR05	R/W		00000111
B6$_H$	Interrupt control register 06	ICR06	R/W		00000111
B7$_H$	Interrupt control register 07	ICR07	R/W		00000111
B8$_H$	Interrupt control register 08	ICR08	R/W		00000111
B9$_H$	Interrupt control register 09	ICR09	R/W		00000111
BA$_H$	Interrupt control register 10	ICR10	R/W		00000111
BB$_H$	Interrupt control register 11	ICR11	R/W		00000111
BC$_H$	Interrupt control register 12	ICR12	R/W		00000111
BD$_H$	Interrupt control register 13	ICR13	R/W		00000111
BE$_H$	Interrupt control register 14	ICR14	R/W		00000111
BF$_H$	Interrupt control register 15	ICR15	R/W		00000111
C0$_H$ to FF$_H$	Reserved				

Address	Register	Abbreviation	Access	Resource name	Initial value
3500H	Reload L	PRLL0	R/W	16-bit Programable Pulse Generator 0/1	XXXXXXXX
3501H	Reload H	PRLH0	R/W		XXXXXXXX
3502H	Reload L	PRLL1	R/W		XXXXXXXX
3503H	Reload H	PRLH1	R/W		XXXXXXXX
3504H	Reload L	PRLL2	R/W	16-bit Programable Pulse Generator 2/3	XXXXXXXX
3505H	Reload H	PRLH2	R/W		XXXXXXXX
3506H	Reload L	PRLL3	R/W		XXXXXXXX
3507H	Reload H	PRLH3	R/W		XXXXXXXX
3508H	Reload L	PRLL4	R/W	16-bit Programable Pulse Generator 4/5	XXXXXXXX
3509H	Reload H	PRLH4	R/W		XXXXXXXX
350AH	Reload L	PRLL5	R/W		XXXXXXXX
350BH	Reload H	PRLH5	R/W		XXXXXXXX
350CH	Reload L	PRLL6	R/W	16-bit Programable Pulse Generator 6/7	XXXXXXXX
350DH	Reload H	PRLH6	R/W		XXXXXXXX
350EH	Reload L	PRLL7	R/W		XXXXXXXX
350FH	Reload H	PRLH7	R/W		XXXXXXXX
3510H	Reload L	PRLL8	R/W	16-bit Programable Pulse Generator 8/9	XXXXXXXX
3511H	Reload H	PRLH8	R/W		XXXXXXXX
3512H	Reload L	PRLL9	R/W		XXXXXXXX
3513H	Reload H	PRLH9	R/W		XXXXXXXX
3514H	Reload L	PRLLA	R/W	16-bit Programable Pulse Generator A/B	XXXXXXXX
3515H	Reload H	PRLHA	R/W		XXXXXXXX
3516H	Reload L	PRLLB	R/W		XXXXXXXX
3517H	Reload H	PRLHB	R/W		XXXXXXXX
3518H	Serial Mode Register	SMR3	R/W	UART3	00000000
3519H	Serial Control Register	SCR3	R/W		00000000
351AH	Reception/Transmission Data Register	RDR3/ TDR3	R/W		00000000
351BH	Serial Status Register	SSR3	R/W		00001000
351CH	Extended Communication Control Reg.	ECCR3	R/W		000000XX
351DH	Extended Status/Control Register	ESCR3	R/W		00000100
351EH	Baud Rate Register 0	BGR03	R/W		00000000
351FH	Baud Rate Register 1	BGR13	R/W		00000000

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
3520H	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX
3521H	Input Capture 0	IPCP0	R		XXXXXXXX
3522H	Input Capture 1	IPCP1	R		XXXXXXXX
3523H	Input Capture 1	IPCP1	R		XXXXXXXX
3524H	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX
3525H	Input Capture 2	IPCP2	R		XXXXXXXX
3526H	Input Capture 3	IPCP3	R		XXXXXXXX
3527H	Input Capture 3	IPCP3	R		XXXXXXXX
3528H	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX
3529H	Input Capture 4	IPCP4	R		XXXXXXXX
352AH	Input Capture 5	IPCP5	R		XXXXXXXX
352BH	Input Capture 5	IPCP5	R		XXXXXXXX
352CH	Timer Data 0	TCDT0	R/W	I/O Timer 0	00000000
352DH	Timer Data 0	TCDT0	R/W		00000000
352EH	Timer Control 0	TCCS0	R/W		00000000
352FH	Timer Control 0	TCCS0	R/W		0XXXXXXX
3530H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX
3531H	Output Compare 0	OCCP0	R/W		XXXXXXXX
3532H	Output Compare 1	OCCP1	R/W		XXXXXXXX
3533H	Output Compare 1	OCCP1	R/W		XXXXXXXX
3534H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX
3535H	Output Compare 2	OCCP2	R/W		XXXXXXXX
3536H	Output Compare 3	OCCP3	R/W		XXXXXXXX
3537H	Output Compare 3	OCCP3	R/W		XXXXXXXX
3538H to 353BH	Reserved				
353CH	Timer Data 1	TCDT1	R/W	I/O Timer 1	00000000
353DH	Timer Data 1	TCDT1	R/W		00000000
353EH	Timer Control 1	TCCS1	R/W		00000000
353FH	Timer Control 1	TCCS1	R/W		0XXXXXXX
3540H	Timer 0/Reload 0	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX
3541H	Timer 0/Reload 0	TMR0/ TMRLR0	R/W		XXXXXXXX
3542H to 356DH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
356EH	CAN Direct Mode Register	CDMR	R/W	CAN clock sync	XXXXXXX0
356FH to 359FH	Reserved				
35A0H	I²C bus status register	IBSR	R	I²C Interface	00000000
35A1H	I²C bus control register	IBCR	R/W		00000000
35A2H	I²C ten bit slave address register	ITBAL	R/W		00000000
35A3H		ITBAH	R/W		00000000
35A4H	I²C ten bit address mask register	ITMKL	R/W		11111111
35A5H		ITMKH	R/W		00111111
35A6H	I²C seven bit slave address register	ISBA	R/W		00000000
35A7H	I²C seven bit address mask register	ISMK	R/W		01111111
35A8H	I²C data register	IDAR	R/W		00000000
35A9H to 35AAH	Reserved				
35ABH	I²C clock control register	ICCR	R/W	I²C Interface	00011111
35ACH to 35C1H	Reserved				
35C2H	Clock Modulator Control Register	CMCR	R/W	Phase Modulator	0XXXXXXX
35C3H to 35C8H	Reserved				
35C9H	Input Capture Edge 0/1	ICE01	R/W	Input Capture 0/1	XXXXX0XX
35CAH	Input Capture Edge 2/3	ICE23	R	Input Capture 2/3	XXXXXXXX
35CBH	Input Capture Edge 4/5	ICE45	R/W	Input Capture 4/5	XXXXX0XX
35CCH to 35CEH	Reserved				
35CFH	PLL and Special Configuration Control Register	PSCCR	W	PLL	XXXX0000
35D0H to 35DFH	Reserved				
35E0H	ROM Correction Address 0	PADR0	R/W	Address Matching Detection Function 0	XXXXXXXX
35E1H	ROM Correction Address 0	PADR0	R/W		XXXXXXXX
35E2H	ROM Correction Address 0	PADR0	R/W		XXXXXXXX
35E3H	ROM Correction Address 1	PADR1	R/W		XXXXXXXX
35E4H	ROM Correction Address 1	PADR1	R/W		XXXXXXXX
35E5H	ROM Correction Address 1	PADR1	R/W		XXXXXXXX

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
35E6H	ROM Correction Address 2	PADR2	R/W	Address Matching Detection Function 0	XXXXXXXX
35E7H	ROM Correction Address 2	PADR2	R/W		XXXXXXXX
35E8H	ROM Correction Address 2	PADR2	R/W		XXXXXXXX
35E9H to 37FFH	Reserved				
3800H to 38FFH	Reserved for CAN Interface 1. Refer to "■ CAN CONTROLLER"				
3900H to 39FFH	Reserved for CAN Interface 1. Refer to "■ CAN CONTROLLER"				
3A00H to 3FFFH	Reserved				

_ : Unused bit

X : Unknown value

Note : Addresses in the range 0000H to 00BFH, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results reading "X" and any write access should not be performed.

■ CAN CONTROLLER

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance mask register 0/acceptance mask register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers (1)

Address CAN1	Register	Abbreviation	Access	Initial Value
000080H	Message buffer valid register	BVALR	R/W	00000000
000081H				00000000
000082H	Transmit request register	TREQR	R/W	00000000
000083H				00000000
000084H	Transmit cancel register	TCANR	W	00000000
000085H				00000000
000086H	Transmit complete register	TCR	R/W	00000000
000087H				00000000
000088H	Receive complete register	RCR	R/W	00000000
000089H				00000000
00008AH	Remote request receiving register	RRTRR	R/W	00000000
00008BH				00000000
00008CH	Receive overrun register	ROVRR	R/W	00000000
00008DH				00000000
00008EH	Receive interrupt enable register	RIER	R/W	00000000
00008FH				00000000

List of Control Registers (2)

Address CAN1	Register	Abbreviation	Access	Initial Value
003900H	Control status register	CSR	R/W, R	00XXX000
003901H				0XXXX0X1
003902H	Last event indicator register	LEIR	R/W	XXXXXXXX
003903H				000X0000
003904H	Receive/transmit error counter	RTEC	R	00000000
003905H				00000000
003906H	Bit timing register	BTR	R/W	X1111111
003907H				11111111
003908H	IDE register	IDER	R/W	XXXXXXXX
003909H				XXXXXXXX
00390AH	Transmit RTR register	TRTRR	R/W	00000000
00390BH				00000000
00390CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX
00390DH				XXXXXXXX
00390EH	Transmit interrupt enable register	TIER	R/W	00000000
00390FH				00000000
003910H	Acceptance mask select register	AMSR	R/W	XXXXXXXX
003911H				XXXXXXXX
003912H				XXXXXXXX
003913H				XXXXXXXX
003914H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX
003915H				XXXXXXXX
003916H				XXXXXXXX
003917H				XXXXXXXX
003918H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX
003919H				XXXXXXXX
00391AH				XXXXXXXX
00391BH				XXXXXXXX

List of Message Buffers (ID Registers) (1)

Address CAN1	Register	Abbreviation	Access	Initial Value
003800H to 00381FH	General-purpose RAM	—	R/W	XXXXXXXX to XXXXXXXX
003820H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXX
003821H				
003822H				XXXXXXXX XXXXXXXX
003823H				
003824H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXX
003825H				
003826H				XXXXXXXX XXXXXXXX
003827H				
003828H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXX
003829H				
00382AH				XXXXXXXX XXXXXXXX
00382BH				
00382CH	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX
00382DH				
00382EH				XXXXXXXX XXXXXXXX
00382FH				
003830H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX
003831H				
003832H				XXXXXXXX XXXXXXXX
003833H				
003834H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX
003835H				
003836H				XXXXXXXX XXXXXXXX
003837H				
003838H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX
003839H				
00383AH				XXXXXXXX XXXXXXXX
00383BH				
00383CH	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX
00383DH				
00383EH				XXXXXXXX XXXXXXXX
00383FH				

List of Message Buffers (ID Registers) (2)

Address CAN1	Register	Abbreviation	Access	Initial Value
003840H	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX
003841H				
003842H				XXXXXXXX XXXXXXXX
003843H				
003844H	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX
003845H				
003846H				XXXXXXXX XXXXXXXX
003847H				
003848H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX
003849H				
00384AH				XXXXXXXX XXXXXXXX
00384BH				
00384CH	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX
00384DH				
00384EH				XXXXXXXX XXXXXXXX
00384FH				
003850H	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX
003851H				
003852H				XXXXXXXX XXXXXXXX
003853H				
003854H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX
003855H				
003856H				XXXXXXXX XXXXXXXX
003857H				
003858H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX
003859H				
00385AH				XXXXXXXX XXXXXXXX
00385BH				
00385CH	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX
00385DH				
00385EH				XXXXXXXX XXXXXXXX
00385FH				

List of Message Buffers (DLC Registers and Data Registers) (1)

Address CAN1	Register	Abbreviation	Access	Initial Value
003860H	DLC register 0	DLCR0	R/W	XXXXXXXX
003861H				
003862H	DLC register 1	DLCR1	R/W	XXXXXXXX
003863H				
003864H	DLC register 2	DLCR2	R/W	XXXXXXXX
003865H				
003866H	DLC register 3	DLCR3	R/W	XXXXXXXX
003867H				
003868H	DLC register 4	DLCR4	R/W	XXXXXXXX
003869H				
00386AH	DLC register 5	DLCR5	R/W	XXXXXXXX
00386BH				
00386CH	DLC register 6	DLCR6	R/W	XXXXXXXX
00386DH				
00386EH	DLC register 7	DLCR7	R/W	XXXXXXXX
00386FH				
003870H	DLC register 8	DLCR8	R/W	XXXXXXXX
003871H				
003872H	DLC register 9	DLCR9	R/W	XXXXXXXX
003873H				
003874H	DLC register 10	DLCR10	R/W	XXXXXXXX
003875H				
003876H	DLC register 11	DLCR11	R/W	XXXXXXXX
003877H				
003878H	DLC register 12	DLCR12	R/W	XXXXXXXX
003879H				
00387AH	DLC register 13	DLCR13	R/W	XXXXXXXX
00387BH				
00387CH	DLC register 14	DLCR14	R/W	XXXXXXXX
00387DH				
00387EH	DLC register 15	DLCR15	R/W	XXXXXXXX
00387FH				

List of Message Buffers (DLC Registers and Data Registers) (2)

Address CAN1	Register	Abbreviation	Access	Initial Value
003880H to 003887H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX to XXXXXXXX
003888H to 00388FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX to XXXXXXXX
003890H to 003897H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX to XXXXXXXX
003898H to 00389FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX to XXXXXXXX
0038A0H to 0038A7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX to XXXXXXXX
0038A8H to 0038AFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX to XXXXXXXX
0038B0H to 0038B7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX to XXXXXXXX
0038B8H to 0038BFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX to XXXXXXXX
0038C0H to 0038C7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX to XXXXXXXX
0038C8H to 0038CFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX to XXXXXXXX
0038D0H to 0038D7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX to XXXXXXXX
0038D8H to 0038DFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX to XXXXXXXX
0038E0H to 0038E7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX to XXXXXXXX
0038E8H to 0038EFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX to XXXXXXXX

List of Message Buffers (DLC Registers and Data Registers) (3)

Address CAN1	Register	Abbreviation	Access	Initial Value
0038F0H to 0038F7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX to XXXXXXXX
0038F8H to 0038FFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX to XXXXXXXX

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC$_H$	—	—
INT9 instruction	N/A	#09	FFFFD8$_H$	—	—
Exception	N/A	#10	FFFFD4$_H$	—	—
Time Base Timer	N/A	#11	FFFFD0$_H$	ICR00	0000B0$_H$
External Interrupt INT0 to INT7	○	#12	FFFFCC$_H$		
Reserved	×	#13	FFFFC8$_H$	ICR01	0000B1$_H$
Reserved	×	#14	FFFFC4$_H$		
CAN 1 RX	N/A	#15	FFFFC0$_H$	ICR02	0000B2$_H$
CAN 1 TX/NS	N/A	#16	FFFFBC$_H$		
PPG 0/1	N/A	#17	FFFFB8$_H$	ICR03	0000B3$_H$
PPG 2/3	N/A	#18	FFFFB4$_H$		
PPG 4/5	N/A	#19	FFFFB0$_H$	ICR04	0000B4$_H$
PPG 6/7	N/A	#20	FFFFAC$_H$		
PPG 8/9	N/A	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG A/B	N/A	#22	FFFFA4$_H$		
16-bit Reload Timer 0	○	#23	FFFFA0$_H$	ICR06	0000B6$_H$
Reserved	×	#24	FFFF9C$_H$		
Input Capture 0/1	○	#25	FFFF98$_H$	ICR07	0000B7$_H$
Output compare 0/1	○	#26	FFFF94$_H$		
Input Capture 2/3	○	#27	FFFF90$_H$	ICR08	0000B8$_H$
Output Compare 2/3	○	#28	FFFF8C$_H$		
Input Capture 4/5	○	#29	FFFF88$_H$	ICR09	0000B9$_H$
I²C	○	#30	FFFF84$_H$		
A/D Converter	○	#31	FFFF80$_H$	ICR10	0000BA$_H$
I/O Timer 0 / I/O Timer 1	N/A	#32	FFFF7C$_H$		
Serial I/O	○	#33	FFFF78$_H$	ICR11	0000BB$_H$
Reserved	×	#34	FFFF74$_H$		
UART 0 RX	◎	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART 0 TX	○	#36	FFFF6C$_H$		
Reserved	×	#37	FFFF68$_H$	ICR13	0000BD$_H$
Reserved	×	#38	FFFF64$_H$		

(Continued)

(Continued)

Interrupt cause	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
UART 3 RX	◎	#39	FFFF60H	ICR14	0000BEH
UART 3 TX	○	#40	FFFF5CH		
Flash Memory	N/A	#41	FFFF58H	ICR15	0000BFH
Delayed interrupt	N/A	#42	FFFF54H		

○ : The interrupt request flag is cleared by the EI²OS interrupt clear signal.

◎ : The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

× : Unavailable

N/A : The interrupt request flag is not cleared by the EI²OS interrupt clear signal.

Notes :
- For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ *2
	AVRH, AVRL	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH ≥ AVRL
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum Clamp Current	I_{CLAMP}	–4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	—	40	mA	*5
“L” level maximum output current	I_{OL1}	—	15	mA	*4
“L” level average output current	I_{OLAV1}	—	4	mA	*4
“L” level maximum overall output current	ΣI_{OL1}	—	100	mA	*4
“L” level average overall output current	ΣI_{OLAV1}	—	50	mA	*4
“H” level maximum output current	I_{OH1}	—	–15	mA	*4
“H” level average output current	I_{OHAV1}	—	–4	mA	*4
“H” level maximum overall output current	ΣI_{OH1}	—	–100	mA	*4
“H” level average overall output current	ΣI_{OHAV}	—	–50	mA	*4
Power consumption	P_D	—	500	mW	MB90F947, MB90F949
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{STG}	–55	+150	°C	

*1 : This parameter is based on $V_{SS} = AV_{SS} = 0$ V.

*2 : Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

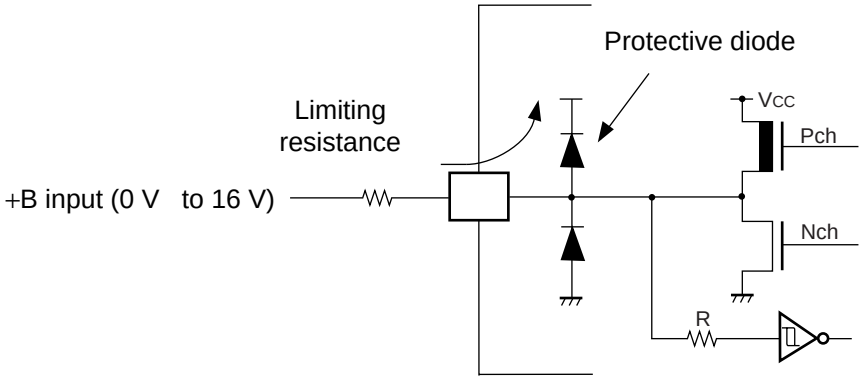
*3 : V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.

*4 : Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P80, P81, P90 to P97, PA0 to PA7, PB0 to PB7

*5 :
- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P80, P81, P90 to P97, PA0 to PA7, PB0 to PB7
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.

- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

- Input/output equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

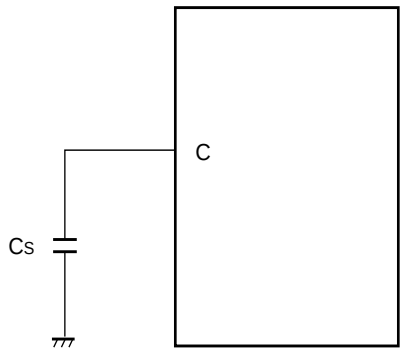
2. Recommended Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	3.5	5.0	5.5	V	Other than when writing to Flash Memory and when using the A/D converter
		4.0	5.0	5.5	V	When writing to Flash Memory
		4.5	5.0	5.5	V	When using the A/D converter
		2.0	—	5.5	V	Retain RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	µF	*
Operating temperature	T_A	–40	—	+85	°C	

* : Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the V_{CC} pin, use a bypass capacitor that has a larger capacity than that of C_S. Refer to the following figure for connection of smoothing capacitor C_S.

• C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “H” voltage	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs except ports P21/RX1, P42/SDA, P43/SCL
	V_{IHA}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Port inputs P21/RX1, P42/SDA, P43/SCL
	V_{IHR}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS Hysteresis)
	V_{IHM}	—	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	MD input pin
Input “L” voltage	V_{ILS}	—	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	Port inputs except ports P21/RX1, P42/SDA, P43/SCL
	V_{ILA}	—	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	Port inputs P21/RX1, P42/SDA, P43/SCL
	V_{ILR}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS Hysteresis)
	V_{ILM}	—	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	MD input pin
Output “H” voltage	V_{OH}	Normal outputs	V_{CC} = 4.5 V, I_{OH1} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Output “H” voltage	V_{OHI}	I^2C outputs	V_{CC} = 4.5 V, I_{OH1} = –3.0 mA	V_{CC} – 0.5	—	—	V	
Output “L” voltage	V_{OL}	Normal outputs	V_{CC} = 4.5 V, I_{OL1} = 4.0 mA	—	—	0.4	V	
Output “L” voltage	V_{OLI}	I^2C outputs	V_{CC} = 4.5 V, I_{OL1} = 3.0 mA	—	—	0.4	V	
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–1	—	1	µA	

(Continued)

(Continued)

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	60	75	mA	MB90F947 MB90F949
			V_{CC} = 5.0 V, Internal frequency : 20 MHz, At normal operation.	—	50	65	mA	MB90F947 MB90F949
			V_{CC} = 5.0 V, Internal frequency : 20 MHz, At writing FLASH memory.	—	65	80	mA	MB90F947 MB90F949
			V_{CC} = 5.0 V, Internal frequency : 20 MHz, At erasing FLASH memory.	—	70	85	mA	MB90F947 MB90F949
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At Sleep mode.	—	25	35	mA	MB90F947 MB90F949
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency : 2 MHz, At Main Timer mode	—	0.3	0.6	mA	MB90F947 MB90F949
	$I_{CTSPLL6}$		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At PLL Timer mode, external frequency = 4 MHz	—	5	7	mA	MB90F947 MB90F949
	I_{CCH}		V_{CC} = 5.0 V, At Stop mode, T_A = +25°C	—	5	100	µA	MB90F947 MB90F949
Input capacity	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}	—	—	5	15	pF	

* : The power supply current is measured with an external clock.

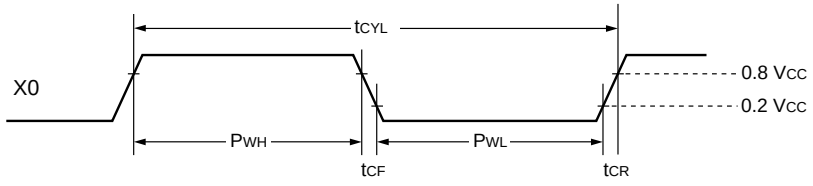
4. AC Characteristics

(1) Clock Timing

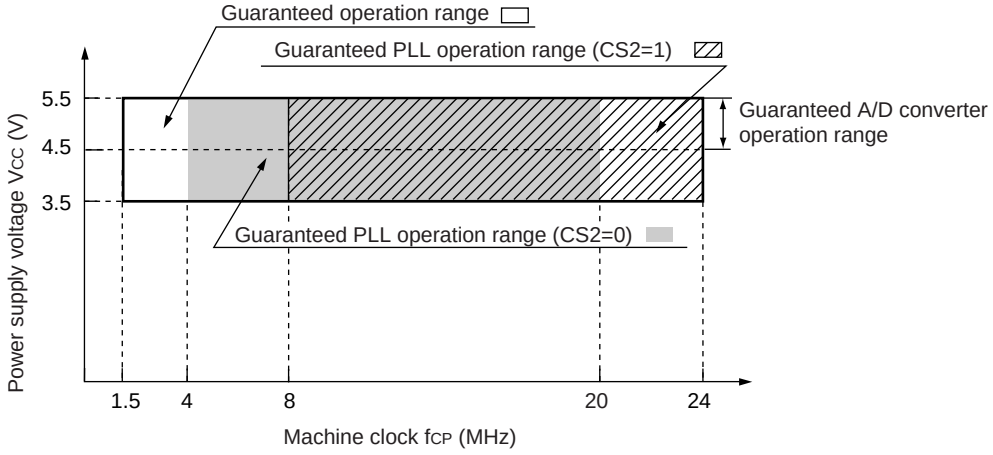
(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value				Unit	Remarks
			Min	Typ	Max			
					CS2 = 0	CS2 = 1		
Clock frequency	f_C	X0, X1	3	—	8	8	MHz	× 1/2 (When PLL stops) When using an oscillation circuit
			4	—	8	—	MHz	PLL × 1 When using an oscillation circuit
			4	—	8	8	MHz	PLL × 2 When using an oscillation circuit
			4	—	6.67	—	MHz	PLL × 3 When using an oscillation circuit
			4	—	5	6	MHz	PLL × 4 When using an oscillation circuit
			4	—	—	4	MHz	PLL × 6 When using an oscillation circuit
		X0	3	—	12	12	MHz	× 1/2 (When PLL stops) When using an external circuit
			4	—	12	—	MHz	PLL × 1 When using an external circuit
			4	—	10	12	MHz	PLL × 2 When using an external circuit
			4	—	6.67	—	MHz	PLL × 3 When using an external circuit
			4	—	5	6	MHz	PLL × 4 When using an external circuit
			4	—	—	4	MHz	PLL × 6 When using an external circuit
Clock cycle time	t_{CYL}	X0, X1	125	—	333		ns	When using an oscillation circuit
		X0, X1	83.33	—	333		ns	When using an external clock
Input clock pulse width	P_{WH}, P_{WL}	X0	20	—	—		ns	Duty ratio is about 30% to 70%.
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5		ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	24		MHz	Except programming or erasing Flash memory. When using clock modulation, be sure that the maximum momentary frequency F_{max} does not exceed 24MHz. Refer to the Clock Modulator chapter of the Hardware Manual.
		—	1.5	—	20		MHz	When programming or erasing Flash memory. Be sure that the maximum momentary frequency F_{max} does not exceed 20MHz.
Machine clock cycle time	t_{CP}	—	41.67	—	666		ns	Except programming or erasing Flash memory.
		—	50	—	666		ns	When programming or erasing Flash memory.

Clock Timing

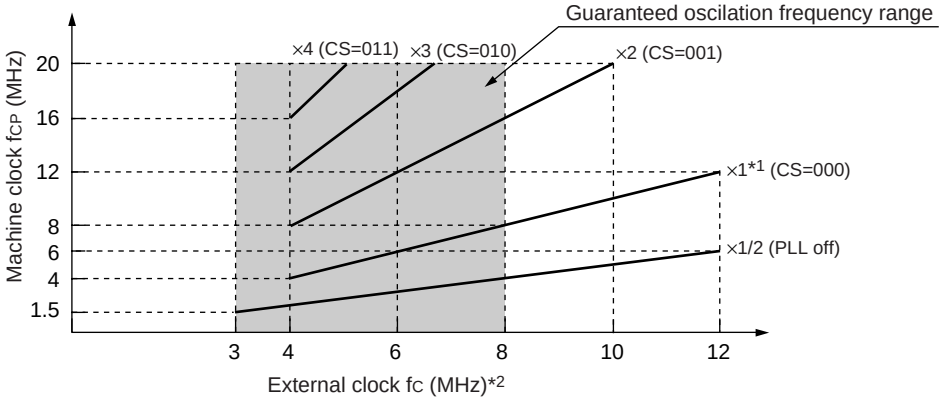


• Guaranteed PLL operation range

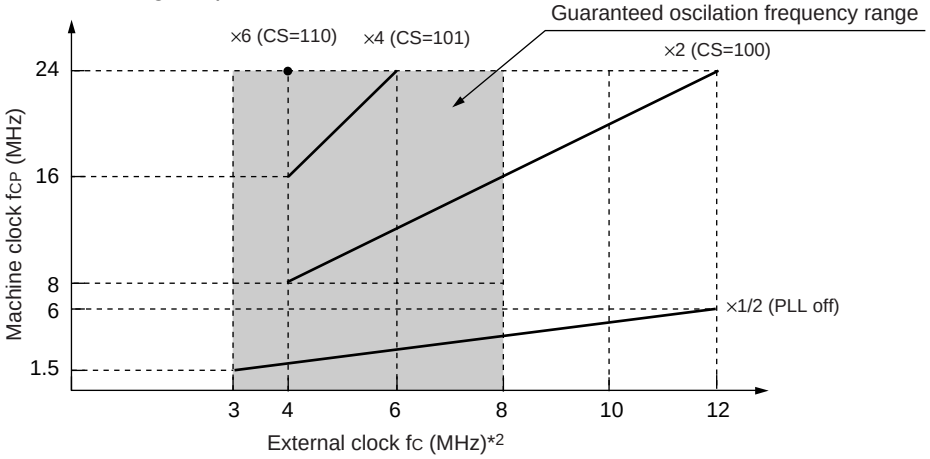


Guaranteed operation range of MB90F947/MB90F949

• CS2 (bit 0 in PSCCR register) = 0



• CS2 (bit 0 in PSCCR register) = 1



*1 : PLL × 1 guaranteed operation range is from 4.0 MHz to 12 MHz.

*2 : When using a crystal oscillator or a ceramic oscillator, the maximum oscillation clock frequency is 8 MHz

External clock frequency and Machine clock frequency

(2) Reset Standby Input

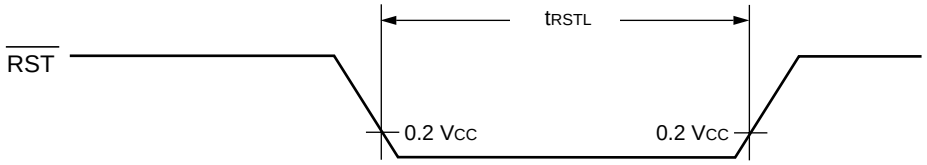
(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	16 t_{CP}*1	—	ns	Under normal operation
			Oscillation time of oscillator*2 + 100 + 16 t_{CP}*1	—	µs	In Stop mode
			100	—	µs	In Time Base Timer mode

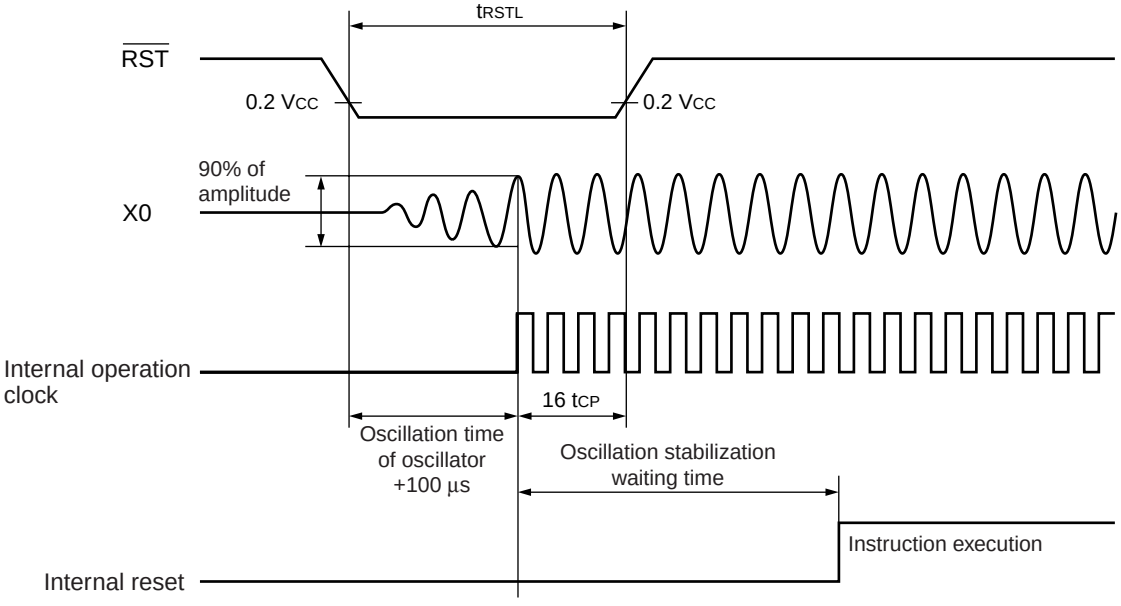
*1 : "t_{CP}" represents one cycle time of the machine clock.
No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90%.
In the crystal oscillator, the oscillation time is between several ms and to tens of ms. In FAR / ceramic oscillators, the oscillation time is between hundreds of µs to several ms. With an external clock, the oscillation time is 0 ms

Under normal operation :



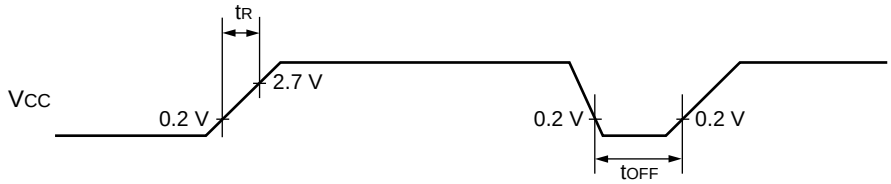
In Stop mode :



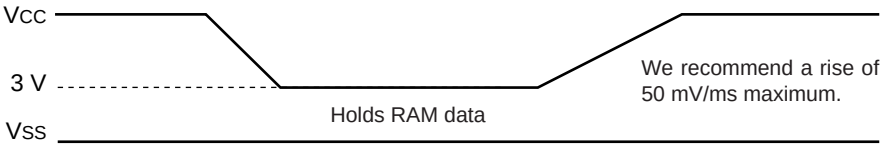
(3) Power On Reset

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Due to repetitive operation



If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



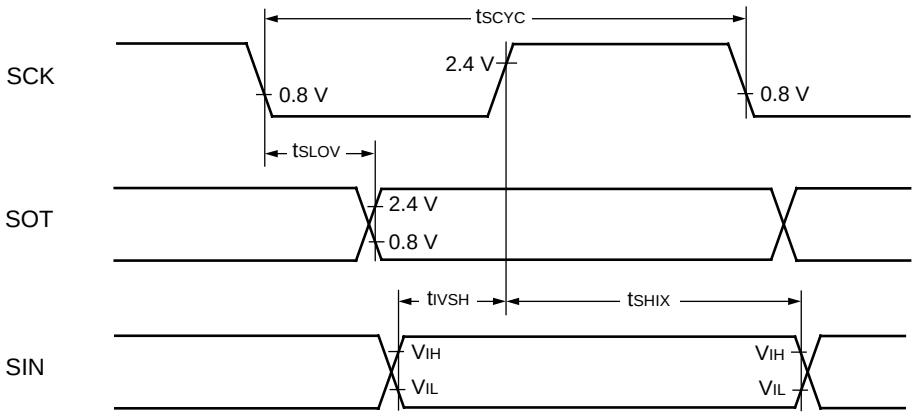
(4) UART0, SIO Timing

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V)

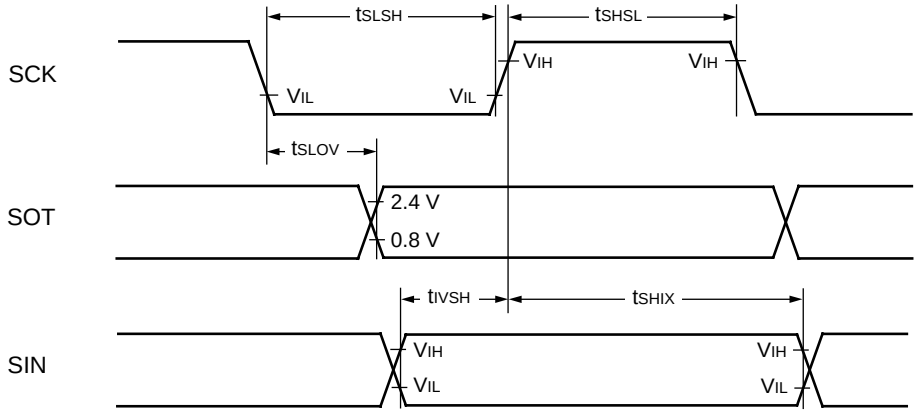
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0, SCK4	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK4, SOT0, SOT4		–80	+80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK4, SIN0, SIN4		100	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK0, SCK4, SIN0, SIN4		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0, SCK4	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0, SCK4		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK4, SOT0, SOT4		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK4, SIN0, SIN4		60	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK0, SCK4, SIN0, SIN4		60	—	ns	

Notes :
- AC characteristics in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing” rating for t_{CP}.

- Internal Shift Clock Mode



- External Shift Clock Mode



(5) UART3 Timing

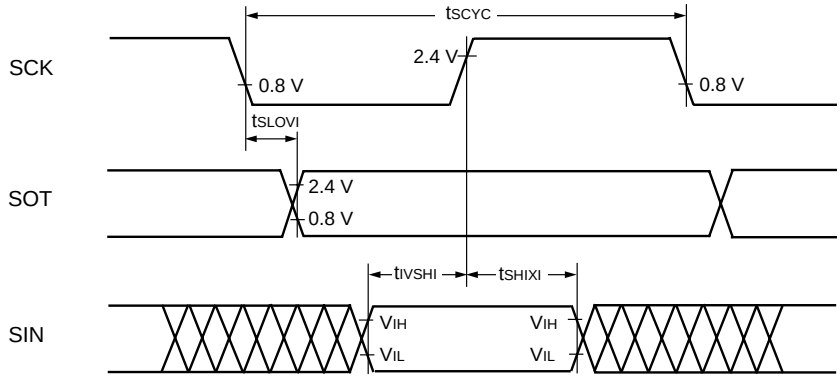
- Bit setting : ESCR : SCES = 0, ECCR : SCDE = 0

(T_A = –40 °C to +85 °C, V_{CC} = 3.5V to 5.5V, V_{SS} = AV_{SS} = 0V)

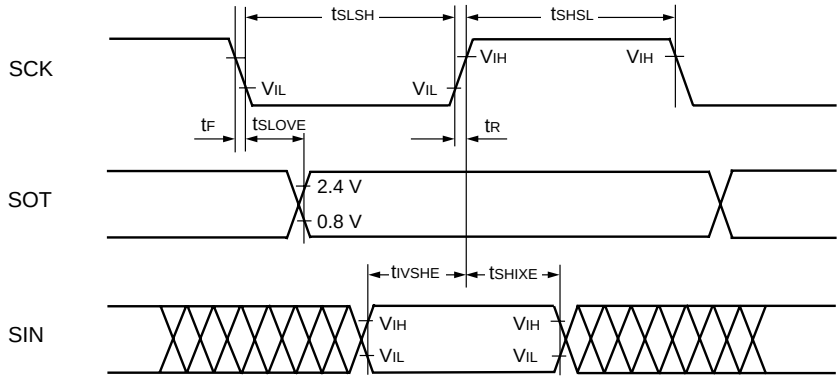
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOVI}	SCK3, SOT3		–50	+50	ns	
Valid SIN → SCK ↑	t_{IVSHI}	SCK3, SIN3		t_{CP} + 80	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK3, SIN3		0	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK3	External clock operation output pins are C_L = 80 pF + 1 TTL.	t_{CP} + 10	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK3		3 t_{CP} – t_R	—	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK3, SOT3		—	2 t_{CP} + 60	ns	
Valid SIN → SCK ↑	t_{IVSHE}	SCK3, SIN3		30	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK3, SIN3		t_{CP} + 30	—	ns	
SCK fall time	t_F	SCK3		—	10	ns	
SCK rise time	t_R	SCK3		—	10	ns	

Note : t_{CP} is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing” rating for t_{CP}.

- Internal Shift Clock Mode



- External Shift Clock Mode



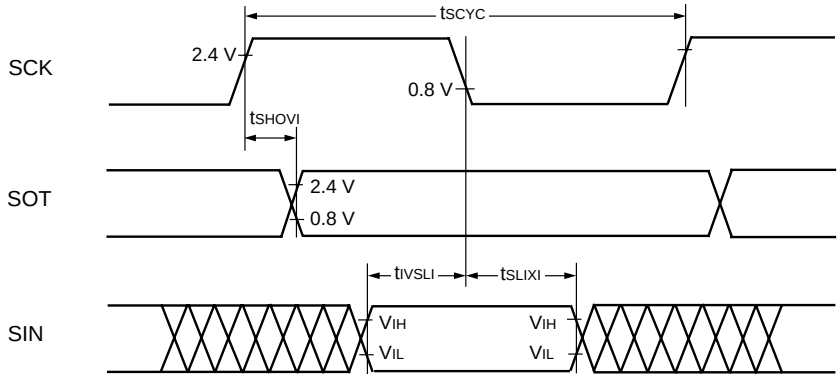
• Bit setting : ESCR : SCES = 1, ECCR : SCDE = 0

(T_A = –40 °C to +85 °C, V_{CC} = 3.5V to 5.5V, V_{SS} = AV_{SS} = 0V)

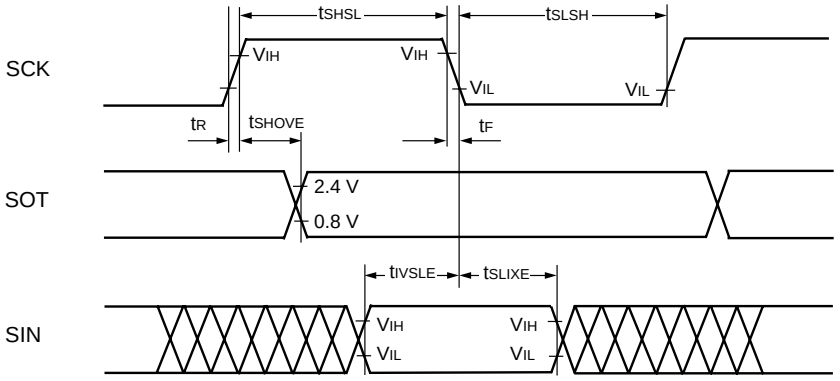
Parameter	Sym-bol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns	
SCK ↑ → SOT delay time	t_{SHOVI}	SCK3, SOT3		–50	+50	ns	
Valid SIN → SCK ↓	t_{IVSLI}	SCK3, SIN3		t_{CP} + 80	—	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK3, SIN3		0	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK3	External clock operation output pins are C_L = 80 pF + 1 TTL.	3 t_{CP} – t_R	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK3		t_{CP} + 10	—	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK3, SOT3		—	2 t_{CP} + 60	ns	
Valid SIN → SCK ↓	t_{IVSLE}	SCK3, SIN3		30	—	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}	SCK3, SIN3		t_{CP} + 30	—	ns	
SCK fall time	t_F	SCK3		—	10	ns	
SCK rise time	t_R	SCK3		—	10	ns	

Note : t_{CP} is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing” rating for t_{CP}.

• Internal Shift Clock Mode



• External Shift Clock Mode

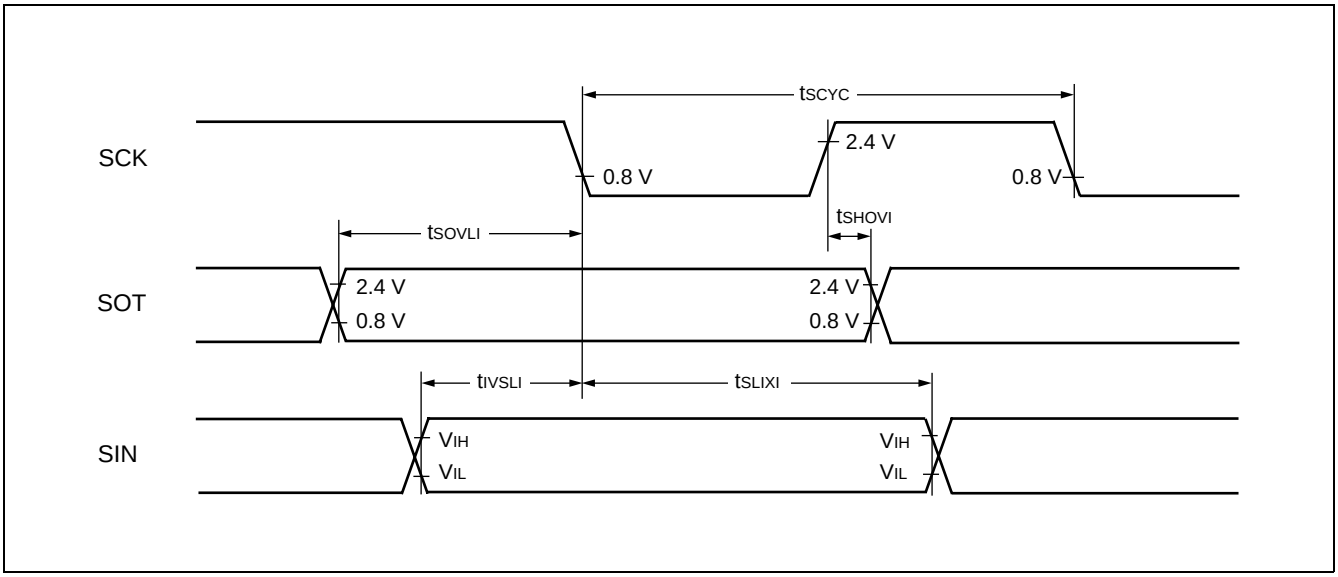


• Bit setting : ESCR : SCES = 0, ECCR : SCDE = 1

(T_A = –40 °C to +85 °C, V_{CC} = 3.5V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Sym-bol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns	
SCK ↑ → SOT delay time	t_{SHOVI}	SCK3, SOT3		–50	+50	ns	MB90F947, MB90F949
				t_{CP} – 60	t_{SCYC} / 2 + 70 – t_{CP}	ns	MB90V390H
Valid SIN → SCK ↓	t_{IVSLI}	SCK3, SIN3		t_{CP} + 80	—	ns	MB90F947, MB90F949
				100 – t_{CP}	—	ns	MB90V390H
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK3, SIN3		0	—	ns	MB90F947, MB90F949
				t_{SCYC} / 2	—	ns	MB90V390H
SOT → SCK ↓ delay time	t_{SOVLI}	SCK3, SOT3		3 t_{CP} – 70	—	ns	MB90F947, MB90F949
				t_{CP} – 60	—	ns	MB90V390H

Note : t_{CP} is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing” rating for t_{CP}.

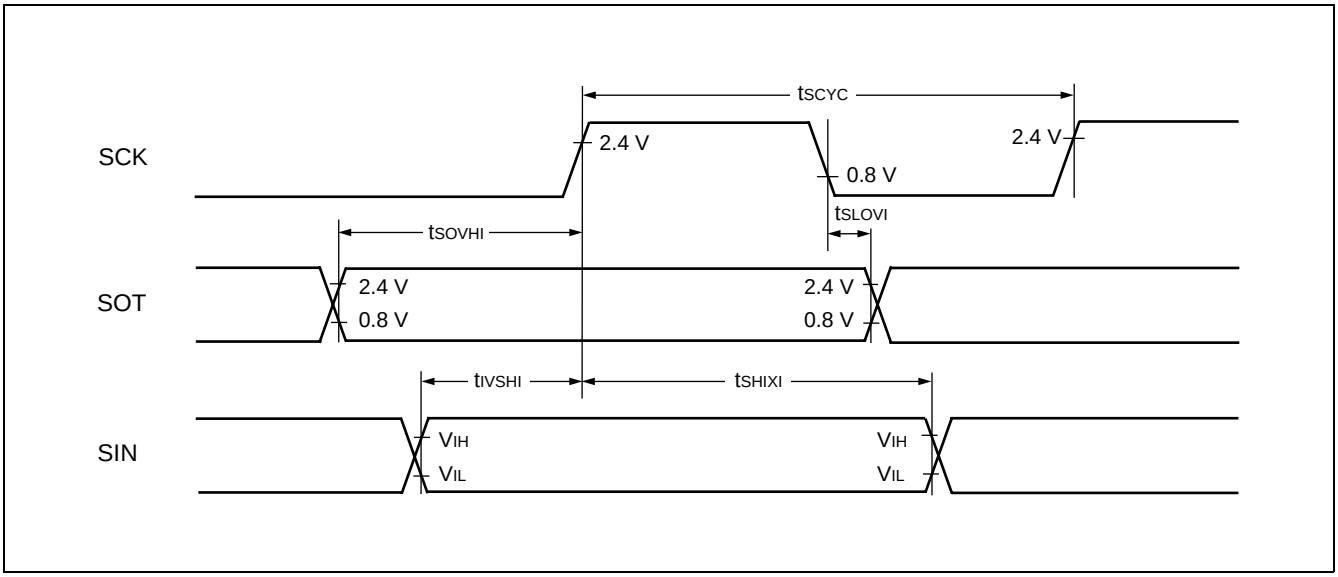


• Bit setting : ESCR : SCES = 1, ECCR : SCDE = 1

(T_A = –40 °C to +85 °C, V_{CC} = 3.5V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Sym-bol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOVI}	SCK3, SOT3		–50	+50	ns	MB90F947, MB90F949
				t_{CP} – 60	t_{SCYC} / 2 + 70 – t_{CP}	ns	MB90V390H
Valid SIN → SCK ↑	t_{IVSHI}	SCK3, SIN3		t_{CP} + 80	—	ns	MB90F947, MB90F949
				100 – t_{CP}	—	ns	MB90V390H
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK3, SIN3		0	—	ns	MB90F947, MB90F949
				t_{SCYC} / 2	—	ns	MB90V390H
SOT → SCK ↑ delay time	t_{SOVHI}	SCK3, SOT3		3 t_{CP} – 70	—	ns	MB90F947, MB90F949
				t_{CP} – 60	—	ns	MB90V390H

Note : t_{CP} is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing” rating for t_{CP}.



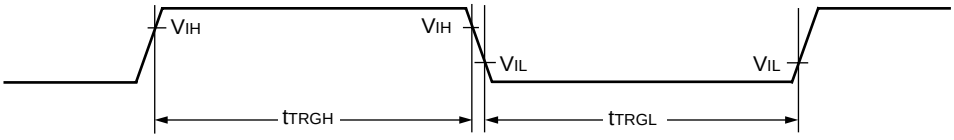
(6) Trigger Input Timing

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}	INT0 to INT7	—	200	—	ns	
	t_{TRGL}	ADTG		t_{CP} + 200	—	ns	

Note : t_{CP} is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing” rating for t_{CP}.

- Trigger Input Timing



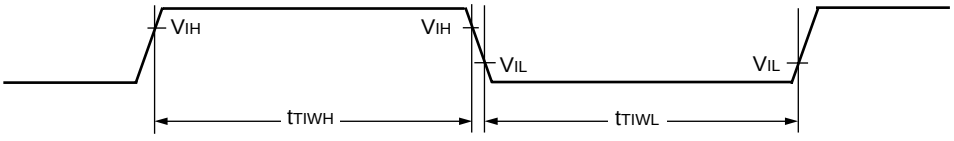
(7) Timer Related Resource Input Timing

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, IN0 to IN5	—	4 t_{CP}	—	ns	
	t_{TIWL}						

Note : t_{CP} is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing” rating for t_{CP}.

- Timer Input Timing



(8) I²C Timing

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.3 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	0.6	—	µs
"L" width of SCL clock	t_{LOW}		4.7	—	1.3	—	µs
"H" width of SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL ↑ → SDA ↓↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data set-up time SDA ↓↑ → SCL ↑	t_{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUS}		4.7	—	1.3	—	µs

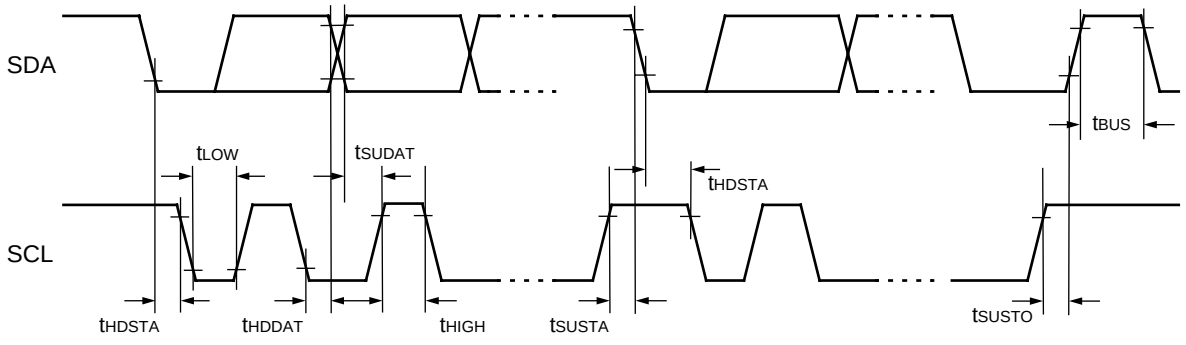
*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t_{HDDAT} only has to be met if the devie does not stretch the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.

*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.

• I²C Timing



5. A/D Converter

(T_A = –40 °C to +85 °C, 3.0 V ≤ AVRH – AVRL, V_{CC} = AV_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—		10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN14	AVRL – 1.5	AVRL + 0.5	AVRL + 2.5	LSB	
Full scale reading voltage	V_{FST}	AN0 to AN14	AVRH – 3.5	AVRH – 1.5	AVRH + 0.5	LSB	
Compare time	—	—	3.3	66 t_{CP}	16500	µs	
Sampling time	—	—	1.6	32 t_{CP}	∞	µs	
Analog port input current	I_{AIN}	AN0 to AN14	–0.3	—	+0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN14	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
		AVRL	0	—	AVRH – 2.7	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	165	250	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN14	—	—	4	LSB	

* : When not operating A/D converter, this is the current (V_{CC} = AV_{CC} = AVRH = 5.0 V) .

Terminology

Conversion error	:	Absolute maximum conversion deviation with respect to the theoretical conversion line.
Nonlinearity	:	Relative maximum conversion deviation with respect to the theoretical conversion line conncecting to the device unigque zero reading voltage and full scale reading voltage.
Differential nonlinearity	:	Max conversion deviation in any two adjacent reading voltages with respect to the theoretical LSB conversion step.
Zero reading voltage	:	Input voltage which results in the minimum conversion value.
Full scale reading voltage	:	Input voltage which results in the maximum conversion value.

Notes :
- t_{CP} is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing” rating for t_{CP}.
- The accuracy gets worse as AVRH – AVRL becomes smaller.

6. Definition of A/D Converter Terms

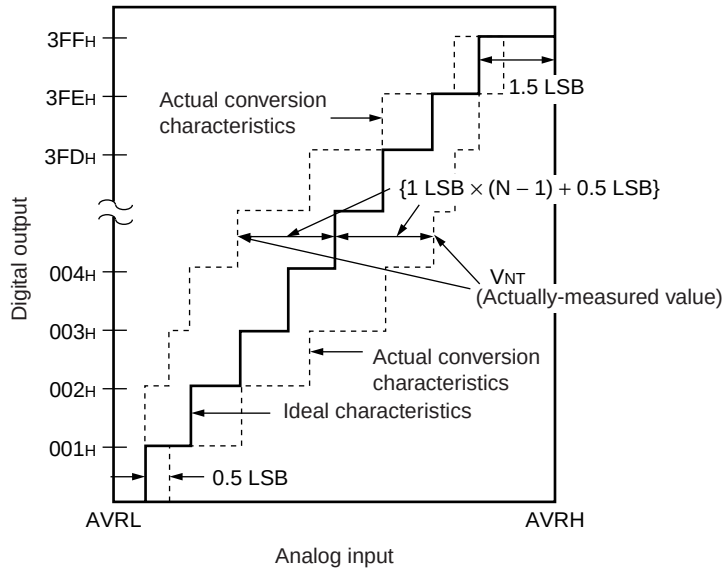
Resolution : Analog variation that is recognized by an A/D converter.

Linear error : Deviation between a line across zero-transition line (“00 0000 0000” ← → “00 0000 0001”) and full-scale transition line (“11 1111 1110” ← → “11 1111 1111”) and actual conversion characteristics.

Differential linear error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Total error : Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

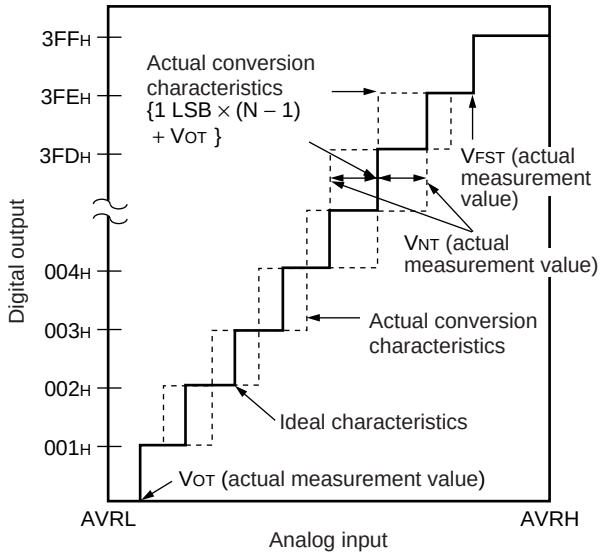
V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

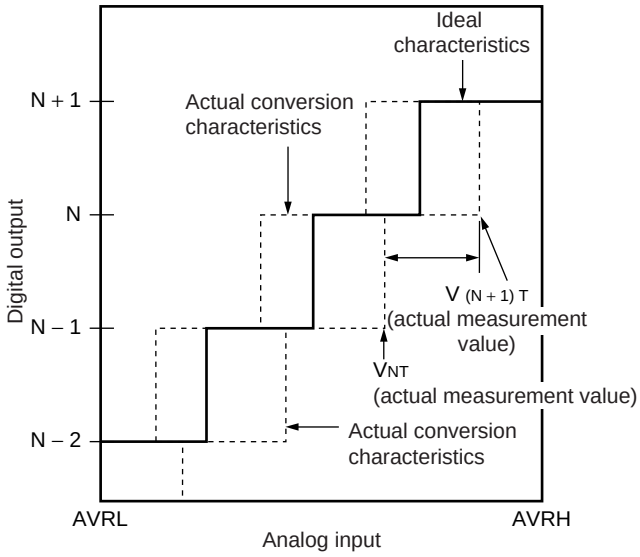
(Continued)

(Continued)

Linear error



Differential linear error



$$\text{Linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)\,T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

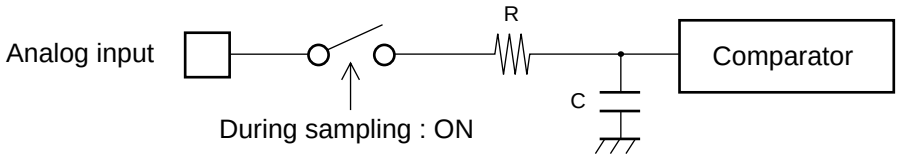
V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

7. Notes on A/D Converter Section

• About the external impedance of the analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

• Analog input circuit model



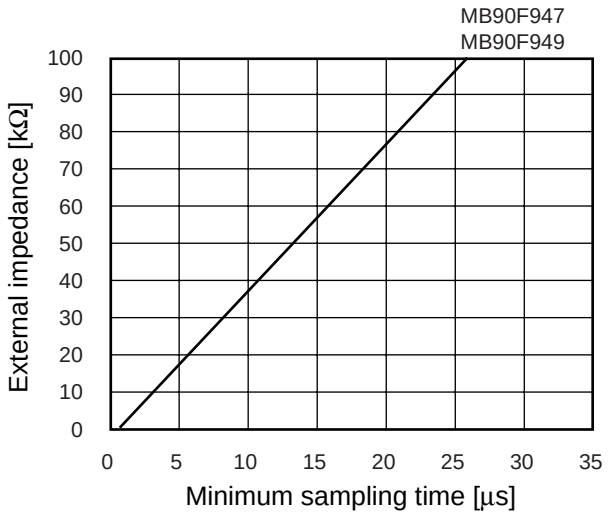
	R	C
MB90F947/F949	2.4 kΩ (Max)	36.4 pF (Max)

Note : The values are reference values.

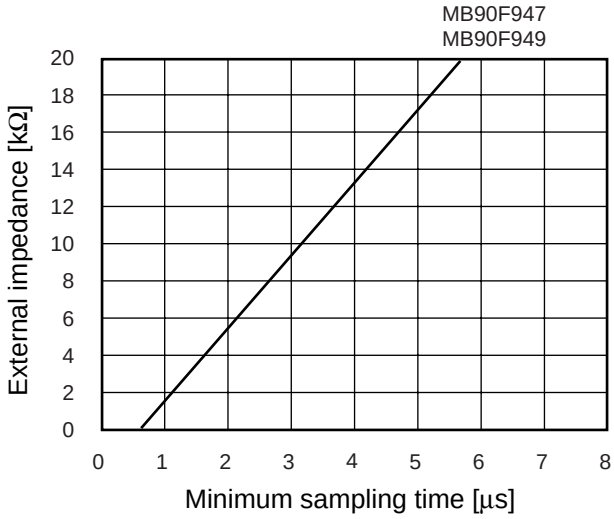
- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

• The relationship between the external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

• About the error

The accuracy gets worse as |AVRH − AVRL| becomes smaller.

8. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = +25 °C V_{CC} = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	5	—	s	MB90F947, Excludes programming prior to erasure
		—	7	—	s	MB90F949, Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3,600	µs	Except for the overhead time of the system
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Data Retention Time	Average T_A = +85 °C	20	—	—	Year	*

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

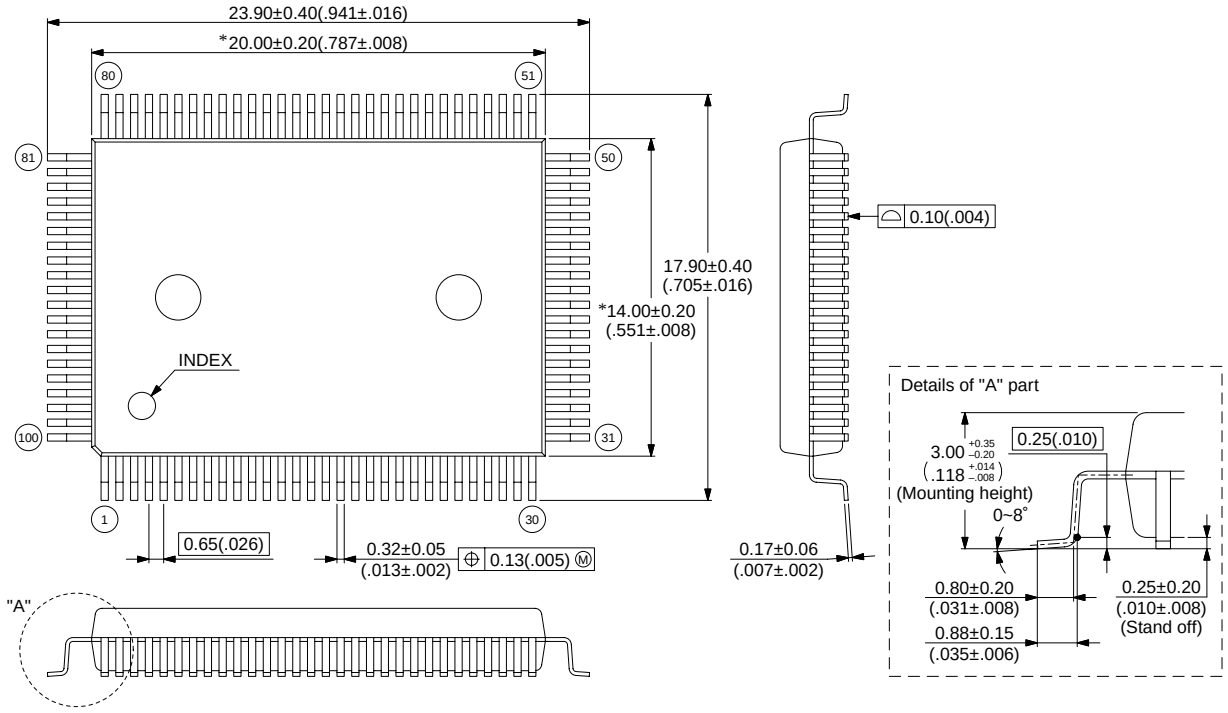
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F947PF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F949PF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V390HCR	299-pin Ceramic PGA (PGA-299C-A01)	For evaluation

■ PACKAGE DIMENSIONS

100-pin Plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



© 2002 FUJITSU LIMITED F100008S-c-5-5

Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

FUJITSU LIMITED

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-party's intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0502
© 2005 FUJITSU LIMITED Printed in Japan