



## DSP56724/DSP56725

# Symphony™ DSP56724/ DSP56725 Multi-Core Audio Processors



DSP56724  
144-Pin LQFP  
20 mm × 20 mm  
0.5 mm pitch



DSP56725  
80-Pin LQFP  
14 mm × 14 mm  
0.65 mm pitch

See [Table 19](#).

The Symphony DSP56724/DSP56725 Multi-Core Audio Processors are part of the DSP5672x family of programmable CMOS DSPs, designed using dual DSP56300 24-bit cores.

The DSP56724 is intended for consumer and professional audio applications that require high performance for audio processing. In addition, the DSP56724 is ideally suited for applications that need the capability to expand memory off-chip or to interface to external parallel peripherals. Potential applications include A/V receivers, DVD Receivers, Home Theater in a Box (HTIB), and professional audio equipment including portable recording equipment, musical instruments, guitar amplifiers and pedals. The DSP56724 offers customers flexibility in their designs by providing a more cost-effective alternative to the DSP56720 while maintaining pin compatibility.

The DSP56725 is intended for automotive and audio applications that require high performance for audio processing. Potential applications include A/V receivers, DVD Receivers, Home Theater in a Box (HTIB), and automotive amplifiers and entertainment systems. The DSP56725 offers customers flexibility in their designs by providing a more cost-effective alternative to the DSP56721 while maintaining pin compatibility.

The DSP56724/DSP56725 devices provide a wealth of on-chip audio processing functions, via a plug and play software architecture system that supports audio decoding algorithms, various equalization algorithms, compression, signal generator, tone control, fade/balance, level meter/spectrum analyzer, among others. The DSP56724/DSP56725 devices also support various matrix decoders and sound field processing algorithms.

With two DSP56300 cores, a single DSP56724/ DSP56725 device can replace dual-DSP designs, saving costs while

meeting high MIPs requirements. Legacy peripherals from the previous DSP5636x/37x families are included, as are a variety of new modules available in the DSP5672x family. Modules from the DSP56720 are included, such as an Asynchronous Sample Rate Converter (ASRC), an Inter-Core Communication (ICC) module, an External Memory Controller (EMC) to support SDRAM (DSP56724 only), and a Sony/Philips Digital Interface (S/PDIF) transceiver.

The DSP56724/DSP56725 devices offer up to 250 million instructions per second (MIPs) per core using an internal 250 MHz clock. The DSP56724/ DSP56725 products are high density CMOS devices with 3.3 V inputs and outputs.

The DSP56724 block diagram is shown in [Figure 1](#); the DSP56725 block diagram is shown in [Figure 2](#).

### NOTE

This document contains information on a new product. Specifications and information herein are subject to change without notice. Finalized specifications may be published after further characterization and device qualifications are completed.

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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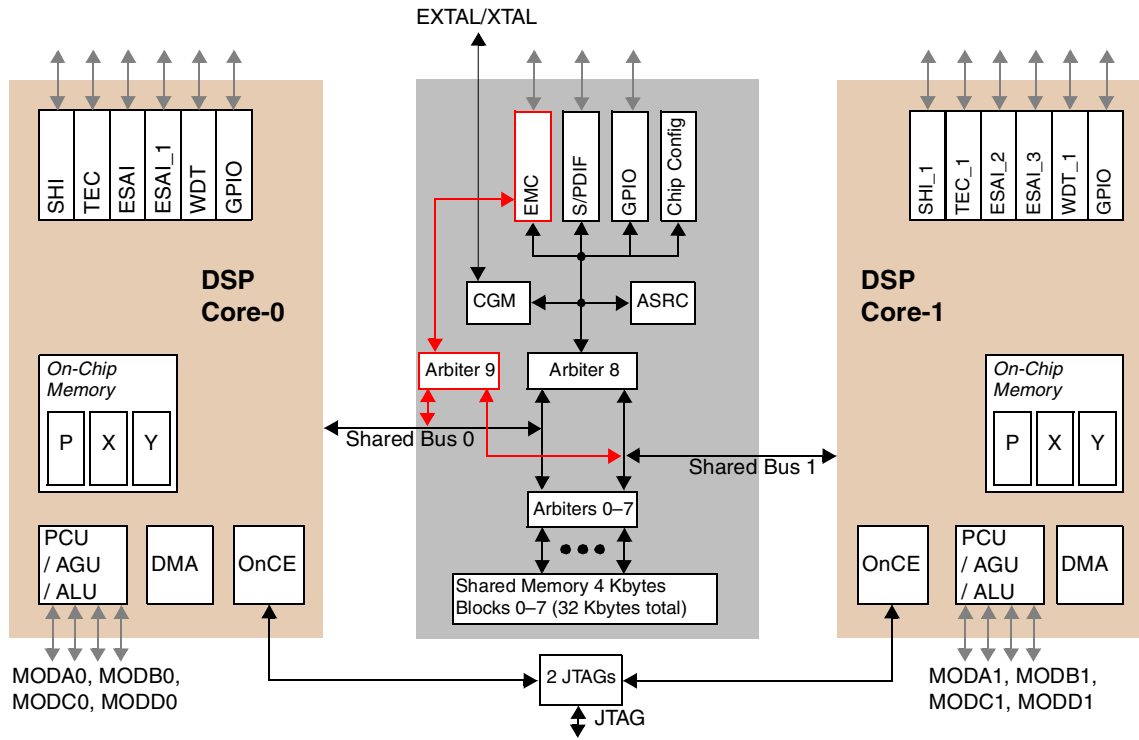


Figure 1. DSP56724 Block Diagram

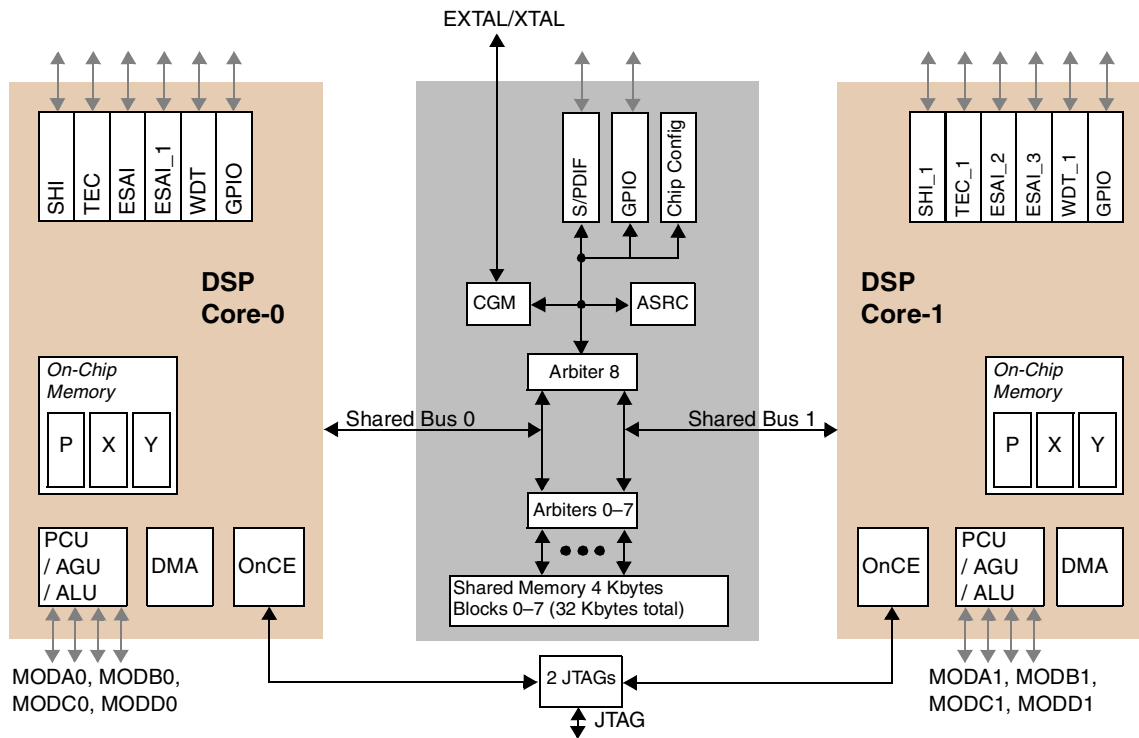


Figure 2. DSP56725 Block Diagram

# 1 Electrical Characteristics

## 1.1 Chip-Level Conditions

Table 1 provides a quick reference to the subsections in this section.

**Table 1. Chip-Level Conditions**

| For   | See        |
|---|------------|
| Section 1.1.1, "Maximum Ratings"                                | on page 4  |
| Section 1.1.2, "Thermal Characteristics"                        | on page 6  |
| Section 1.1.3, "Power Requirements"                             | on page 6  |
| Section 1.1.4, "DC Electrical Characteristics"                  | on page 7  |
| Section 1.1.5, "AC Electrical Characteristics"                  | on page 8  |
| Section 1.1.6, "Internal Clocks"                                | on page 8  |
| Section 1.1.7, "External Clock Operation"                       | on page 9  |
| Section 1.1.8, "Reset, Stop, Mode Select, and Interrupt Timing" | on page 10 |

### 1.1.1 Maximum Ratings

#### CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (for example, either GND or  $V_{DD}$ ). The suggested value for a pull-up or pull-down resistor is 4.7 k $\Omega$ .

#### NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification will never occur in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 lists the maximum ratings.

**Table 2. Maximum Ratings**

| Rating <sup>1</sup>   | Symbol  | Value <sup>1, 2</sup>  | Unit |
|---|---|------------------------|------|
| Supply Voltage  | $V_{\text{CORE\_VDD}}, V_{\text{PLLD\_VDD}}$  | -0.3 to + 1.26         | V    |
|   | $V_{\text{PLL\_VDD}}, V_{\text{IO\_VDD}}, V_{\text{IO\_VDD\_25}}, V_{\text{PLLA\_VDD}}$ | -0.3 to + 4.0          | V    |
| Maximum CORE_VDD power supply ramp time   | $T_r$   | 10                     | ms   |
| Input Voltage per pin excluding VDD and GND   | $V_{\text{IN}}$   | GND – 0.3 to 5.5 V     | V    |
| Current drain per pin excluding V <sub>DD</sub> and GND (Except for pads listed below)      | I   | 12                     | mA   |
| LSYNC_OUT   | $I_{\text{lsync\_out}}$   | 5                      | mA   |
| LCLK  | $I_{\text{clk}}$  | 5                      | mA   |
| LALE  | $I_{\text{ale}}$  | 5                      | mA   |
| TDO   | $I_{\text{JTAG}}$   | 12                     | mA   |
| Operating temperature range<br>• F <sub>sys</sub> < 200 MHz<br>• F <sub>sys</sub> < 250 MHz | $T_J$   | -40 to +100<br>0 to 90 | °C   |
| Storage temperature   | $T_{\text{STG}}$  | -65 to +150            | °C   |
| ESD protected voltage (Human Body Model)  | —   | 2000                   | V    |
| ESD protected voltage (Charged Device Model)<br>• All pins<br>• Corner pins                 | —   | 500<br>750             | V    |

**Note:**

1. GND = 0 V,  $T_J = -40^\circ\text{C}$  to  $100^\circ\text{C}$ , CL = 50 pF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.

## 1.1.2 Thermal Characteristics

Table 3 lists the thermal characteristics.

**Table 3. Thermal Characteristics**

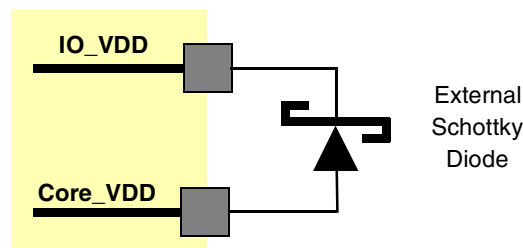
| Characteristic  |                         | Symbol                           | LQFP Values                     | Unit                        |
|---|-------------------------|----------------------------------|---------------------------------|-----------------------------|
| Natural Convection, Junction-to-ambient thermal resistance <sup>1,2</sup> | Single layer board (1s) | $R_{\theta JA}$ or $\theta_{JA}$ | 57 for 80 QFP<br>49 for 144 QFP | $^{\circ}\text{C}/\text{W}$ |
|   | Four layer board (2s2p) |                                  | 44 for 80 QFP<br>40 for 144 QFP | $^{\circ}\text{C}/\text{W}$ |
| Junction-to-case thermal resistance <sup>3</sup>                          |                         | $R_{\theta JC}$ or $\theta_{JC}$ | 10 for 80 QFP<br>9 for 144 QFP  | $^{\circ}\text{C}/\text{W}$ |

**Note:**

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

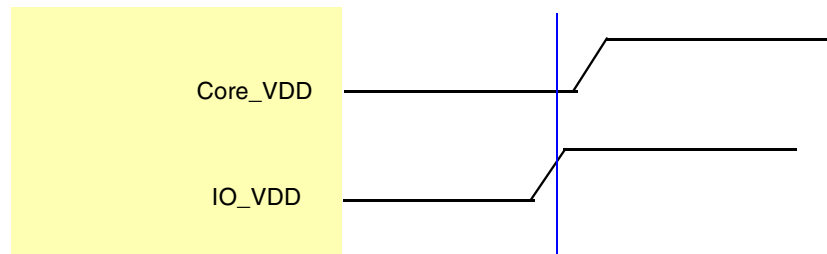
## 1.1.3 Power Requirements

To prevent high current conditions due to possible improper sequencing of the power supplies, use an external Schottky diode as shown in Figure 3, connected between the DSP56724/DSP56725 IO\_VDD and Core\_VDD power pins.



**Figure 3. Prevent High Current Conditions by Using External Schottky Diode**

If an external Schottky diode is not used (to prevent a high current condition at power-up), then IO\_VDD must be applied ahead of Core\_VDD, as shown in Figure 4.



**Figure 4. Prevent High Current Conditions by Applying IO\_VDD Before Core\_VDD**

For correct operation of the internal power-on reset logic, the Core\_VDD ramp rate (Tr) to full supply must be less than 10 ms, as shown in Figure 4.

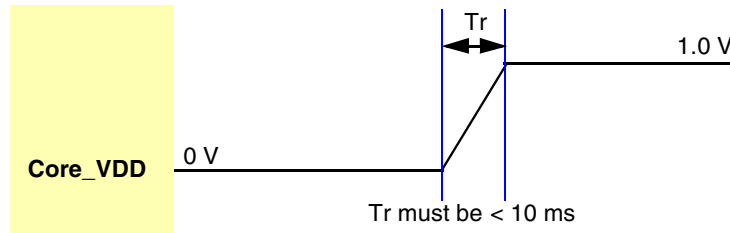


Figure 5. Ensure Correct Operation of Power-On Reset with Fast Ramp of Core\_VDD

## 1.1.4 DC Electrical Characteristics

Table 4. DC Electrical Characteristics

| Characteristics   | Symbol   | Min          | Typ        | Max                      | Unit |
|---|--|--------------|------------|--------------------------|------|
| Core Supply voltages<br>• Fsys < 200 MHz<br>• Fsys < 250 MHz  | V <sub>CORE_VDD</sub> ,<br>V <sub>PLLD_VDD</sub>                           | 0.95<br>1.14 | 1.0<br>1.2 | 1.05<br>1.26             | V    |
| IO Supply voltages  | V <sub>IO_VDD</sub> ,<br>V <sub>PLL_P_VDD</sub> ,<br>V <sub>PLLA_VDD</sub> | 3.14         | 3.3        | 3.45                     | V    |
| Input high voltage  | V <sub>IH</sub>  | 2.0          | —          | V <sub>IO_VDD</sub> + 2V | V    |
| <b>Note:</b> To avoid a high current condition and possible system damage, all 3.3-V and 2.5-V supplies must rise before the 1.0-V supplies rise. |  |              |            |                          |      |
| Input low voltage   | V <sub>IL</sub>  | -0.3         | —          | 0.8                      | V    |
| Input leakage current   | I <sub>IN</sub>  | —            | —          | ± 80                     | μA   |
| Clock pin Input Capacitance (EXTAL)   | C <sub>IN</sub>  | —            | 2.057      | —                        | pF   |
| High impedance (off-state) input current (@ 3.3 V or 0 V)   | I <sub>TSI</sub>   | -10          | —          | 10                       | μA   |
| Output high voltage<br>I <sub>OH</sub> = -12 mA<br>LSYNC_OUT, LALE, LCLK Pins I <sub>OH</sub> = -16 mA,<br>TDO Pin I <sub>OH</sub> = -24 mA       | V <sub>OH</sub>  | 2.4          | —          | —                        | V    |
| Output low voltage<br>I <sub>OL</sub> = 12 mA<br>LSYNC_OUT, LALE, LCLK Pins I <sub>OL</sub> = 16 mA,<br>TDO Pins I <sub>OL</sub> = 24 mA          | V <sub>OL</sub>  | —            | —          | 0.4                      | V    |
| Internal pull-up resistor   | R <sub>PU</sub>  | 63           | 92         | 142                      | kΩ   |
| Internal pull-down resistor   | R <sub>PD</sub>  | 57           | 91         | 159                      | kΩ   |
| Internal supply current <sup>1</sup> (core only) operating at Fsys < 200 MHz<br>• In Normal mode<br>• In Wait mode                                | I <sub>CCI</sub><br>I <sub>CCW</sub>                                       | —<br>—       | 90<br>60   | 280<br>250               | mA   |

**Table 4. DC Electrical Characteristics (Continued)**

| Characteristics  | Symbol           | Min | Typ | Max | Unit |
|--|------------------|-----|-----|-----|------|
| • In Stop mode <sup>2</sup>  | I <sub>CCS</sub> | —   | 30  | 220 | mA   |
| Internal supply current <sup>1</sup> (core only) operating at F <sub>sys</sub> < 250 MHz |                  |     |     |     |      |
| • In Normal mode   | I <sub>CCI</sub> | —   | 140 | 340 | mA   |
| • In Wait mode   | I <sub>CCW</sub> | —   | 90  | 290 | mA   |
| • In Stop mode <sup>2</sup>  | I <sub>CCS</sub> | —   | 40  | 240 | mA   |
| Input capacitance  | C <sub>IN</sub>  | —   | —   | 10  | pF   |

**Note:**

1. The Current Consumption section provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (for example, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current with F<sub>sys</sub> < 200 MHz is measured with V<sub>CORE\_VDD</sub> = 1.0 V, V<sub>DD\_IO</sub> = 3.3 V at T<sub>J</sub> = 25° C. Maximum internal supply current is measured with V<sub>CORE\_VDD</sub> = 1.05 V, V<sub>IO\_VDD</sub> = 3.6 V at T<sub>J</sub> = 100° C. Typical internal supply current with F<sub>sys</sub> < 250 MHz is measured with V<sub>CORE\_VDD</sub> = 1.2 V, V<sub>DD\_IO</sub> = 3.3 V at T<sub>J</sub> = 25° C. Maximum internal supply current is measured with V<sub>CORE\_VDD</sub> = 1.26 V, V<sub>IO\_VDD</sub> = 3.6 V at T<sub>J</sub> = 90° C.
2. In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (that is, not allowed to float).

## 1.1.5 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V<sub>IL</sub> maximum of 0.8 V and a V<sub>IH</sub> minimum of 2.0 V for all pins. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. For all pins, output levels are measured with the production test machine V<sub>OL</sub> and V<sub>OH</sub> reference levels set at 0.4 V and 2.4 V, respectively.

## 1.1.6 Internal Clocks

Table 5 lists the internal clocks.

**Table 5. Internal Clocks**

| No. | Characteristics       | Symbol | Min | Typ | Max | Unit | Condition     |
|-----|-----------------------|--------|-----|-----|-----|------|---------------|
| 1   | Comparison Frequency  | Fref   | 2   | —   | 8   | MHz  | Fref = Fin/NR |
| 2   | Input Clock Frequency | Fin    | 2   | —   | 248 | MHz  | —             |
|     | • with PLL enabled    |        | —   |     | 200 |      |               |
|     | • with PLL disabled   |        |     |     |     |      |               |



**Table 5. Internal Clocks (Continued)**

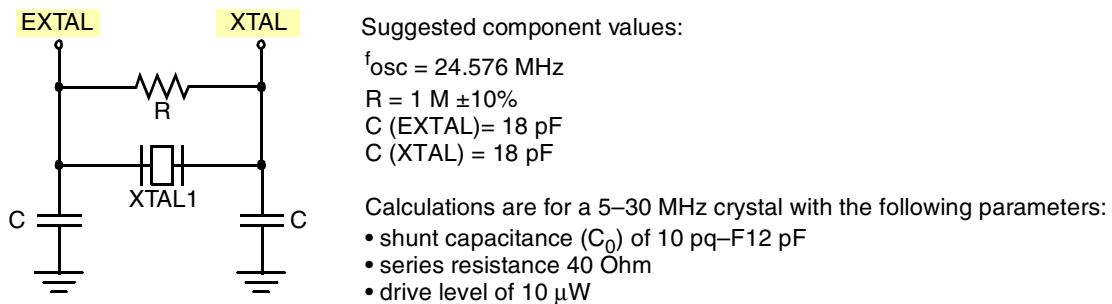
| No. | Characteristics   | Symbol | Min        | Typ | Max                      | Unit | Condition   |
|-----|---|--------|------------|-----|--------------------------|------|---|
| 3   | PLL VCO Frequency   | Fvco   | 200        | —   | 500                      | MHz  | $F_{vco} = (F_{in} * NF)/NR$                      |
| 4   | Output Clock Frequency <sup>[1] [2]</sup> <ul style="list-style-type: none"> <li>with PLL enabled</li> <li>with PLL disabled</li> </ul> | Fout   | 25<br>—    | —   | 200 or 250<br>200 or 250 | MHz  | $F_{out} = F_{vco}/NO$<br>$F_{out} = F_{in}$      |
| 5   | System Clock Frequency <ul style="list-style-type: none"> <li>with PLL enabled<sup>[2]</sup></li> <li>with PLL disabled</li> </ul>      | Fsys   | 0.195<br>0 | —   | 200 or 250<br>200        | MHz  | $F_{sys} = F_{out}/2^{DF}$<br>$F_{sys} = F_{out}$ |

**Note:**

1. Fin = External frequency  
 NF = Multiplication Factor  
 NR = Predivision Factor  
 NO = Output Divider  
 DF = Division Factor
2. Maximum frequency of 200 MHz supported at  $0.95\text{ V} < V_{DD\_CORE} < 1.05\text{ V}$  and  $-40 < T_j < 100^\circ\text{ C}$   
 Maximum frequency of 250 MHz supported at  $1.14\text{ V} < V_{DD\_CORE} < 1.26\text{ V}$  and  $0 < T_j < 90^\circ\text{ C}$

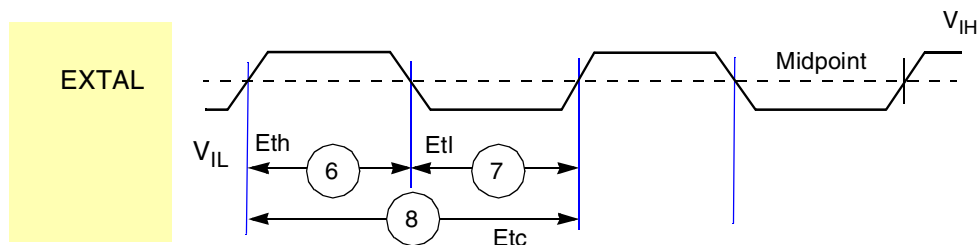
### 1.1.7 External Clock Operation

The DSP56724/DSP56725 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; see Figure 6.



**Figure 6. Using the On-Chip Oscillator**

If the DSP56724/DSP56725 system clock is an externally supplied square wave voltage source, it is connected to EXTAL (Figure 7). When the external square wave source is connected to EXTAL, the XTAL pin is not used.



Note: The midpoint is  $0.5(V_{IH} + V_{IL})$ .

**Figure 7. External Clock Timing**

Table 6 lists the clock operation.

**Table 6. Clock Operation**

| No. | Characteristics   | Symbol | Min                 | Max         | Units |
|-----|---|--------|---------------------|-------------|-------|
| 6   | EXTAL input high <sup>1</sup><br>(40% to 60% duty cycle)<br>• Crystal oscillator<br>• Square wave input | Eth    | 16.67<br>2.5        | 100<br>inf  | ns    |
| 7   | EXTAL input low <sup>1</sup><br>(40% to 60% duty cycle)<br>• Crystal oscillator<br>• Square wave input  | Etl    | 16.67<br>2.5        | 100<br>inf  | ns    |
| 8   | EXTAL cycle time<br>• With PLL disabled<br>• With PLL enabled   | Etc    | 5<br>33.3           | inf<br>500  | ns    |
| 9   | Instruction cycle time<br>• With PLL disabled<br>• With PLL enabled                                     | Tc     | 5<br>4 <sup>4</sup> | inf<br>5120 | ns    |

**Note:**

1. Measured at 50% of the input transition.
2. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.
3. Maximum frequency of 200 MHz supported at  $0.95\text{ V} < V_{\text{VDD\_CORE}} < 1.05\text{ V}$  and  $-40 < T_j < 100^\circ\text{ C}$   
Maximum frequency of 250 MHz supported at  $1.14\text{ V} < V_{\text{VDD\_CORE}} < 1.26\text{ V}$  and  $0 < T_j < 90^\circ\text{ C}$
4.  $\text{PLL}_{\text{LOCK}} = 200\ \mu\text{s}$ .

## 1.1.8 Reset, Stop, Mode Select, and Interrupt Timing

Table 7 lists the reset, stop, mode select, and interrupt timing.

**Table 7. Reset, Stop, Mode Select, and Interrupt Timing**

| No. | Characteristics   | Expression                                  | Min | Max | Unit |
|-----|---|---|-----|-----|------|
| 10  | Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value <sup>3</sup>  | —   | —   | 11  | ns   |
| 11  | Required $\overline{\text{RESET}}$ duration <sup>4</sup><br>• Power on, external clock generator, PLL disabled<br>• Power on, external clock generator, PLL enabled | $2 \times T_C$                              | 10  | —   | ns   |
|     |   | $2 \times T_C$                              | 10  | —   | ns   |
| 13  | Syn reset deassert delay time<br>• Minimum<br>• Maximum (PLL enabled)   | $2 \times T_C$                              | 10  | —   | ns   |
|     |   | $(2 \times T_C) + \text{PLL}_{\text{LOCK}}$ | 200 | —   | us   |
| 14  | Mode select setup time  | —   | 10  | —   | ns   |
| 15  | Mode select hold time   | —   | 12  | —   | ns   |
| 16  | Minimum edge-triggered interrupt request assertion width  | —   | 7   | —   | ns   |
| 17  | Minimum edge-triggered interrupt request deassertion width  | —   | 4   | —   | ns   |
| 18  | Delay from interrupt trigger to interrupt code execution  | $10 \times T_C + 4$                         | 54  | —   | ns   |

**Table 7. Reset, Stop, Mode Select, and Interrupt Timing (Continued)**

| No. | Characteristics   | Expression                        | Min | Max  | Unit          |
|-----|---|-----------------------------------|-----|------|---------------|
| 19  | Duration of level sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting Stop) <sup>1, 2, 3</sup>  |                                   |     |      |               |
|     | • PLL is active during Stop and Stop delay is enabled (OMR Bit 6 = 0)   | $(128 \text{ Kbytes} \times T_C)$ | 655 | —    | $\mu\text{s}$ |
|     | • PLL is active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)   | $25 \times T_C$                   | 125 | —    | ns            |
|     | • PLL is not active during Stop and Stop delay is enabled (OMR Bit 6 = 0)   | $(128K \times T_C) + PLL_{LOCK}$  | 855 | —    | $\mu\text{s}$ |
|     | • PLL is not active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)   | $(25 \times T_C) + PLL_{LOCK}$    | 200 | —    | $\mu\text{s}$ |
| 20  | • Delay from $\overline{IRQA}$ , $\overline{IRQB}$ , $\overline{IRQC}$ , $\overline{IRQD}$ , $\overline{NMI}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution <sup>1</sup> | $10 \times T_C + 3.8$             | —   | 53.8 | ns            |
| 21  | Interrupt Requests Rate <sup>1</sup>  |                                   |     |      |               |
|     | • ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1, Timer, Timer_1  | $12 \times T_C$                   | —   | 60.0 | ns            |
|     | • DMA   | $8 \times T_C$                    | —   | 40.0 | ns            |
|     | • $\overline{IRQ}$ , $\overline{NMI}$ (edge trigger)  | $8 \times T_C$                    | —   | 40.0 | ns            |
|     | • $\overline{IRQ}$ (level trigger)  | $12 \times T_C$                   | —   | 60.0 | ns            |
| 22  | DMA Requests Rate   |                                   |     |      |               |
|     | • Data read from ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1   | $6 \times T_C$                    | —   | 30.0 | ns            |
|     | • Data write to ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1  | $7 \times T_C$                    | —   | 35.0 | ns            |
|     | • Timer, Timer_1  | $2 \times T_C$                    | —   | 10.0 | ns            |
|     | • $\overline{IRQ}$ , $\overline{NMI}$ (edge trigger)  | $3 \times T_C$                    | —   | 15.0 | ns            |

**Note:**

- When using fast interrupts and when  $\overline{IRQA}$ ,  $\overline{IRQB}$ ,  $\overline{IRQC}$ , and  $\overline{IRQD}$  are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
- For PLL disable, if using an external clock (PCTL Bit 13 = 1), no stabilization delay is required and recovery time will be defined by the OMR Bit 6 settings.  
For PLL enable, (if bit 12 of the PCTL register is 0), the PLL is shut down during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 200  $\mu\text{s}$ .
- Periodically sampled and not 100% tested.
- $\overline{RESET}$  duration is measured during the time in which  $\overline{RESET}$  is asserted,  $V_{DD}$  is valid, and the EXTAL input is active and valid. When  $V_{DD}$  is valid, but the other “required  $\overline{RESET}$  duration” conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

Figure 8 shows the reset timing diagram.

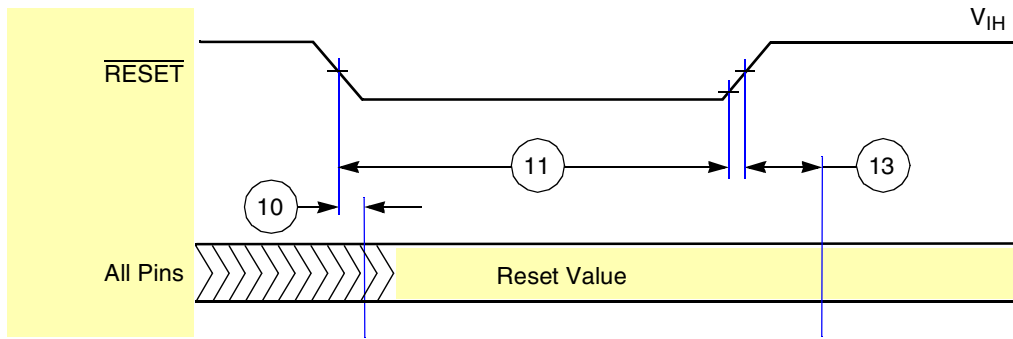


Figure 8. Reset Timing

Figure 9 shows external fast interrupt timing diagram.

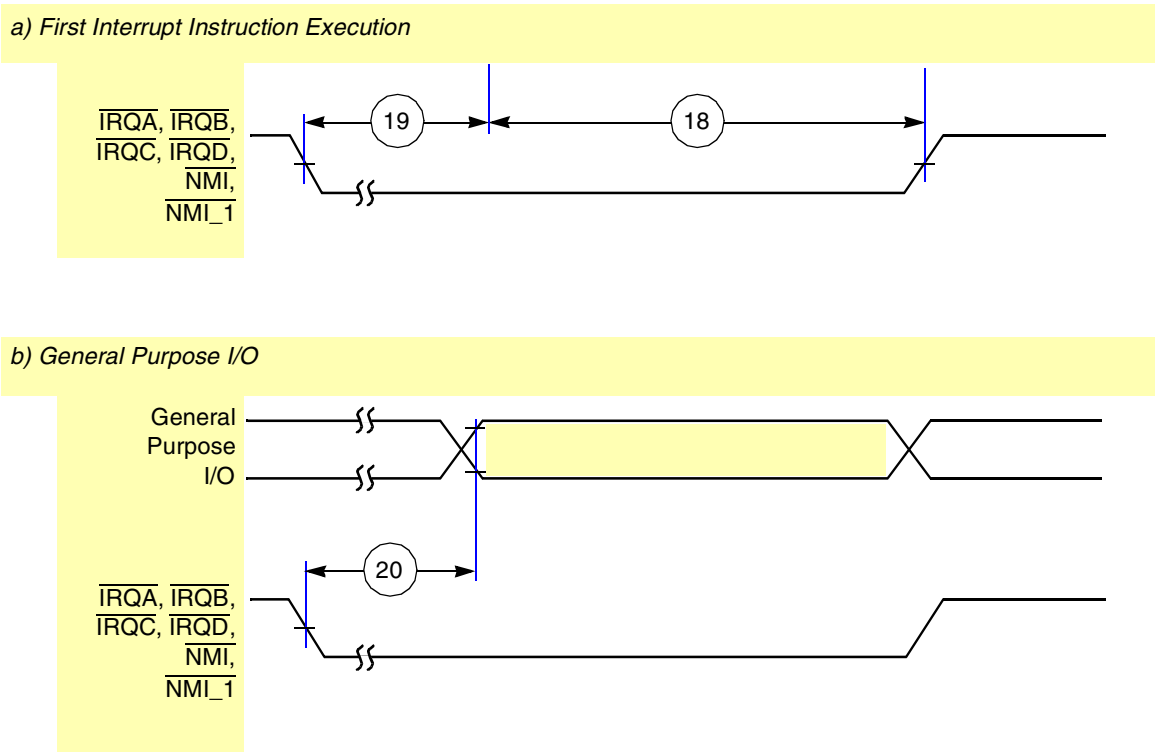


Figure 9. External Fast Interrupt Timing

Figure 10 shows external interrupt timing (negative edge-triggered).

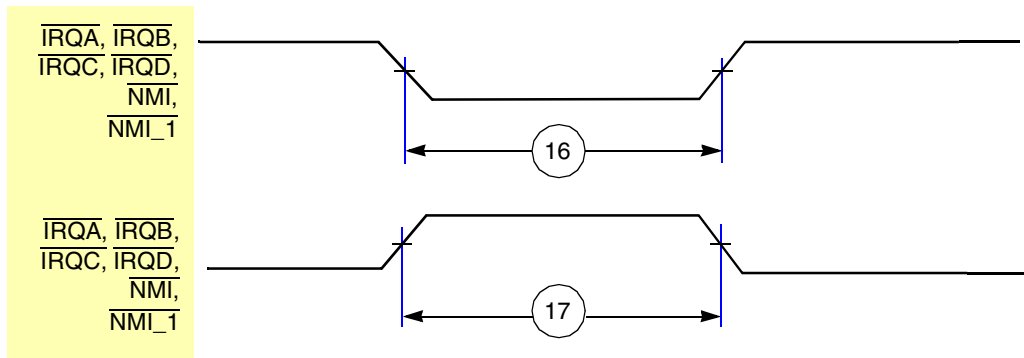


Figure 10. External Interrupt Timing (Negative Edge-Triggered)

Figure 11 shows MODE select set-up and hold time diagram.

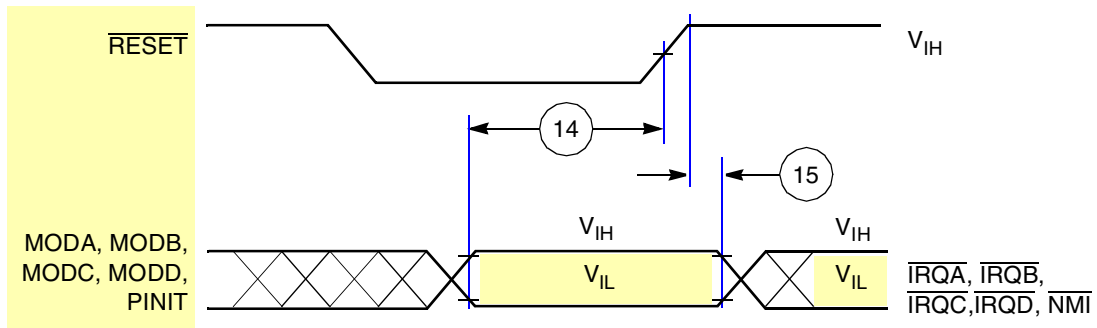


Figure 11. MODE Select Set-Up and Hold Time

## 1.2 Module-Level Specifications

Table 8 provides a quick reference to the subsections of this section.

Table 8. Module-Level Specifications

| For   | See        |
|---|------------|
| Section 1.2.1, “Serial Host Interface SPI Protocol Timing”                    | on page 4  |
| Section 1.2.2, “Serial Host Interface (SHI) I <sup>2</sup> C Protocol Timing” | on page 6  |
| Section 1.2.3, “Programming the SHI I <sup>2</sup> C Serial Clock”            | on page 6  |
| Section 1.2.4, “Enhanced Serial Audio Interface Timing”                       | on page 7  |
| Section 1.2.5, “GPIO Timing”  | on page 28 |
| Section 1.2.6, “JTAG Timing”  | on page 29 |
| Section 1.2.7, “Watchdog Timer Timing”  | on page 31 |
| Section 1.2.8, “S/PDIF Timing”  | on page 32 |
| Section 1.2.9, “EMC Timing Specifications—DSP56724”                           | on page 33 |

## 1.2.1 Serial Host Interface SPI Protocol Timing

Table 9 lists the serial host interface SPI protocol timing.

**Table 9. Serial Host Interface SPI Protocol Timing**

| No. | Characteristics <sup>1,3,4</sup>                     | Mode         | Filter Mode | Expression               | Min   | Max | Unit |
|-----|--|--------------|-------------|--------------------------|-------|-----|------|
| 23  | Minimum serial clock cycle = $t_{SPICC}(\text{min})$ | Master/Slave | Bypassed    | $10 \times T_C + 9$      | 59.0  | —   | ns   |
|     |  |              | Very Narrow | $10 \times T_C + 9$      | 59.0  | —   | ns   |
|     |  |              | Narrow      | $10 \times T_C + 133$    | 183.0 | —   | ns   |
|     |  |              | Wide        | $10 \times T_C + 333$    | 383.0 | —   | ns   |
| XX  | Tolerable Spike width on data or clock in.           | —            | Bypassed    | —                        | —     | 0   | ns   |
|     |  |              | Very Narrow | —                        | —     | 10  | ns   |
|     |  |              | Narrow      | —                        | —     | 50  | ns   |
|     |  |              | Wide        | —                        | —     | 100 | ns   |
| 24  | Serial clock high period                             | Master       | Bypassed    | $0.5 \times (t_{SPICC})$ | 29.5  | —   | ns   |
|     |  |              | Very Narrow | $0.5 \times (t_{SPICC})$ | 29.5  | —   | ns   |
|     |  |              | Narrow      | $0.5 \times (t_{SPICC})$ | 91.5  | —   | ns   |
|     |  |              | Wide        | $0.5 \times (t_{SPICC})$ | 191   | —   | ns   |
|     |  | Slave        | Bypassed    | $2.5 \times T_C + 12$    | 24    | —   | ns   |
|     |  |              | Very Narrow | $2.5 \times T_C + 12$    | 24    | —   | ns   |
|     |  |              | Narrow      | $2.5 \times T_C + 102$   | 114.5 | —   | ns   |
|     |  |              | Wide        | $2.5 \times T_C + 189$   | 201.5 | —   | ns   |
| 25  | Serial clock low period                              | Master       | Bypassed    | $0.5 \times (t_{SPICC})$ | 29.5  | —   | ns   |
|     |  |              | Very Narrow | $0.5 \times (t_{SPICC})$ | 29.5  | —   | ns   |
|     |  |              | Narrow      | $0.5 \times (t_{SPICC})$ | 91.5  | —   | ns   |
|     |  |              | Wide        | $0.5 \times t_{SPICC}$   | 191   | —   | ns   |
|     |  | Slave        | Bypassed    | $2.5 \times T_C + 12$    | 24    | —   | ns   |
|     |  |              | Very Narrow | $2.5 \times T_C + 12$    | 24    | —   | ns   |
|     |  |              | Narrow      | $2.5 \times T_C + 102$   | 114.5 | —   | ns   |
|     |  |              | Wide        | $2.5 \times T_C + 189$   | 201.5 | —   | ns   |
| 26  | Serial clock rise/fall time                          | Master       | —           | —                        | —     | —   | ns   |
|     |  | Slave        | —           | —                        | —     | 5   | ns   |

**Table 9. Serial Host Interface SPI Protocol Timing (Continued)**

| No. | Characteristics <sup>1,3,4</sup>                                | Mode          | Filter Mode | Expression            | Min   | Max  | Unit |
|-----|---|---------------|-------------|-----------------------|-------|------|------|
| 27  | $\overline{SS}$ assertion to first SCK edge<br>CPHA = 0         | Slave         | Bypassed    | $3.5 \times T_C + 15$ | 32.5  | —    | ns   |
|     |   |               | Very Narrow | $3.5 \times T_C + 5$  | 22.5  | —    | ns   |
|     |   |               | Narrow      | —                     | 0     | —    | ns   |
|     |   |               | Wide        | —                     | 0     | —    | ns   |
|     | CPHA = 1  | Slave         | Bypassed    | —                     | 10    | —    | ns   |
|     |   |               | Very Narrow | —                     | 0     | —    | ns   |
|     |   |               | Narrow      | —                     | 0     | —    | ns   |
|     |   |               | Wide        | —                     | 0     | —    | ns   |
| 28  | Last SCK edge to $\overline{SS}$ not asserted                   | Slave         | Bypassed    | —                     | 12    | —    | ns   |
|     |   |               | Very Narrow | —                     | 22    | —    | ns   |
|     |   |               | Narrow      | —                     | 100   | —    | ns   |
|     |   |               | Wide        | —                     | 200   | —    | ns   |
| 29  | Data input valid to SCK edge (data input set-up time)           | Master /Slave | Bypassed    | —                     | 0     | —    | ns   |
|     |   |               | Very Narrow | —                     | 0     | —    | ns   |
|     |   |               | Narrow      | —                     | 0     | —    | ns   |
|     |   |               | Wide        | —                     | 0     | —    | ns   |
| 30  | SCK last sampling edge to data input not valid                  | Master /Slave | Bypassed    | $2 \times T_C + 10$   | 20    | —    | ns   |
|     |   |               | Very Narrow | $2 \times T_C + 30$   | 40    | —    | ns   |
|     |   |               | Narrow      | $2 \times T_C + 60$   | 70    | —    | ns   |
|     |   |               | Wide        | —                     | 100.0 | —    | ns   |
| 31  | $\overline{SS}$ assertion to data out active                    | Slave         | —           | —                     | 5     | —    | ns   |
| 32  | $\overline{SS}$ deassertion to data high impedance <sup>2</sup> | Slave         | —           | —                     | —     | 9    | ns   |
| 33  | SCK edge to data out valid (data out delay time)                | Master /Slave | Bypassed    | —                     | —     | 46.2 | ns   |
|     |   |               | Very Narrow | —                     | —     | 270  | ns   |
|     |   |               | Narrow      | —                     | —     | 376  | ns   |
|     |   |               | Wide        | —                     | —     | 521  | ns   |
| 34  | SCK edge to data out not valid (data out hold time)             | Master /Slave | Bypassed    | —                     | 11.67 | —    | ns   |
|     |   |               | Very Narrow | —                     | 15    | —    | ns   |
|     |   |               | Narrow      | —                     | 55    | —    | ns   |
|     |   |               | Wide        | —                     | 105   | —    | ns   |
| 35  | $\overline{SS}$ assertion to data out valid (CPHA = 0)          | Slave         | —           | —                     | —     | 14.0 | ns   |

**Table 9. Serial Host Interface SPI Protocol Timing (Continued)**

| No. | Characteristics <sup>1,3,4</sup>  | Mode   | Filter Mode | Expression   | Min   | Max | Unit |
|-----|---|--------|-------------|--|-------|-----|------|
| 36  | First SCK sampling edge to $\overline{\text{HREQ}}$ output deassertion  | Slave  | Bypassed    | —  | 45    | —   | ns   |
|     |   |        | Very Narrow | —  | 55    | —   | ns   |
|     |   |        | Narrow      | —  | 95    | —   | ns   |
|     |   |        | Wide        | —  | 145   | —   | ns   |
| 37  | Last SCK sampling edge to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 1)                                     | Slave  | Bypassed    | —  | 50.0  | —   | ns   |
|     |   |        | Very Narrow | —  | 60.0  | —   | ns   |
|     |   |        | Narrow      | —  | 100.0 | —   | ns   |
|     |   |        | Wide        | —  | 150.0 | —   | ns   |
| 38  | $\overline{\text{SS}}$ deassertion to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 0)                         | Slave  | —           | —  | 45.0  | —   | ns   |
| 39  | $\overline{\text{SS}}$ deassertion pulse width (CPHA = 0)   | Slave  | —           | $T_C + 6$  | 11.0  | —   | ns   |
| 40  | $\overline{\text{HREQ}}$ in assertion to first SCK edge   | Master | —           | $0.5 \times T_{\text{SPICCC}} + 3.0 \times T_C + 43$ | 96.0  | —   | ns   |
| 41  | $\overline{\text{HREQ}}$ in deassertion to last SCK sampling edge ( $\overline{\text{HREQ}}$ in set-up time) (CPHA = 1) | Master | —           | —  | 0     | —   | ns   |
| 42  | First SCK edge to $\overline{\text{HREQ}}$ in not asserted ( $\overline{\text{HREQ}}$ in hold time)                     | Master | —           | —  | 0     | —   | ns   |
| 43  | $\overline{\text{HREQ}}$ assertion width  | Master | —           | $3.0 \times T_C$                                     | 15    | —   | ns   |

**Note:**

1.  $0.95 \text{ V} < V_{\text{VDD\_CORE}} < 1.05 \text{ V}$  and  $T_J < 100^\circ \text{ C}$ ,  $C_L = 50 \text{ pF}$
2. Periodically sampled, not 100% tested
3. All times assume noise free inputs.
4. All times assume internal clock frequency of 200 MHz.
5. SHI\_1 specs match those of SHI
6. Slave timings should equal the serial clock high period + the serial clock low period.



Figure 12 shows the SPI master timing (CPHA = 0).

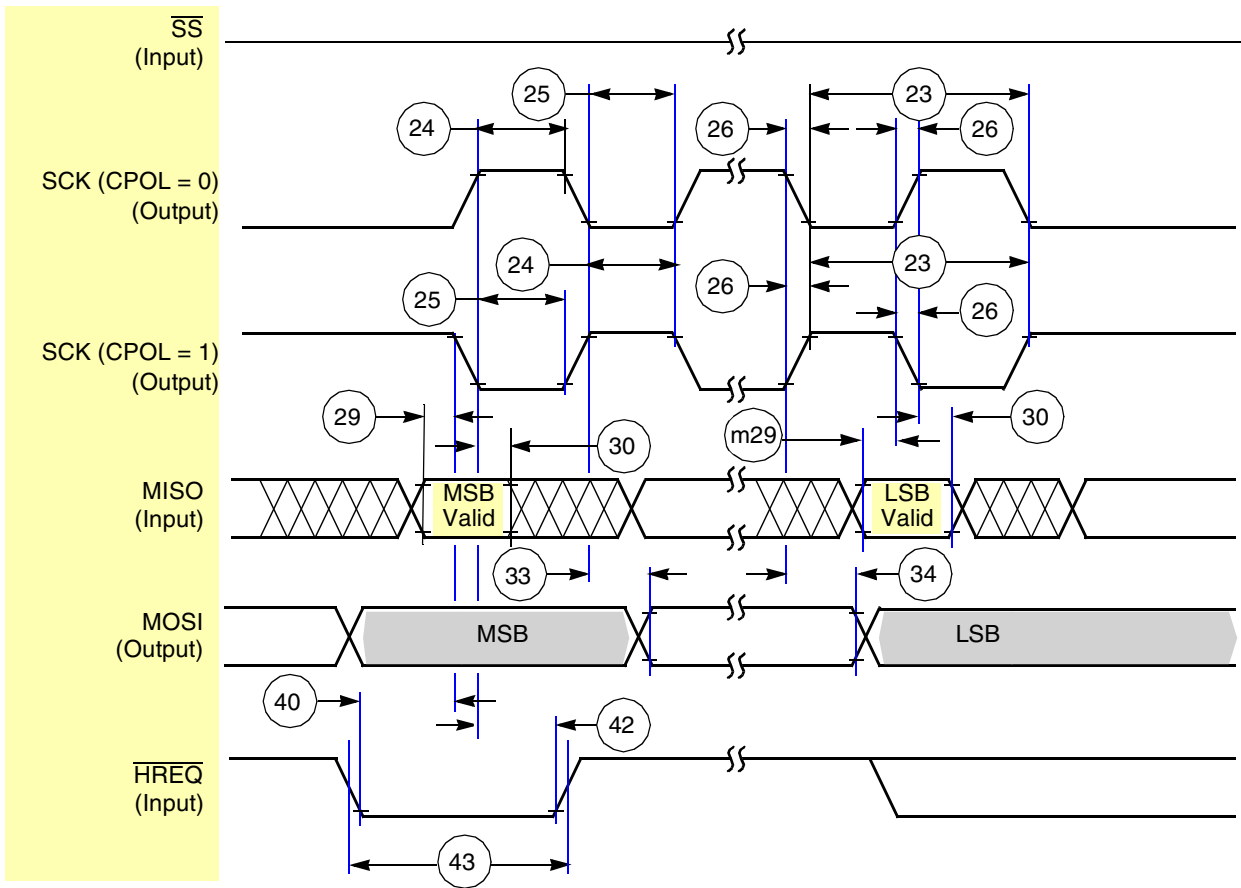


Figure 12. SPI Master Timing (CPHA = 0)

Figure 13 shows the SPI master timing (CPHA = 1).

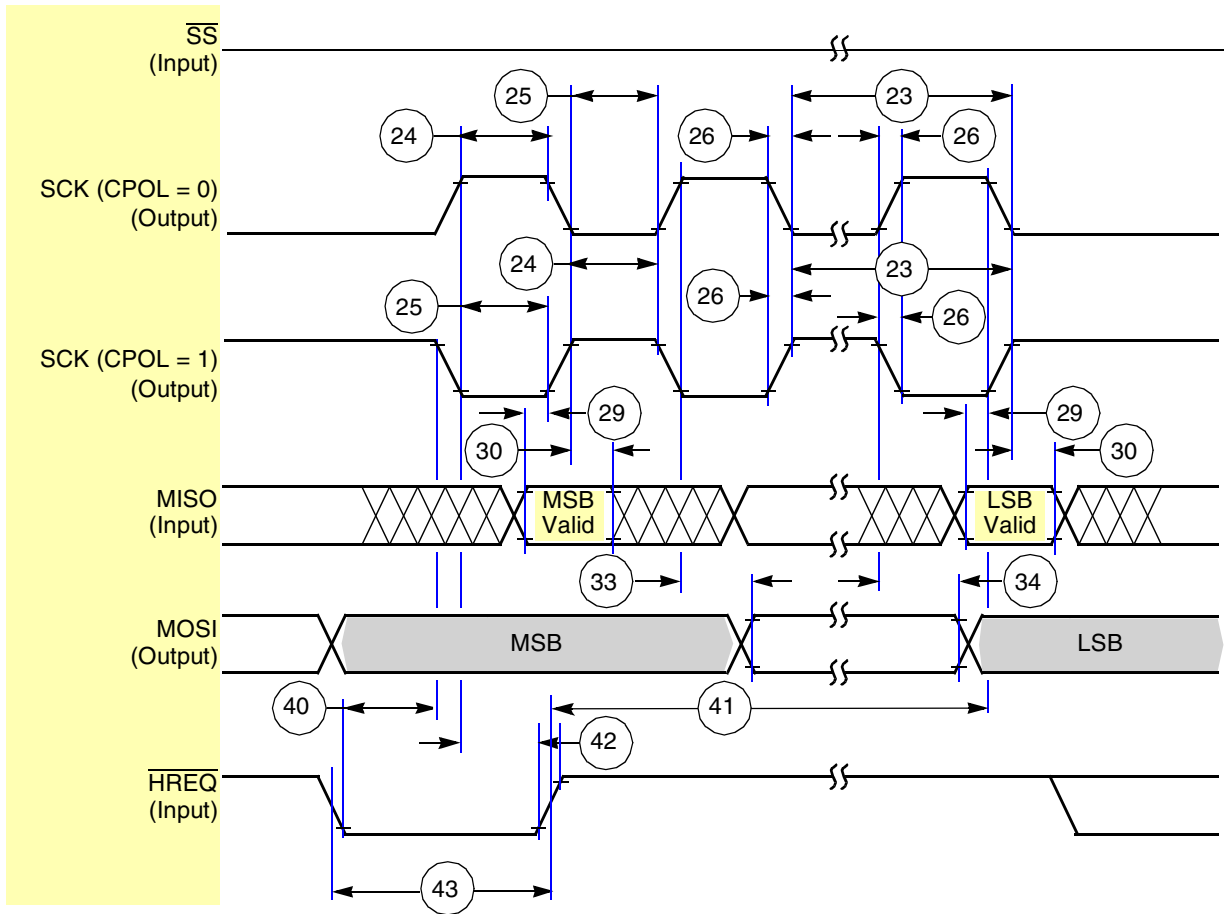


Figure 13. SPI Master Timing (CPHA = 1)

Figure 14 shows the SPI slave timing (CPHA = 0).

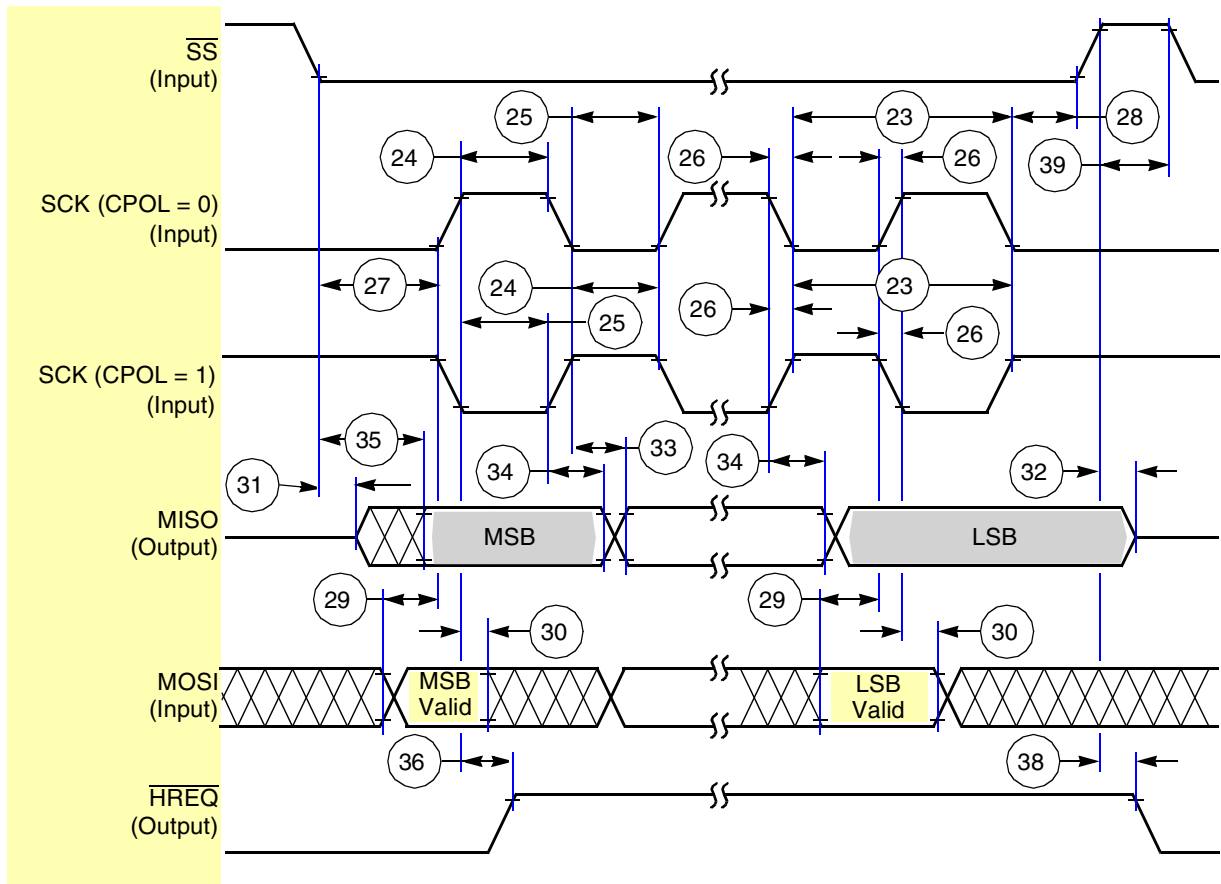


Figure 14. SPI Slave Timing (CPHA = 0)

Figure 15 shows the SPI slave timing (CPHA = 1).

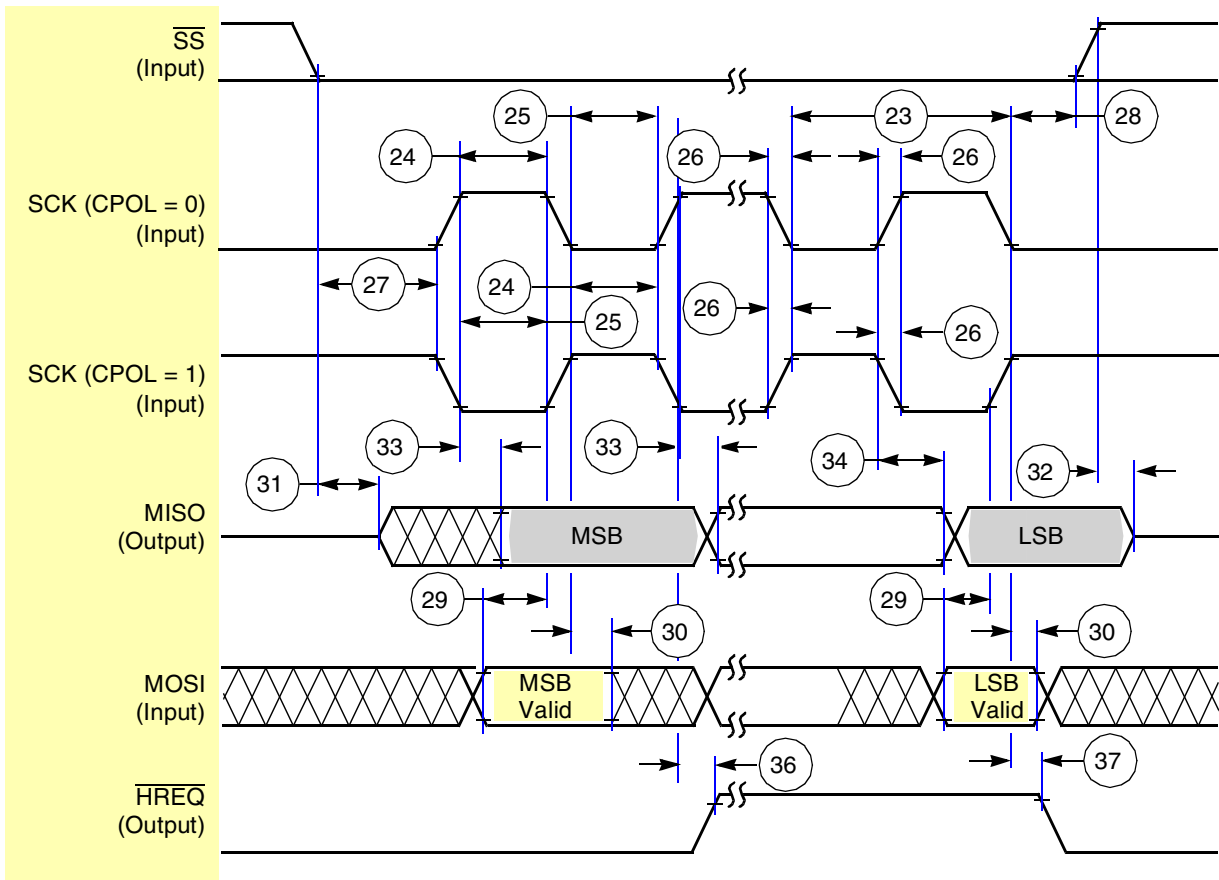


Figure 15. SPI Slave Timing (CPHA = 1)

## 1.2.2 Serial Host Interface (SHI) I<sup>2</sup>C Protocol Timing

Table 10 lists the SHI I<sup>2</sup>C protocol timing diagram.

Table 10. SHI I<sup>2</sup>C Protocol Timing

| Standard I <sup>2</sup> C |   |                       |          |                      |           |                      |         |
|---------------------------|---|-----------------------|----------|----------------------|-----------|----------------------|---------|
| No.                       | Characteristics <sup>1,2,3,4,5</sup>  | Symbol/<br>Expression | Standard |                      | Fast-Mode |                      | Unit    |
|                           |   |                       | Min      | Max                  | Min       | Max                  |         |
| XX                        | Tolerable Spike Width on SCL or SDA<br>Filters Bypassed<br>Very Narrow Filters enabled<br>Narrow Filters enabled<br>Wide Filters enabled. | —                     | —        | 0<br>10<br>50<br>100 | —         | 0<br>10<br>50<br>100 | ns      |
| 44                        | SCL clock frequency   | $F_{SCL}$             | —        | 100                  | —         | 400                  | kHz     |
| 44                        | SCL clock cycle   | $T_{SCL}$             | 10       | —                    | 2.5       | —                    | $\mu$ s |
| 45                        | Bus free time   | $T_{BUF}$             | 4.7      | —                    | 1.3       | —                    | $\mu$ s |
| 46                        | Start condition set-up time   | $T_{SUSTA}$           | 4.7      | —                    | 0.6       | —                    | $\mu$ s |

Table 10. SHI I<sup>2</sup>C Protocol Timing (Continued)

| Standard I <sup>2</sup> C |   |                       |                          |      |           |     |       |    |
|---------------------------|---|-----------------------|--------------------------|------|-----------|-----|-------|----|
| No.                       | Characteristics <sup>1,2,3,4,5</sup>  | Symbol/<br>Expression | Standard                 |      | Fast-Mode |     | Unit  |    |
|                           |   |                       | Min                      | Max  | Min       | Max |       |    |
| 47                        | Start condition hold time   | T <sub>HD;STA</sub>   | 4.0                      | —    | 0.6       | —   | μs    |    |
| 48                        | SCL low period  | T <sub>LOW</sub>      | 4.7                      | —    | 1.3       | —   | μs    |    |
| 49                        | SCL high period   | T <sub>HIGH</sub>     | 4.0                      | —    | 1.3       | —   | μs    |    |
| 50                        | SCL and SDA rise time <sup>7</sup>  | T <sub>R</sub>        | —                        | 1000 | —         | 300 | ns    |    |
| 51                        | SCL and SDA fall time <sup>7</sup>  | T <sub>F</sub>        | —                        | 5.0  | —         | 5.0 | ns    |    |
| 52                        | Data set-up time  | T <sub>SU;DAT</sub>   | 250                      | —    | 100       | —   | ns    |    |
| 53                        | Data hold time  | T <sub>HD;DAT</sub>   | 0.0                      | —    | 0.0       | 0.9 | μs    |    |
| 54                        | DSP clock frequency <ul style="list-style-type: none"> <li>• Filters bypassed</li> <li>• Very Narrow filters enabled</li> <li>• Narrow filters enabled</li> <li>• Wide filters enabled</li> </ul>   | F <sub>OSC</sub>      | 10.6                     | —    | 28.5      | —   | MHz   |    |
|                           |   |                       | 10.6                     | —    | 28.5      | —   | MHz   |    |
|                           |   |                       | 11.8                     | —    | 39.7      | —   | MHz   |    |
|                           |   |                       | 13.1                     | —    | 61.0      | —   | MHz   |    |
| 55                        | SCL low to data out valid   | T <sub>VD;DAT</sub>   | —                        | 3.4  | —         | 0.9 | μs    |    |
| 56                        | Stop condition setup time   | T <sub>SU;STO</sub>   | 4.0                      | —    | 0.6       | —   | μs    |    |
| 57                        | $\overline{\text{HREQ}}$ in deassertion to last SCL edge ( $\overline{\text{HREQ}}$ in set-up time)   | t <sub>SU;RQI</sub>   | 0.0                      | —    | 0.0       | —   | ns    |    |
| 58                        | First SCL sampling edge to $\overline{\text{HREQ}}$ output deassertion <sup>2</sup> <ul style="list-style-type: none"> <li>• Filters bypassed</li> <li>• Very Narrow filters enabled</li> <li>• Narrow filters enabled</li> <li>• Wide filters enabled</li> </ul> | T <sub>NG;RQO</sub>   | 4 × T <sub>C</sub> + 30  | —    | 50.0      | —   | 50.0  | ns |
|                           |   |                       | 4 × T <sub>C</sub> + 50  | —    | 70.0      | —   | 70.0  | ns |
|                           |   |                       | 4 × T <sub>C</sub> + 130 | —    | 250.0     | —   | 150.0 | ns |
|                           |   |                       | 4 × T <sub>C</sub> + 230 | —    | 150.0     | —   | 250.0 | ns |
| 59                        | Last SCL edge to $\overline{\text{HREQ}}$ output not deasserted <sup>2</sup> <ul style="list-style-type: none"> <li>• Filters bypassed</li> <li>• Very Narrow filters enabled</li> <li>• Narrow filters enabled</li> <li>• Wide filters enabled</li> </ul>        | T <sub>AS;RQO</sub>   | 2 × T <sub>C</sub> + 30  | 40   | —         | 40  | —     | ns |
|                           |   |                       | 2 × T <sub>C</sub> + 40  | 50   | —         | 50  | —     | ns |
|                           |   |                       | 2 × T <sub>C</sub> + 80  | 90   | —         | 90  | —     | ns |
|                           |   |                       | 2 × T <sub>C</sub> + 130 | 140  | —         | 140 | —     | ns |

**Table 10. SHI I<sup>2</sup>C Protocol Timing (Continued)**

| Standard I <sup>2</sup> C |  |                       |          |     |           |     |      |
|---------------------------|--|-----------------------|----------|-----|-----------|-----|------|
| No.                       | Characteristics <sup>1,2,3,4,5</sup>   | Symbol/<br>Expression | Standard |     | Fast-Mode |     | Unit |
|                           |  |                       | Min      | Max | Min       | Max |      |
| 60                        | $\overline{\text{HREQ}}$ in assertion to first SCL edge<br>• Filters bypassed<br>• Very Narrow filters enabled<br>• Narrow filters enabled<br>• Wide filters enabled | $T_{\text{AS;RQI}}$   | 4327     | —   | 927       | —   | ns   |
|                           |  |                       | 4317     | —   | 917       | —   | ns   |
|                           |  |                       | 4282     | —   | 877       | —   | ns   |
|                           |  |                       | 4227     | —   | 827       | —   | ns   |
| 61                        | First SCL edge to $\overline{\text{HREQ}}$ is not asserted ( $\overline{\text{HREQ}}$ in hold time.)   | $t_{\text{HO;RQI}}$   | 0.0      | —   | 0.0       | —   | ns   |

**Note:**

1.  $V_{\text{CORE\_VDD}} = 1.00 \pm 0.05 \text{ V}$ ;  $T_J = -40^\circ \text{ C to } 100^\circ \text{ C}$ ,  $C_L = 50 \text{ pF}$
2. Pull-up resistor:  $R_P (\text{min}) = 1.5 \text{ k}\Omega$
3. Capacitive load:  $C_b (\text{max}) = 50 \text{ pF}$
5. All times assume noise free inputs
5. All times assume internal clock frequency of 200 MHz
6. SHI\_1 specs match those of SHI
7. The numbers listed are based on the module/pad design and its characteristics during output. The module is compliant with I<sup>2</sup>C standard, so the module should receive I<sup>2</sup>C bus compliant signal without any issue.

### 1.2.3 Programming the SHI I<sup>2</sup>C Serial Clock

The programmed serial clock cycle,  $T_{\text{I}^2\text{CCP}}$ , is specified by the value of the HDM[7:0] and HRS bits of the HCKR (SHI clock control register).

The expression for  $T_{\text{I}^2\text{CCP}}$  is

$$T_{\text{I}^2\text{CCP}} = [T_C \times 2 \times (\text{HDM}[7:0] + 1) \times (7 \times (1 - \text{HRS}) + 1)] \quad \text{Eqn. 1}$$

where

- HRS is the prescaler rate select bit. When HRS is cleared, the fixed divide-by-eight prescaler is operational. When HRS is set, the prescaler is bypassed.
- HDM[7:0] are the divider modulus select bits. A divide ratio from 1 to 256 (HDM[7:0] = \$00 to \$FF) may be selected.

In I<sup>2</sup>C mode, the user may select a value for the programmed serial clock cycle from

$$6 \times T_C \quad (\text{if HDM}[7:0] = \$02 \text{ and HRS} = 1) \quad \text{Eqn. 2}$$

to

$$4096 \times T_C \quad (\text{if HDM}[7:0] = \$FF \text{ and HRS} = 0) \quad \text{Eqn. 3}$$

The programmed serial clock cycle ( $T_{\text{I}^2\text{CCP}}$ ) should be chosen in order to achieve the desired SCL serial clock cycle ( $T_{\text{SCL}}$ ), as shown in next.

$$T_{\text{I}^2\text{CCP}} + 3 \times T_C + 45\text{ns} + T_R \quad (\text{Nominal, SCL Serial Clock Cycle (TSCL) generated as master}) \quad \text{Eqn. 4}$$

Figure 16 shows the I<sup>2</sup>C timing diagram.

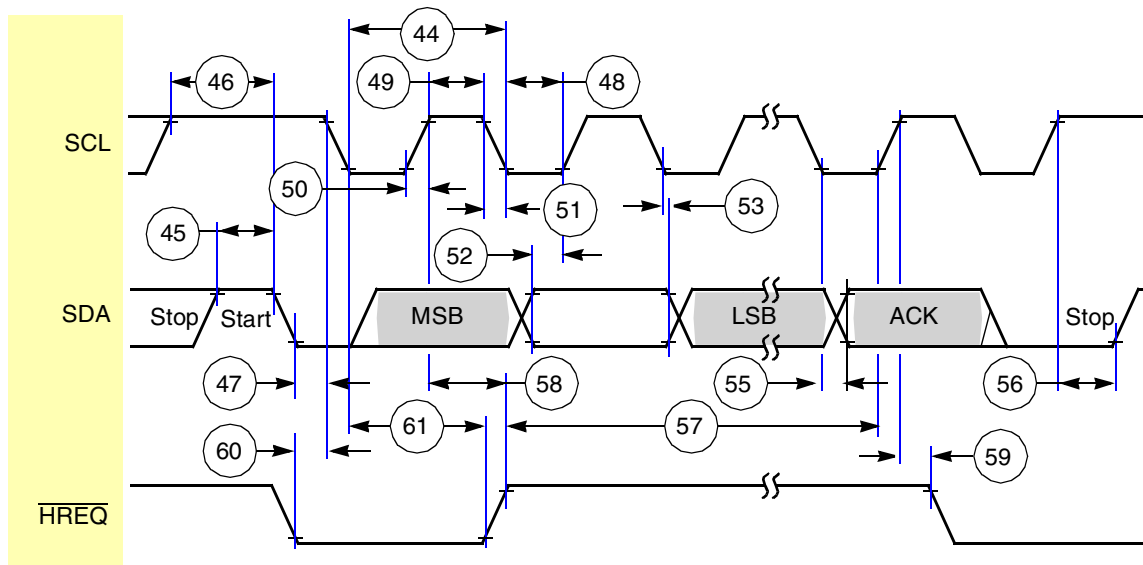


Figure 16. I<sup>2</sup>C Timing

## 1.2.4 Enhanced Serial Audio Interface Timing

Table 11 lists the enhanced serial audio interface timing.

Table 11. Enhanced Serial Audio Interface Timing

| No. | Characteristics <sup>1, 2, 3</sup>                                | Symbol      | Expression <sup>3</sup>          | Min          | Max         | Condition <sup>4</sup> | Unit |
|-----|---|-------------|----------------------------------|--------------|-------------|------------------------|------|
| 62  | Clock cycle <sup>5</sup>  | $t_{SSICC}$ | $4 \times T_C$<br>$4 \times T_C$ | 20.0<br>20.0 | —<br>—      | i ck<br>i ck           | ns   |
| 63  | Clock high period<br>• For internal clock<br>• For external clock | —<br>—      | $2 \times T_C$<br>$2 \times T_C$ | 10<br>10     | —<br>—      | —<br>—                 | ns   |
| 64  | Clock low period<br>• For internal clock<br>• For external clock  | —<br>—      | $2 \times T_C$<br>$2 \times T_C$ | 10<br>10     | —<br>—      | —<br>—                 | ns   |
| 65  | SCKR rising edge to FSR out (bl) high                             | —           | —                                | —<br>—       | 17.0<br>7.0 | x ck<br>i ck a         | ns   |
| 66  | SCKR rising edge to FSR out (bl) low                              | —           | —                                | —<br>—       | 17.0<br>7.0 | x ck<br>i ck a         | ns   |
| 67  | SCKR rising edge to FSR out (wr) high <sup>6</sup>                | —           | —                                | —<br>—       | 19.0<br>9.0 | x ck<br>i ck a         | ns   |
| 68  | SCKR rising edge to FSR out (wr) low <sup>6</sup>                 | —           | —                                | —<br>—       | 19.0<br>9.0 | x ck<br>i ck a         | ns   |
| 69  | SCKR rising edge to FSR out (wl) high                             | —           | —                                | —<br>—       | 16.0<br>6.0 | x ck<br>i ck a         | ns   |
| 70  | SCKR rising edge to FSR out (wl) low                              | —           | —                                | —<br>—       | 17.0<br>7.0 | x ck<br>i ck a         | ns   |

**Table 11. Enhanced Serial Audio Interface Timing (Continued)**

| No. | Characteristics <sup>1, 2, 3</sup>                                       | Symbol | Expression <sup>3</sup> | Min          | Max          | Condition <sup>4</sup> | Unit |
|-----|--|--------|-------------------------|--------------|--------------|------------------------|------|
| 71  | Data in setup time before SCKR (SCK in synchronous mode) falling edge    | —      | —                       | 12.0<br>19.0 | —<br>—       | x ck<br>i ck           | ns   |
| 72  | Data in hold time after SCKR falling edge                                | —      | —                       | 3.5<br>9.0   | —<br>—       | x ck<br>i ck           | ns   |
| 73  | FSR input (bl, wr) high before SCKR falling edge <sup>6</sup>            | —      | —                       | 2.0<br>12.0  | —<br>—       | x ck<br>i ck a         | ns   |
| 74  | FSR input (wl) high before SCKR falling edge                             | —      | —                       | 2.0<br>12.0  | —<br>—       | x ck<br>i ck a         | ns   |
| 75  | FSR input hold time after SCKR falling edge                              | —      | —                       | 2.5<br>8.5   | —<br>—       | x ck<br>i ck a         | ns   |
| 76  | Flags input setup before SCKR falling edge                               | —      | —                       | 0.0<br>19.0  | —<br>—       | x ck<br>i ck s         | ns   |
| 77  | Flags input hold time after SCKR falling edge                            | —      | —                       | 6.0<br>0.0   | —<br>—       | x ck<br>i ck s         | ns   |
| 78  | SCKT rising edge to FST out (bl) high                                    | —      | —                       | —<br>—       | 18.0<br>8.0  | x ck<br>i ck           | ns   |
| 79  | SCKT rising edge to FST out (bl) low                                     | —      | —                       | —<br>—       | 20.0<br>10.0 | x ck<br>i ck           | ns   |
| 80  | SCKT rising edge to FST out (wr) high <sup>6</sup>                       | —      | —                       | —<br>—       | 20.0<br>10.0 | x ck<br>i ck           | ns   |
| 81  | SCKT rising edge to FST out (wr) low <sup>6</sup>                        | —      | —                       | —<br>—       | 22.0<br>12.0 | x ck<br>i ck           | ns   |
| 82  | SCKT rising edge to FST out (wl) high                                    | —      | —                       | —<br>—       | 15.0<br>9.0  | x ck<br>i ck           | ns   |
| 83  | SCKT rising edge to FST out (wl) low                                     | —      | —                       | —<br>—       | 15.0<br>10.0 | x ck<br>i ck           | ns   |
| 84  | SCKT rising edge to data out enable from high impedance                  | —      | —                       | —<br>—       | 22.0<br>17.0 | x ck<br>i ck           | ns   |
| 85  | SCKT rising edge to transmitter #0 drive enable assertion                | —      | —                       | —<br>—       | 17.0<br>11.0 | x ck<br>i ck           | ns   |
| 86  | SCKT rising edge to data out valid                                       | —      | —                       | —<br>—       | 25.0<br>13.0 | x ck<br>i ck           | ns   |
| 87  | SCKT rising edge to data out high impedance <sup>7</sup>                 | —      | —                       | —<br>—       | 25.0<br>16.0 | x ck<br>i ck           | ns   |
| 88  | SCKT rising edge to transmitter #0 drive enable deassertion <sup>7</sup> | —      | —                       | —<br>—       | 14.0<br>9.0  | x ck<br>i ck           | ns   |
| 89  | FST input (bl, wr) setup time before SCKT falling edge <sup>6</sup>      | —      | —                       | 2.0<br>18.0  | —<br>—       | x ck<br>i ck           | ns   |
| 90  | FST input (wl) setup time before SCKT falling edge                       | —      | —                       | 2.0<br>18.0  | —<br>—       | x ck<br>i ck           | ns   |
| 91  | FST input hold time after SCKT falling edge                              | —      | —                       | 4.0<br>5.0   | —<br>—       | x ck<br>i ck           | ns   |



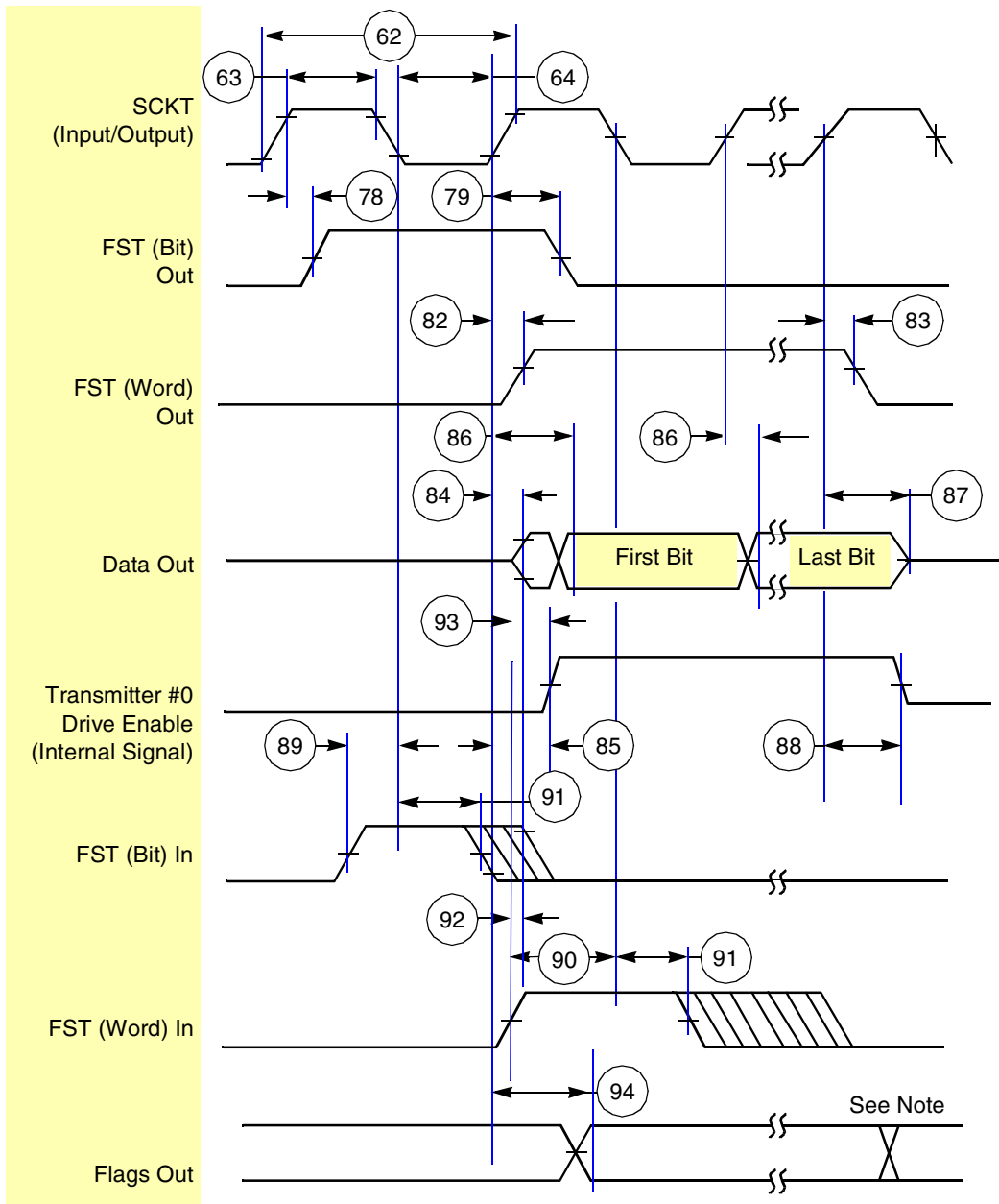
**Table 11. Enhanced Serial Audio Interface Timing (Continued)**

| No. | Characteristics <sup>1, 2, 3</sup>                      | Symbol | Expression <sup>3</sup> | Min | Max         | Condition <sup>4</sup> | Unit |
|-----|---|--------|-------------------------|-----|-------------|------------------------|------|
| 92  | FST input (wl) to data out enable from high impedance   | —      | —                       | —   | 21.0        | —                      | ns   |
| 93  | FST input (wl) to transmitter #0 drive enable assertion | —      | —                       | —   | 14.0        | —                      | ns   |
| 94  | Flag output valid after SCKT rising edge                | —      | —                       | —   | 14.0<br>9.0 | x ck<br>i ck           | ns   |
| 95  | HCKR/HCKT clock cycle                                   | —      | $2 \times T_C$          | 10  | —           | —                      | ns   |
| 96  | HCKT input rising edge to SCKT output                   | —      | —                       | —   | 18.0        | —                      | ns   |
| 97  | HCKR input rising edge to SCKR output                   | —      | —                       | —   | 18.0        | —                      | ns   |

**Note:**

- 0.95 V < V<sub>VDD\_CORE</sub> < 1.05 V and T<sub>j</sub> < 100° C, C<sub>L</sub> = 50 pF
- i ck = internal clock  
x ck = external clock  
i ck a = internal clock, asynchronous mode  
(asynchronous implies that SCKT and SCKR are two different clocks)  
i ck s = internal clock, synchronous mode  
(synchronous implies that SCKT and SCKR are the same clock)
- bl = bit length  
wl = word length  
wr = word length relative
- SCKT(SCKT pin) = transmit clock  
SCKR(SCKR pin) = receive clock  
FST(FST pin) = transmit frame sync  
FSR(FSR pin) = receive frame sync  
HCKT(HCKT pin) = transmit high frequency clock  
HCKR(HCKR pin) = receive high frequency clock
- For the internal clock, the external clock cycle is defined by T<sub>c</sub> and the ESAI control register.
- The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.
- Periodically sampled and not 100% tested.
- ESAI\_1, ESAI\_2, ESAI\_3 specs match those of ESAI.

Figure 17 shows the ESAI transmitter timing diagram.



**Note:** In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period.

Figure 17. ESAI Transmitter Timing

Figure 18 shows the ESAI receiver timing diagram.

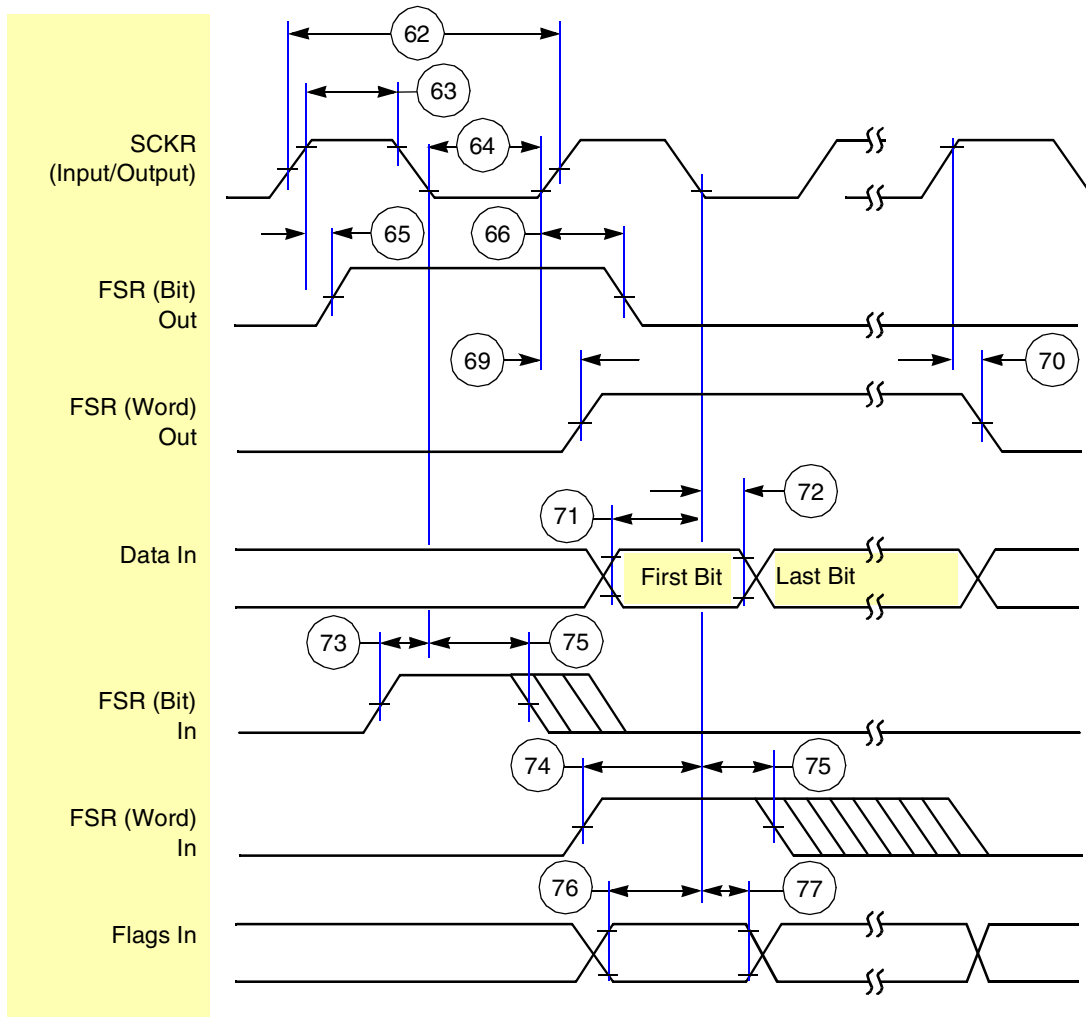


Figure 18. ESAI Receiver Timing

Figure 19 shows the ESAI HCKT timing diagram.

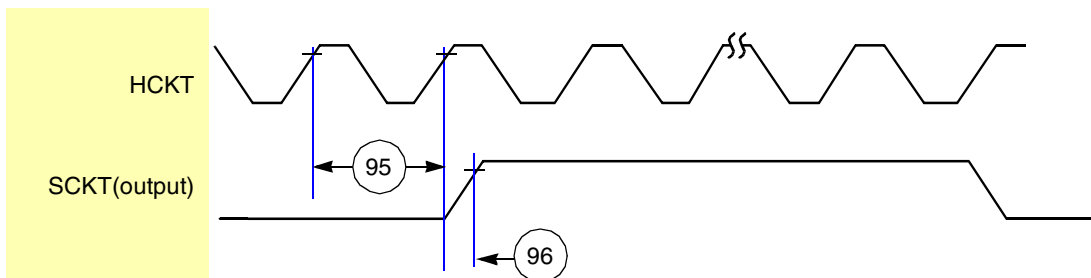


Figure 19. ESAI HCKT Timing

Figure 20 shows the ESAI HCKR timing diagram.

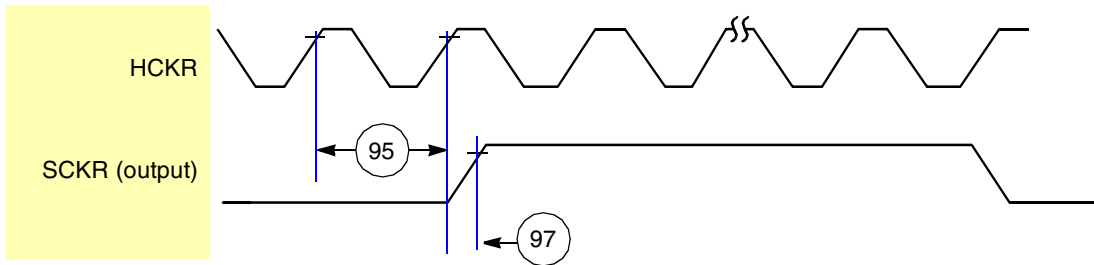


Figure 20. ESAI HCKR Timing

## 1.2.5 GPIO Timing

Table 12 lists the GPIO timing.

Table 12. GPIO Timing

| No. | Characteristics <sup>1</sup>                                      | Expression    | Min | Max  | Unit |
|-----|---|---------------|-----|------|------|
| 100 | Fsys edge to GPIO out valid (GPIO out delay time) <sup>2</sup>    | —             | —   | 7    | ns   |
| 101 | Fsys edge to GPIO out not valid (GPIO out hold time) <sup>2</sup> | —             | —   | 7    | ns   |
| 102 | Fsys In valid to EXTAL edge (GPIO in set-up time) <sup>2</sup>    | —             | 2   | —    | ns   |
| 103 | Fsys edge to GPIO in not valid (GPIO in hold time) <sup>2</sup>   | —             | 0   | —    | ns   |
| 104 | Minimum GPIO pulse high width                                     | $2 \times TC$ | 10  | —    | ns   |
| 105 | Minimum GPIO pulse low width                                      | $2 \times TC$ | 10  | —    | ns   |
| 106 | GPIO out rise time  | —             | —   | 13.0 | ns   |
| 107 | GPIO out fall time  | —             | —   | 13.0 | ns   |

**Note:**

1.  $0.95\text{ V} < V_{\text{VDD\_CORE}} < 1.05\text{ V}$  and  $T_j < 100^\circ\text{ C}$ ,  $C_L = 50\text{ pF}$
2. Simulation numbers-subject to change.

Figure 21 shows the GPIO timing diagram.

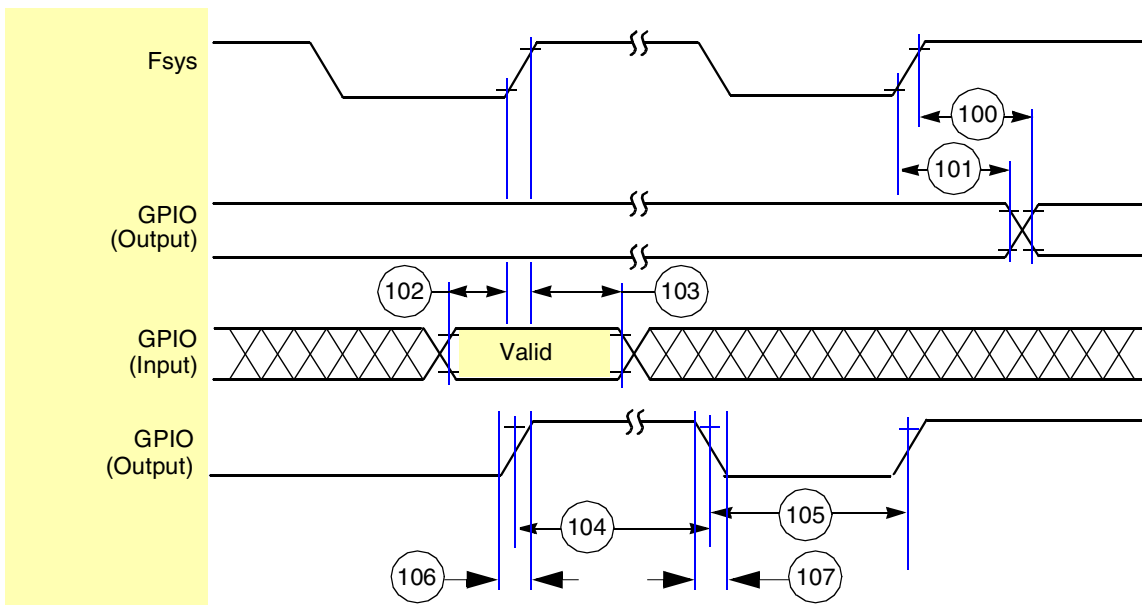


Figure 21. GPIO Timing

## 1.2.6 JTAG Timing

Table 13 lists the JTAG timing.

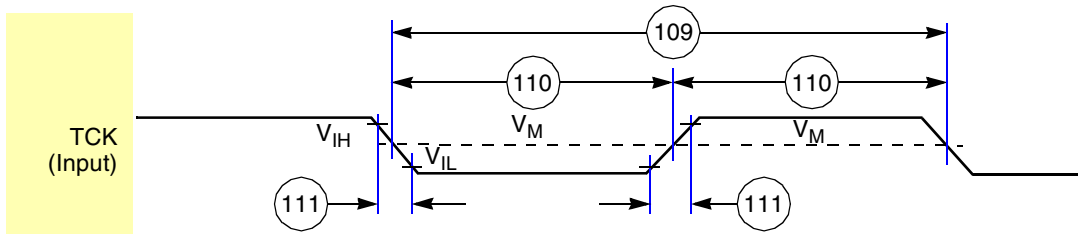
Table 13. JTAG Timing

| No. | Characteristics   | All Frequencies |      | Unit |
|-----|---|-----------------|------|------|
|     |   | Min             | Max  |      |
| 108 | TCK frequency of operation ( $1/(T_C \times 3)$ ; maximum 10 MHz) | —               | 10.0 | MHz  |
| 109 | TCK cycle time in Crystal mode                                    | 100.0           | —    | ns   |
| 110 | TCK clock pulse width measured at 1.65 V                          | 50.0            | —    | ns   |
| 111 | TCK rise and fall times   | —               | 3.0  | ns   |
| 112 | Boundary scan input data setup time                               | 15.0            | —    | ns   |
| 113 | Boundary scan input data hold time                                | 24.0            | —    | ns   |
| 114 | TCK low to output data valid                                      | —               | 40.0 | ns   |
| 115 | TCK low to output high impedance                                  | —               | 40.0 | ns   |
| 116 | TMS, TDI data setup time  | 5.0             | —    | ns   |
| 117 | TMS, TDI data hold time   | 25.0            | —    | ns   |
| 118 | TCK low to TDO data valid   | —               | 44.0 | ns   |
| 119 | TCK low to TDO high impedance                                     | —               | 44.0 | ns   |

**Note:**

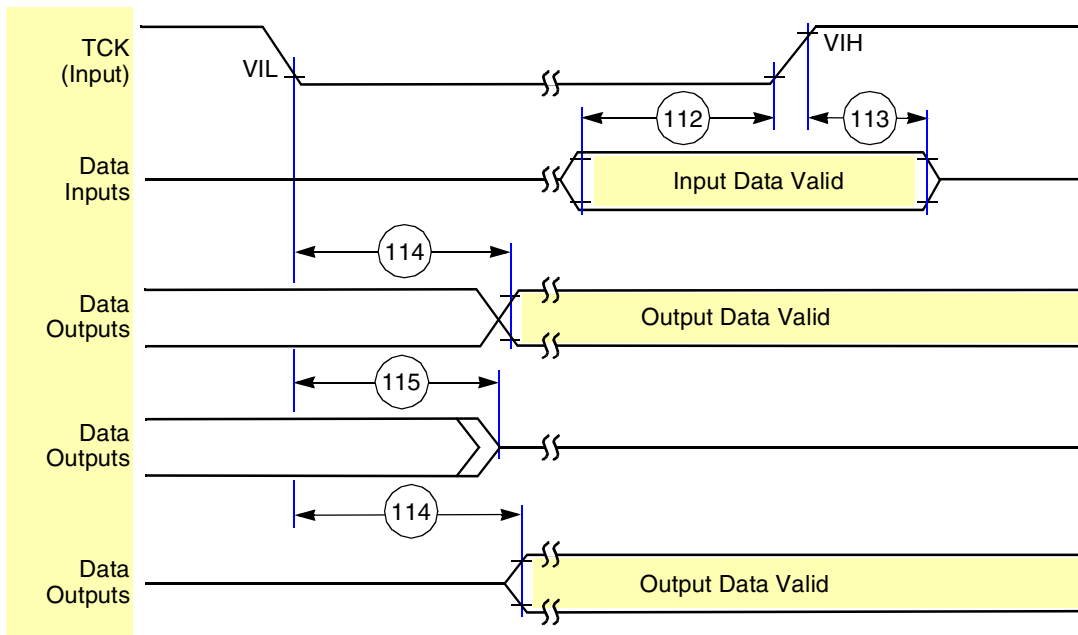
1.  $0.95 \text{ V} < V_{\text{VDD\_CORE}} < 1.05 \text{ V}$  and  $T_j < 100^\circ \text{ C}$ ,  $C_L = 50 \text{ pF}$
2. All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

Figure 22 shows the test clock input timing diagram.



**Figure 22. Test Clock Input Timing Diagram**

Figure 23 shows the debugger port timing diagram.



**Figure 23. Debugger Port Timing Diagram**

Figure 24 shows the test access port timing diagram.

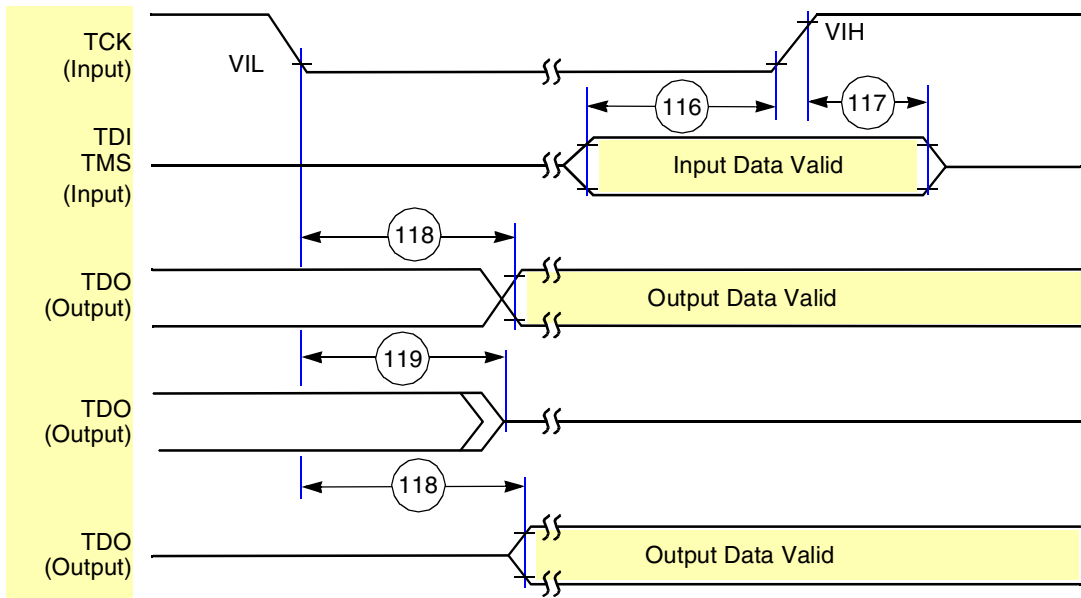


Figure 24. Test Access Port Timing Diagram

## 1.2.7 Watchdog Timer Timing

Table 14 lists the watchdog timer timings.

Table 14. Watchdog Timer Timing

| No. | Characteristics   | Expression     | Min  | Max | Unit |
|-----|---|----------------|------|-----|------|
| 120 | Delay from time-out to fall of $\overline{\text{WDT}}$ , $\overline{\text{WDT}}_1$    | $2 \times T_C$ | 10.0 | —   | ns   |
| 121 | Delay from timer clear to rise of $\overline{\text{WDT}}$ , $\overline{\text{WDT}}_1$ | $2 \times T_c$ | 10.0 | —   | ns   |

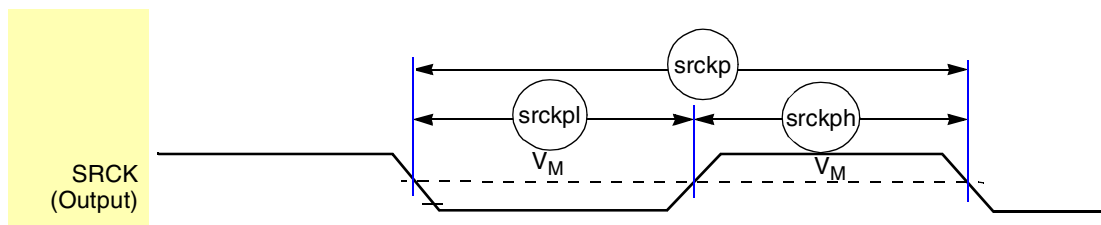
## 1.2.8 S/PDIF Timing

Table 15 lists the S/PDIF timing.

**Table 15. S/PDIF Timing**

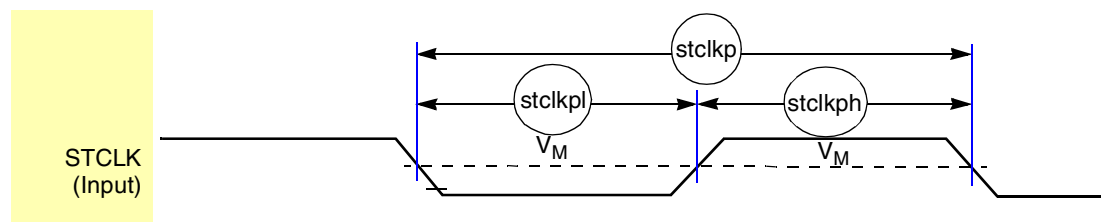
| Characteristics  | Symbol  | All Frequency |      | Unit |
|--|---------|---------------|------|------|
|  |         | Min           | Max  |      |
| SPDIFIN1, SPDIFIN2, SPDIFIN3, SPDIFIN4 Skew: asynchronous inputs, no specs apply | —       | —             | 0.7  | ns   |
| SPDIFOUT1, SPDIFOUT2 output (Load = 50pf)  | —       | —             | 1.5  | ns   |
| • Skew   | —       | —             | 24.2 |      |
| • Transition Rising  | —       | —             | 31.3 |      |
| • Transition Falling   | —       | —             |      |      |
| SPDIFOUT1, SPDIFOUT2 output (Load = 30pf)  | —       | —             | 1.5  | ns   |
| • Skew   | —       | —             | 13.6 |      |
| • Transition Rising  | —       | —             | 18.0 |      |
| • Transition Falling   | —       | —             |      |      |
| SRCK period  | srckp   | 40.0          | —    | ns   |
| SRCK high period   | srckph  | 16.0          | —    | ns   |
| SRCK low period  | srckpl  | 16.0          | —    | ns   |
| STCLK period   | stclkp  | 40.0          | —    | ns   |
| STCLK high period  | stclkph | 16.0          | —    | ns   |
| STCLK low period   | stclkpl | 16.0          | —    | ns   |

Figure 25 shows the SRCK timing diagram.



**Figure 25. SRCK Timing**

Figure 26 shows the STCLK timing diagram.



**Figure 26. STCLK Timing**



## 1.2.9 EMC Timing Specifications—DSP56724

Table 16 lists the EMC timing parameters with EMC PLL enabled.

### NOTE

The DSP56725 device does not have an EMC module.

**Table 16. EMC Timing Parameters (EMC PLL Enabled; LCRR[CLKDIV] = 2)**

| Parameter   | Symbol          | Min            | Max | Unit |
|---|-----------------|----------------|-----|------|
| LCLK cycle time   | $T_{clk}$       | $2 \times T_C$ | —   | ns   |
| LCLK skew to LSYNC_OUT  | $T_{clk\_skew}$ | —              | 160 | ps   |
| Input setup to LSYNC_IN (except $\overline{LGTA}$ /LUPWAIT)           | $T_{in\_s}$     | 3              | —   | ns   |
| Input hold from LSYNC_IN (except $\overline{LGTA}$ /LUPWAIT)          | $T_{in\_h}$     | 2              | —   | ns   |
| $\overline{LGTA}$ valid time  | $T_{gta}$       | 12             | —   | ns   |
| LUPWAIT valid time  | $T_{upwait}$    | 12             | —   | ns   |
| LALE negedge to LAD (address phase) invalid (address latch hold time) | $T_{ale\_h}$    | 3              | —   | ns   |
| LALE valid time   | $T_{ale}$       | 3.8            | —   | ns   |
| Output setup from LSYNC_IN (except LAD[23:0] and LALE)                | $T_{out\_s}$    | 4              | —   | ns   |
| Output hold from LSYNC_IN (except LAD[23:0] and LALE)                 | $T_{out\_h}$    | 2              | —   | ns   |
| LAD[23:0] output setup from LSYNC_IN                                  | $T_{ad\_s}$     | 3.5            | —   | ns   |
| LAD[23:0] output hold from LSYNC_IN                                   | $T_{ad\_h}$     | 1.5            | —   | ns   |
| LSYNC_IN to output high impedance for LAD[23:0]                       | $T_{ad\_z}$     | —              | 4.3 | ns   |

Figure 27 shows the EMC signals diagram, with EMC PLL enabled.

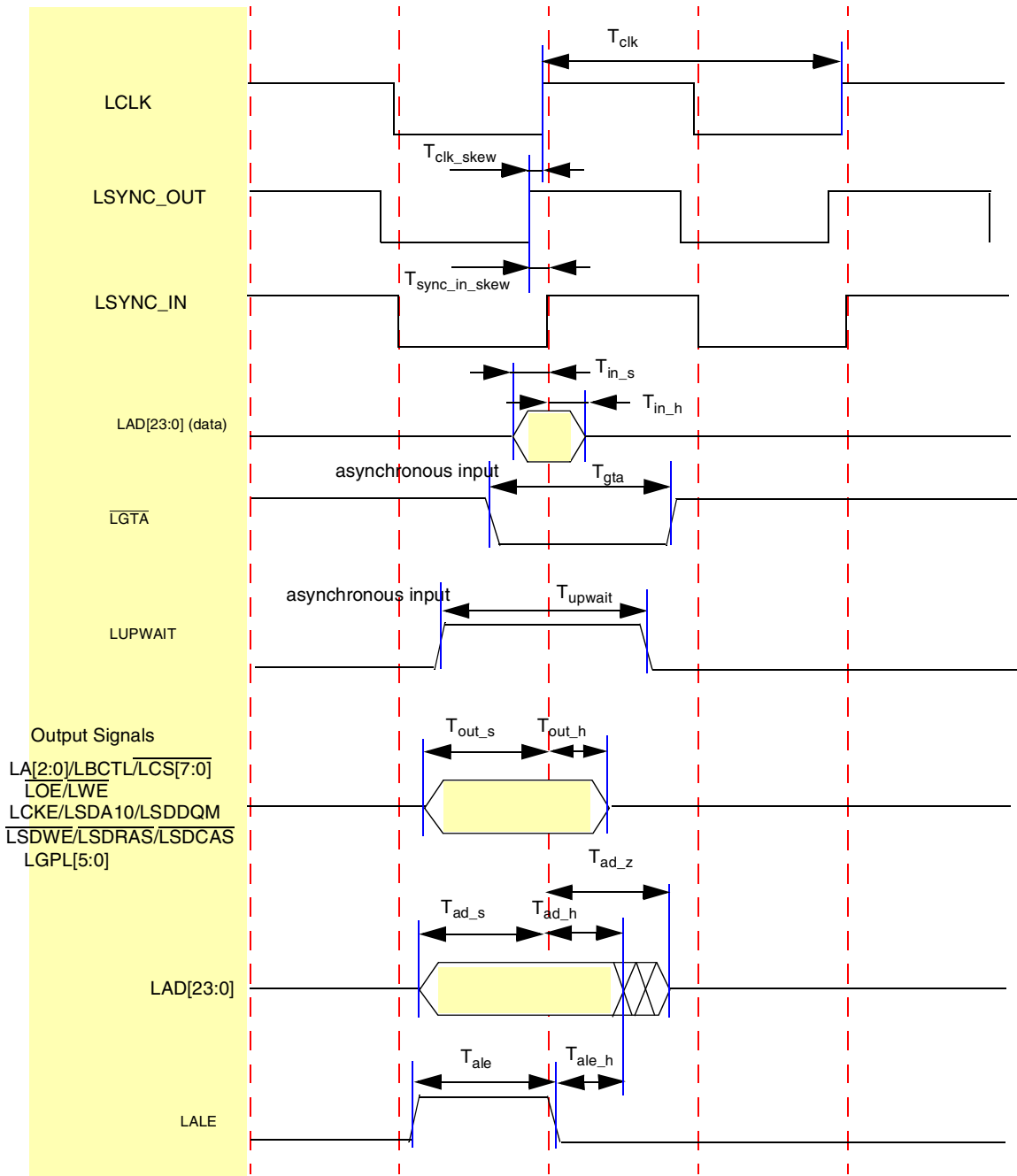


Figure 27. EMC Signals (EMC PLL Enabled; LCRR[CLKDIV] = 2)

Table 17 lists the EMC timing parameters with EMC PLL bypassed.

**Table 17. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 4)**

| Parameter   | Symbol       | Min            | Max | Unit |
|---|--------------|----------------|-----|------|
| LCLK cycle time   | $T_{clk}$    | $4 \times T_C$ | —   | ns   |
| Input setup to LCLK (except $\overline{LGTA}$ /LUPWAIT)               | $T_{in_s}$   | 8              | —   | ns   |
| Input hold from LCLK (except $\overline{LGTA}$ /LUPWAIT) <sup>1</sup> | $T_{in_h}$   | -1             | —   | ns   |
| $\overline{LGTA}$ valid time  | $T_{gta}$    | 22             | —   | ns   |
| LUPWAIT valid time  | $T_{upwait}$ | 22             | —   | ns   |
| LALE negedge to LAD (address phase) invalid (address latch hold time) | $T_{ale_h}$  | 4              | —   | ns   |
| LALE valid time   | $T_{ale}$    | 14             | —   | ns   |
| Output setup from LCLK (except LAD[23:0] and LALE)                    | $T_{out_s}$  | 9              | —   | ns   |
| Output hold from LCLK (except LAD[23:0] and LALE)                     | $T_{out_h}$  | 8              | —   | ns   |
| LAD[23:0] output setup from LCLK                                      | $T_{ad_s}$   | 8              | —   | ns   |
| LAD[23:0] output hold from LCLK                                       | $T_{ad_h}$   | 7              | —   | ns   |
| LCLK to output high impedance for LAD[23:0]                           | $T_{ad_z}$   | —              | 8.1 | ns   |

**Note:** Negative hold time means the signal could be invalid before LCLK rising edge.

Figure 28 shows the EMC signals diagram, with EMC PLL bypassed.

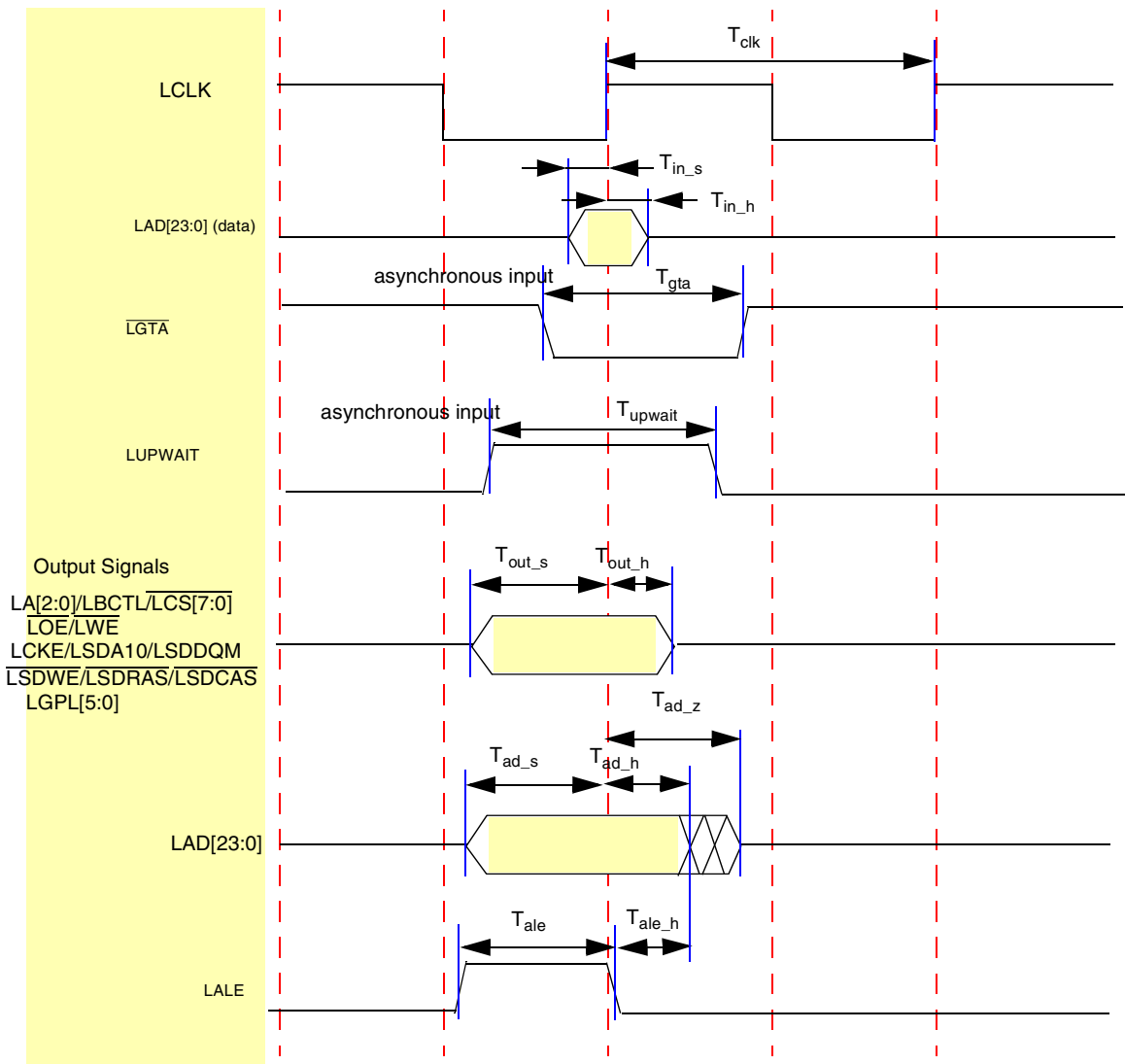


Figure 28. EMC Signals (EMC PLL Bypassed; LRCC[CLKDIV] = 4

Table 18 lists the EMC timing parameters with EMC PLL bypassed.

Table 18. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 8)

| Parameter   | Symbol       | Min            | Max | Unit |
|---|--------------|----------------|-----|------|
| LCLK cycle time   | $T_{clk}$    | $8 \times T_C$ | —   | ns   |
| Input setup to LCLK (except $\overline{LGTA}$ /LUPWAIT)               | $T_{in_s}$   | 8              | —   | ns   |
| Input hold from LCLK (except $\overline{LGTA}$ /LUPWAIT) <sup>1</sup> | $T_{in_h}$   | -1             | —   | ns   |
| $\overline{LGTA}$ valid time  | $T_{gta}$    | 42             | —   | ns   |
| LUPWAIT valid time  | $T_{upwait}$ | 42             | —   | ns   |
| LALE negedge to LAD (address phase) invalid (address latch hold time) | $T_{ale_h}$  | 5              | —   | ns   |
| LALE valid time   | $T_{ale}$    | 34             | —   | ns   |

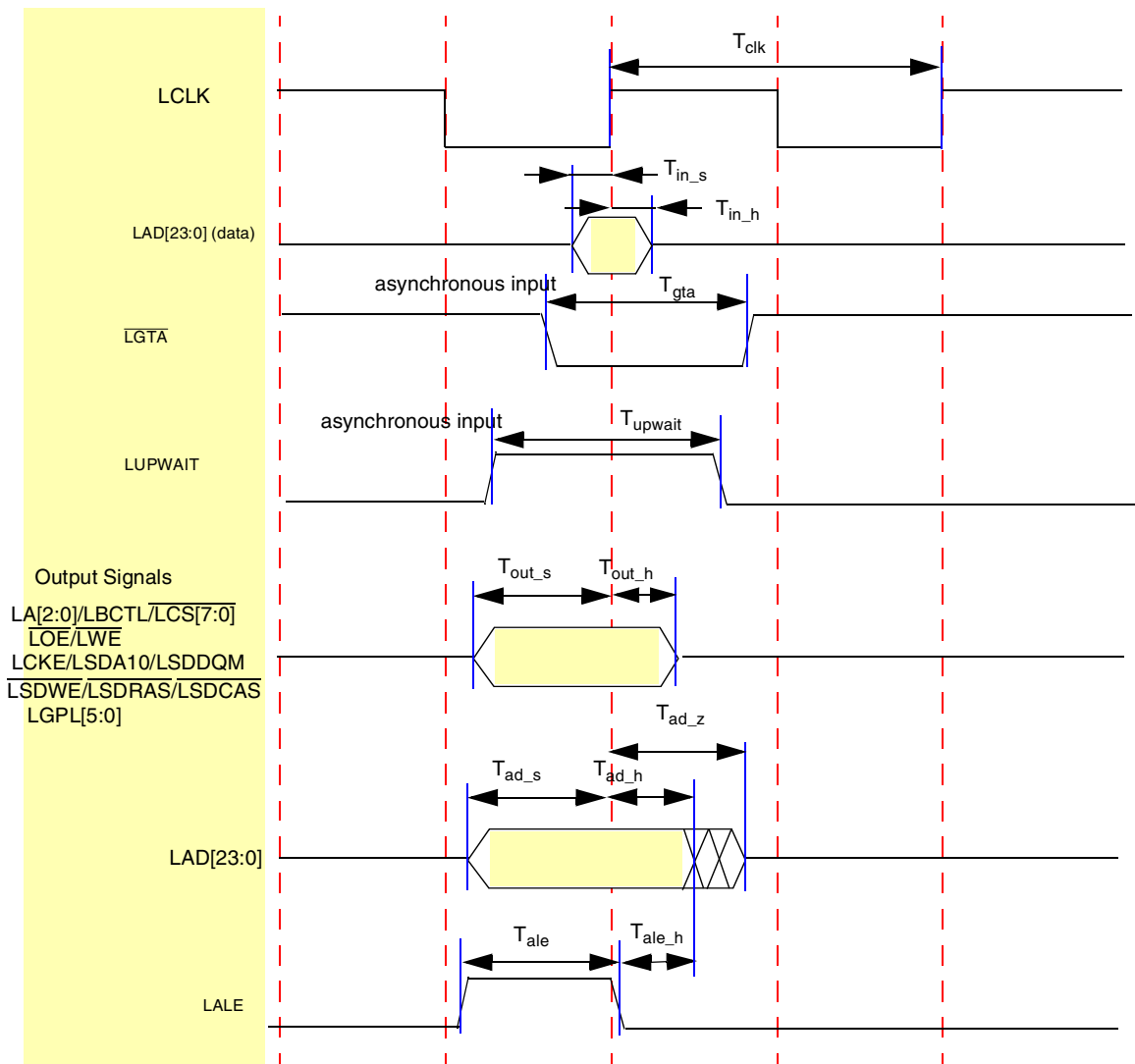
**Table 18. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 8)**

| Parameter  | Symbol       | Min | Max  | Unit |
|--|--------------|-----|------|------|
| Output setup from LCLK (except LAD[23:0] and LALE) | $T_{out\_s}$ | 19  | —    | ns   |
| Output hold from LCLK (except LAD[23:0] and LALE)  | $T_{out\_h}$ | 18  | —    | ns   |
| LAD[23:0] output setup from LCLK                   | $T_{ad\_s}$  | 18  | —    | ns   |
| LAD[23:0] output hold from LCLK                    | $T_{ad\_h}$  | 17  | —    | ns   |
| LCLK to output high impedance for LAD[23:0]        | $T_{ad\_z}$  | —   | 17.1 | ns   |

**Note:**

1. Negative hold time means the signal could be invalid before LCLK raising edge.

Figure 29 shows the EMC signals diagram, with EMC PLL bypassed.



**Figure 29. EMC Signals (EMC PLL Bypassed; LRCC[CLKDIV] = 8)**

## 2 Functional Description and Application Information

Refer to the *Symphony™ DSP56724/DSP56725 Multi-Core Audio Processors Reference Manual (DSP56724RM)* for detailed functional and applications information.

## 3 Ordering Information

Table 19 shows the ordering information for the DSP56724/DSP56725 devices.

**Table 19. Ordering Information**

| Device   | Device Marking | Ambient Temp. | Speed   | Voltage     | LQFP Package  |
|----------|----------------|---------------|---------|-------------|---------------|
| DSP56724 | DSPB56724AG    | 0° C–70° C    | 250 MHz | 1.14–1.26 V | 20 mm × 20 mm |
| DSP56724 | DSPB56724CAG   | –40° C–85° C  | 200 MHz | 0.95–1.05 V | 20 mm × 20 mm |
| DSP56725 | DSPB56725AF    | 0° C–70° C    | 250 MHz | 1.14–1.26 V | 14 mm × 14 mm |
| DSP56725 | DSPB56725CAF   | –40° C–85° C  | 200 MHz | 0.95–1.05 V | 14 mm × 14 mm |

Contact your local Freescale sales representative for ordering information.

## 4 Package Information

This section provides package and pinout information.

Table 20 is a quick reference to the package outline drawings.

**Table 20. Package Outline Drawings**

| Device   | Package              | See   |
|----------|----------------------|---|
| DSP56724 | 144-pin plastic LQFP | See <a href="#">Section 4.2, “144-Pin Package Outline Drawing,”</a> on page 41. |
| DSP56725 | 80-pin plastic LQFP  | See <a href="#">Section 4.3, “80-Pin Package Outline Drawing,”</a> on page 43.  |

## 4.1 Pinout and Package Information

This section provides information about the available package for DSP56724 and DSP56725 devices, including diagrams of the package pinouts. See [Figure 30](#) for the DSP56724 pin assignments and [Figure 31](#) for the DSP56725 pin assignments. For more detailed information about signals, refer to the *Symphony™ DSP56724/DSP56725 Multi-Core Audio Processors Reference Manual* (DSP56724RM).

### 4.1.1 Pinout for DSP56724 144-Pin Plastic LQFP Package

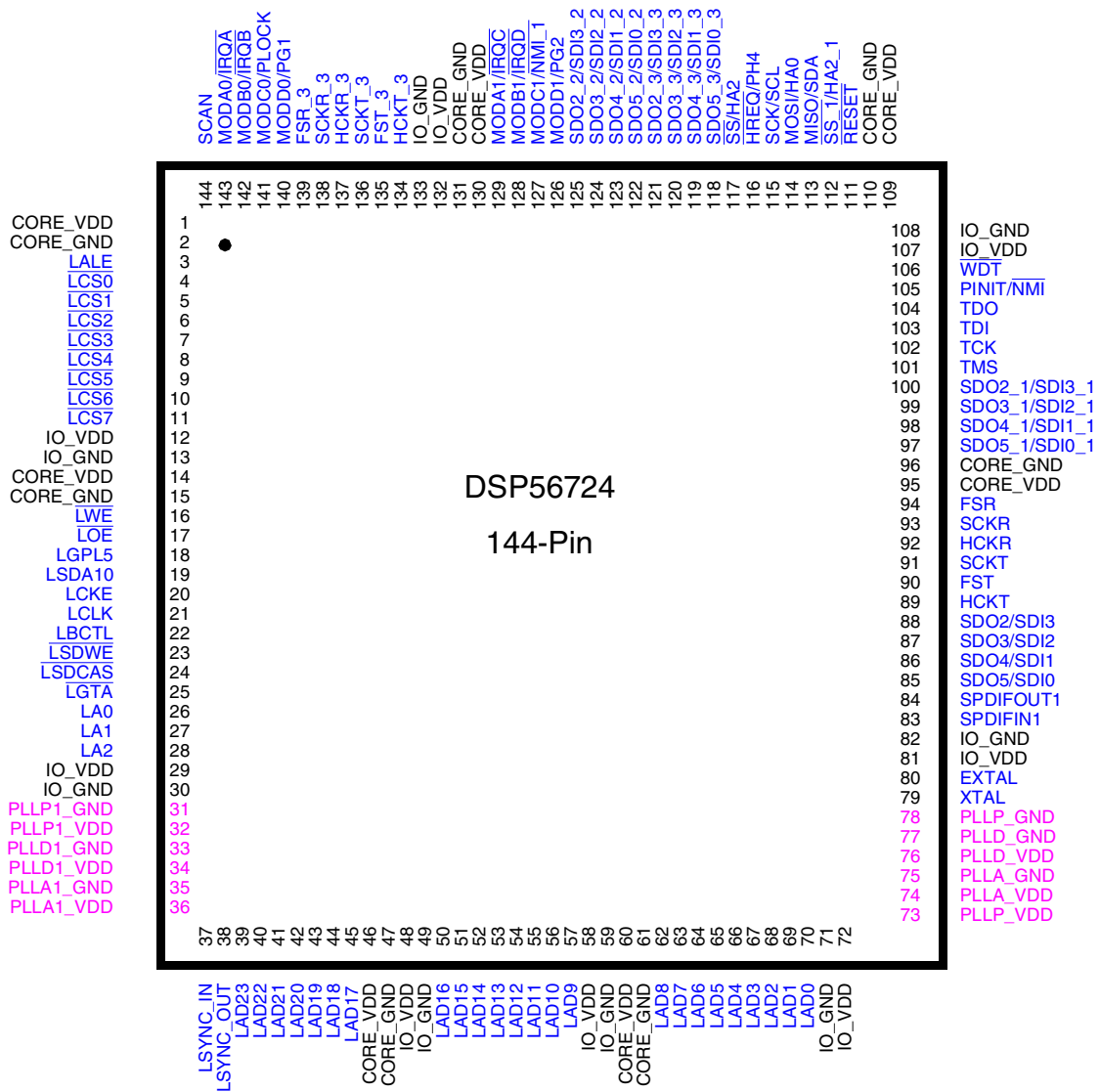


Figure 30. DSP56724 144-Pin Package Pinout

## 4.1.2 Pinout for DSP56725 80-Pin Plastic LQFP Package

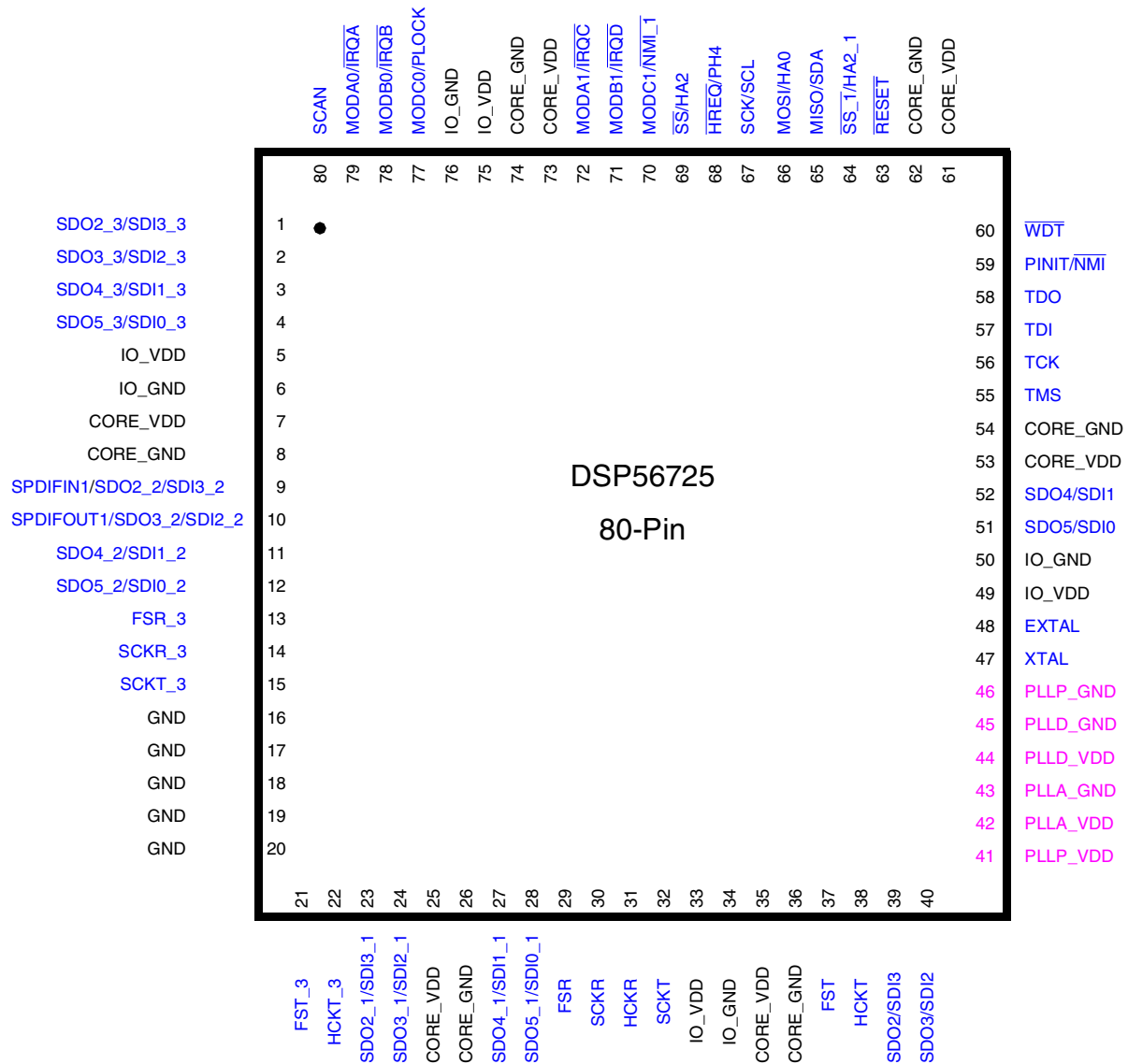


Figure 31. DSP56725 80-Pin Package

## 4.1.3 Pin Multiplexing

Many pins are multiplexed, and depending on the selected configuration, can be one of three possible signals. For more about pin multiplexing, refer to the *Symphony™ DSP56724/DSP56725 Multi-Core Audio Processors Reference Manual* (DSP56724RM).



## 4.2 144-Pin Package Outline Drawing

The 144-pin package outline drawing is shown in [Figure 32](#) and [Figure 33](#).

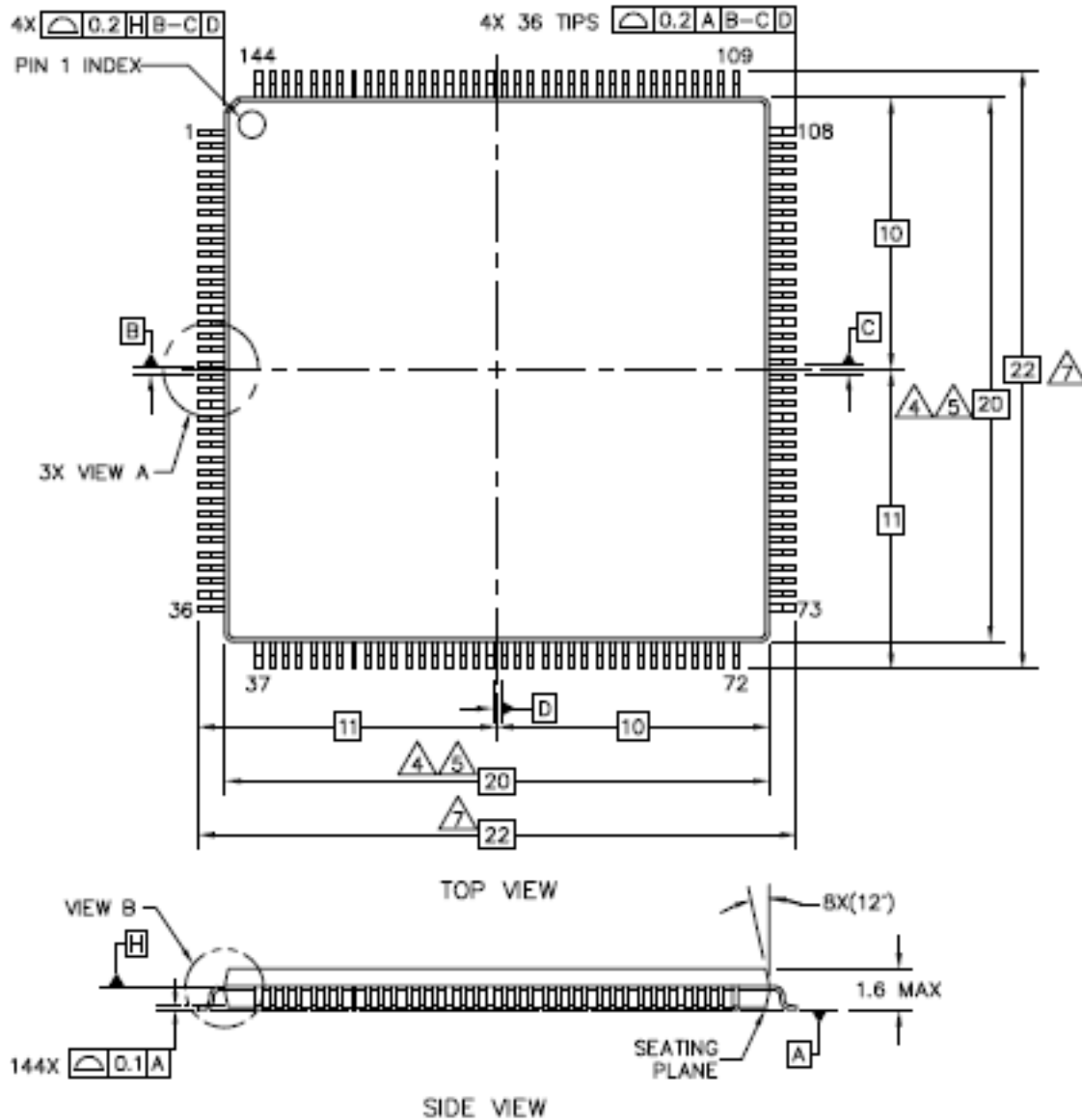


Figure 32. 144-Pin Package Outline Drawing

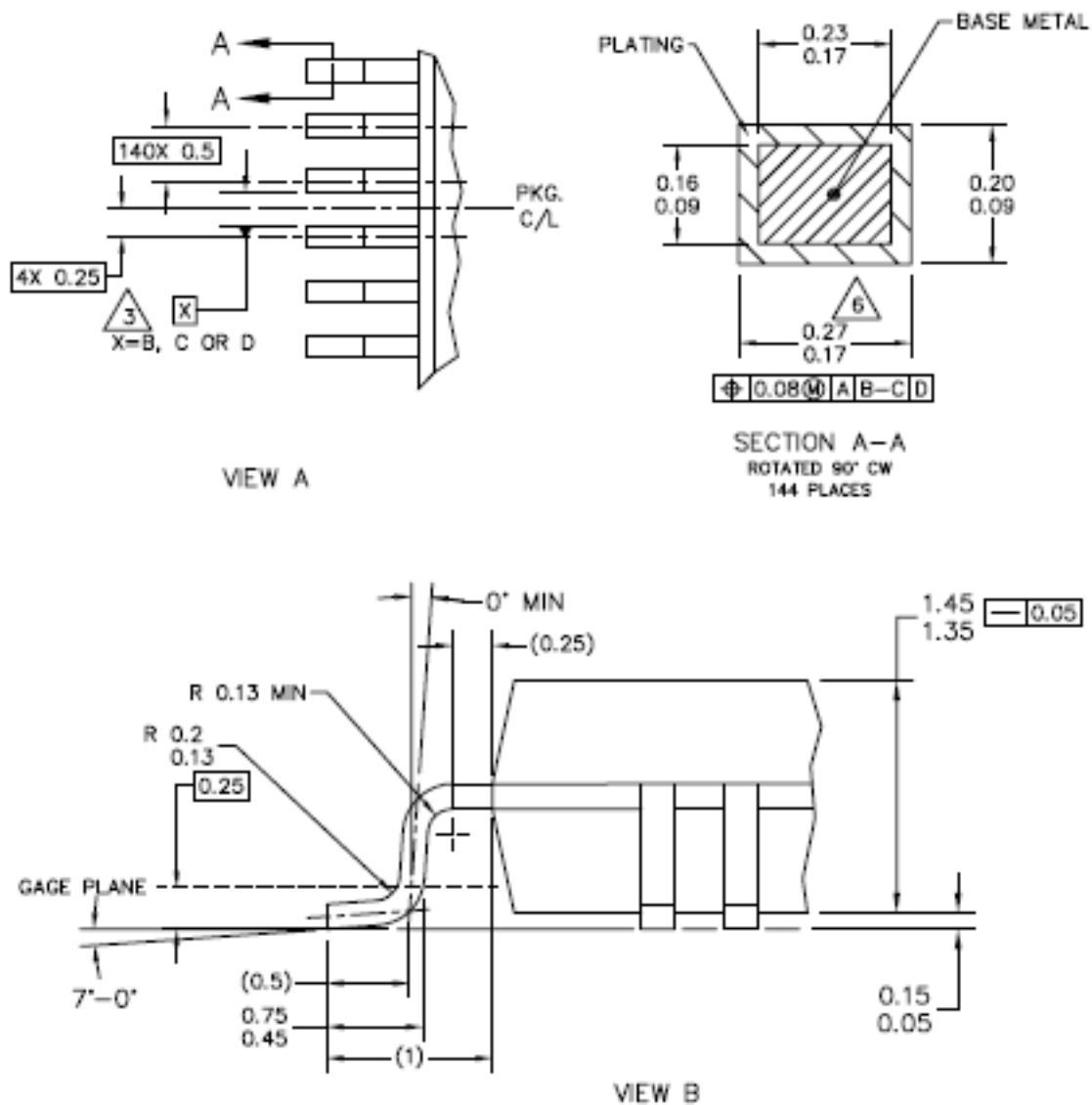


Figure 33. 144-Pin Package Outline Drawing (continued)

**FIGURE NOTES:**

- 1 All dimensions are in millimeters.
- 2 Interpret dimensions and tolerances per ASME Y.14.5M-1994
- 3 Datums B, C and D to be determined at datum plane H.
- 4 The top package body size may be smaller than the bottom package size by a maximum of 0.1 mm.
- 5 These dimensions do not include mold protrusions. The maximum allowable protrusion is 0.25 mm per side. These dimensions are maximum body size dimensions including mold mismatch.
- 6 This dimension does not include dam bar protrusion. Protrusions shall not cause the lead width to exceed 0.35 mm. Minimum space between protrusion and an adjacent lead shall be 0.07 mm.
- 7 These dimensions are determined at the seating plane, datum A.

## 4.3 80-Pin Package Outline Drawing

The 80-pin package outline drawing is shown in Figure 34 and Figure 35.

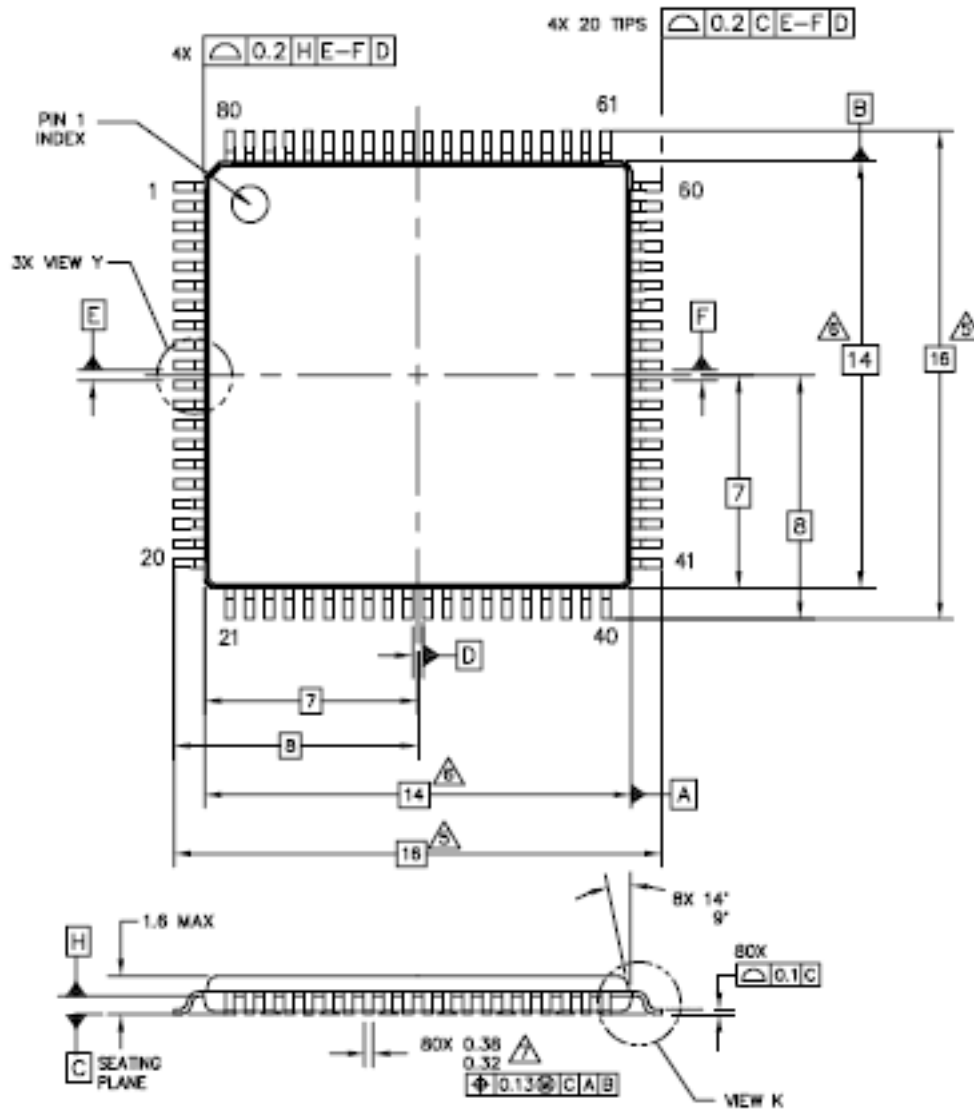


Figure 34. 80-Pin Package Outline Drawing

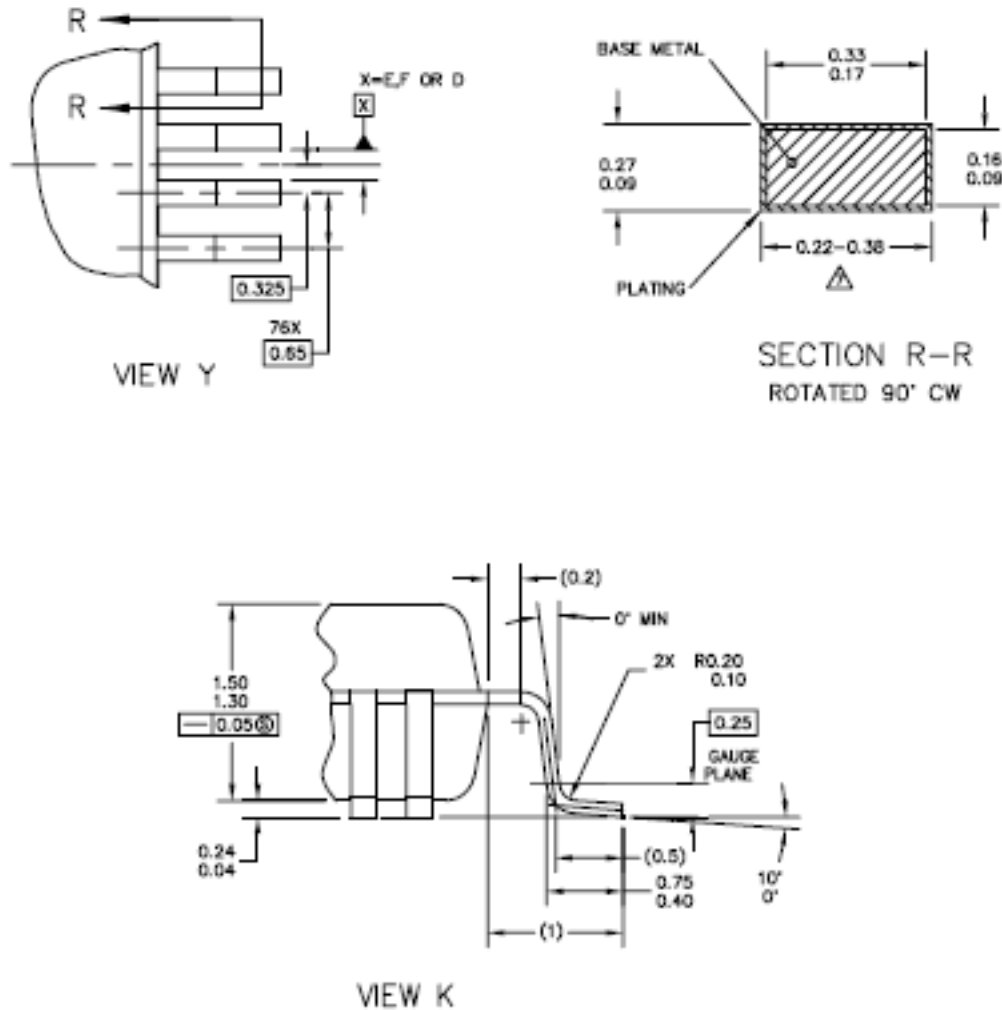


Figure 35. 80-Pin Package Outline Drawing (continued)

**FIGURE NOTES:**

- 1 Dimensioning and tolerancing per ASME Y.14.5M–1994.
- 2 Controlling dimension: millimeter.
- 3 Data plane H is located at the bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
- 4 Datum E, F and to be determined at datum plane H.
- 5 Dimensions to be determined at seating plane C.
- 6 Dimensions do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions include mold mismatch and are determined at datum plane H.
- 7 Dimension does not include dambar protrusion. Dambar protrusion shall not cause the lead width to exceed 0.46 mm. Minimum space between protrusion and adjacent lead or protrusion is 0.07mm.

## 5 Product Documentation

Table 21 lists the documents that provide a complete description of the DSP56724/DSP56725 devices and are required to design properly with the part. Documentation is available from a local Freescale Semiconductor, Inc. (formerly Motorola) distributor, semiconductor sales office, Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

**Table 21. DSP56724 / DSP56725 Documentation**

| Document Name                      | Description   | Order Number |
|------------------------------------|---|--------------|
| DSP56300 Family Manual             | Detailed description of the 56300-family architecture and the 24-bit core processor and instruction set | DSP56300FM   |
| DSP56724/DSP56725 Reference Manual | Detailed description of memory, peripherals, and interfaces   | DSP56724RM   |
| DSP56724 Product Brief             | Brief description of the DSP56724 device  | DSP56724PB   |
| DSP56725 Product Brief             | Brief description of the DSP56725 device  | DSP56725PB   |
| DSP56724/DSP56725 Data Sheet       | Electrical and timing specifications; pin and package descriptions (this document)                      | DSP56724     |

## 6 Revision History

Table 22 summarizes revisions to this document.

**Table 22. Revision History**

| Revision | Date    | Description  |
|----------|---------|--|
| 1        | 12/2008 | <ul style="list-style-type: none"> <li>Modified values and removed rows in Table 4, “DC Electrical Characteristics.”</li> <li>Removed “IO_VDD_25” from Figure 4, “Prevent High Current Conditions by Applying IO_VDD Before Core_VDD.”</li> <li>In Table 7, “Reset, Stop, Mode Select, and Interrupt Timing,” for No. 15, changed 10 to 12, and for No. 16, changed 4 to 7.</li> <li>In Table 9, “Serial Host Interface SPI Protocol Timing,” updated values.</li> <li>In Table 10, “SHI I2C Protocol Timing,” added note 7 and changed Max values for No. 50 to 1000 and 300; in addition, updated the values for note 1.</li> <li>In Table 11, “Enhanced Serial Audio Interface Timing,” for No. 82, changed 19 to 15; for No. 83, changed 20 to 15; for No. 86, changed 18 to 25; for No. 87, changed 21 to 25.</li> <li>Removed Section 1.2.5, “Timer Timing.”</li> <li>In Table 16, “EMC Timing Parameters (EMC PLL Enabled; LCRR[CLKDIV] = 2),” for “LSYNC_IN (except LGTA/LUPWAIT),” changed 2 to 3.</li> <li>In Table 17, “EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 4),” for “LCLK to output high impedance for LAD [23:0],” changed 9 to 8.1.</li> <li>In Table 18, “EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 8),” for LCLK to output high impedance for LAD [23:0],” changed 19 to 17.1</li> <li>In Table 19, “Ordering Information,” added rows for DSPB56724CAG and DSPB56725CAF, and changed “DSPA56724AG” to “DSPB56724AG.”</li> </ul> |
| 0        | 6/2008  | <ul style="list-style-type: none"> <li>Initial public release.</li> </ul>  |



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12/2008

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