TOUCH SCREEN CONTROLLER

FEATURES

- 4-WIRE TOUCH SCREEN INTERFACE
- RATIOMETRIC CONVERSION
- SINGLE SUPPLY: 2.2V to 3.6V
- UP TO 125kHz CONVERSION RATE
- SERIAL INTERFACE
- PROGRAMMABLE 8-/12-BIT RESOLUTION
- 2 AUXILIARY ANALOG INPUT
- AUTO POWER-DOWN
- LOW POWER CONSUMPTION (240uA)

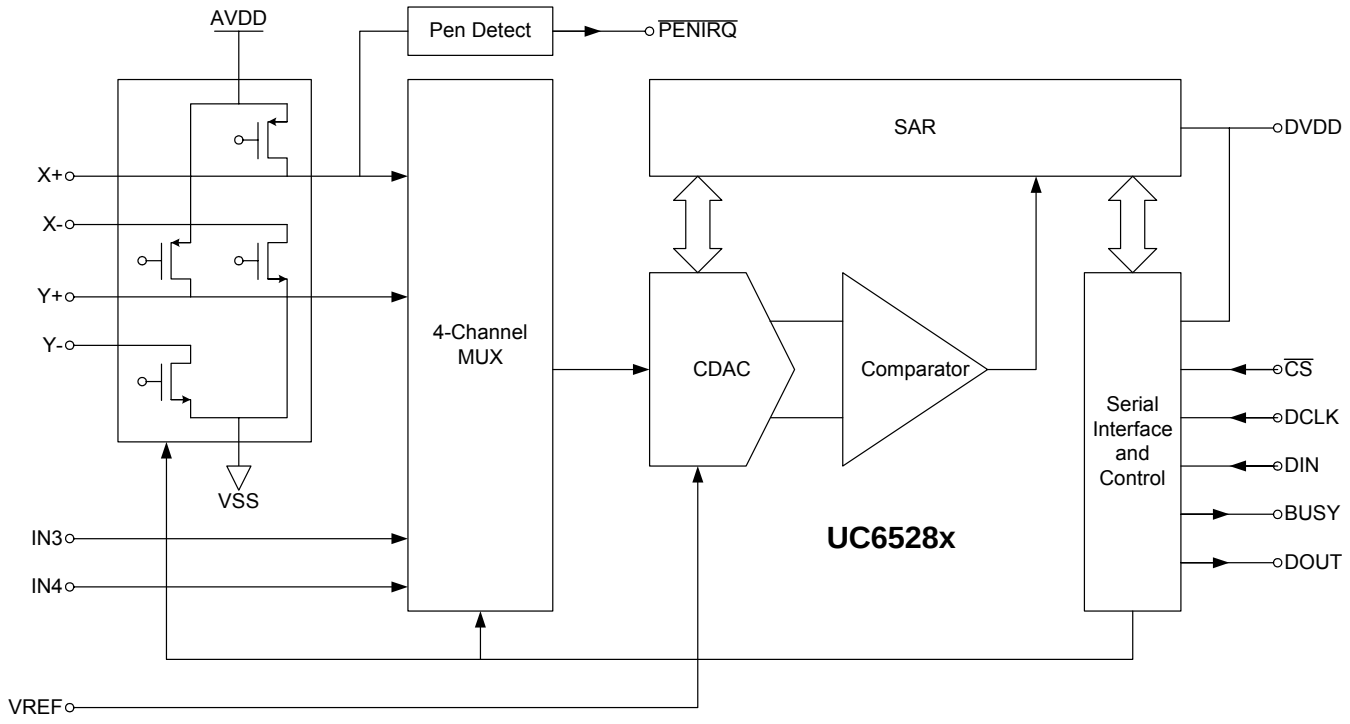
APPLICATIONS

- PERSONAL DITIAL ASSISTANTS
- PORTABLE INSTRUMENTS
- POINT-OF-SALES TERMINALS
- PAGERS
- TOUCH SCREEN MONITORS
- CELLULAR PHONES

DESCRIPTION

The UC6528x is a 12-bit sampling Analog-to-Digital Converter (ADC) with a synchronous serial interface and low on-resistance switches for driving touch screens. Typical power dissipation is 650uW at 125kHz throughput rate and a +2.7V supply. The reference voltage (VREF) can be varied between 1V and +AVDD, providing a corresponding input voltage range of 0V to VREF. The device includes a shutdown mode which reduces typical power dissipation to under 0.3µW. All analog inputs are fully ESD protected, eliminating the need for external devices.

Low power, high speed, and onboard switches make the UC6528x ideal for battery-operated systems such as personal digital assistants (PDAs) with resistive touch screens, pagers, cellular phones, and other portable equipment. The UC6528x is available in QFN-16 package and is specified over the -40°C to +85°C temperature range.



ABSOLUTE MAXIMUM RATINGS(1)

AVDD and DVDD to VSS	-0.3V to +4.0V
Analog Inputs to VSS	-0.3V to +AVDD +0.3V
Digital Inputs to VSS	-0.3V to +DVDD +0.3V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to 150°C
Lead Temperature (soldering, 10s)	+300°C
ESD Susceptibility(2) - HBM (Human Body Mode)	±6000V
ESD Susceptibility(2) - MM (Machine Mode)	±400V

Note (1): Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Note (2): This integrated circuit can be damaged by ESD. UltraChip recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

PACKAGE/ORDERING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Package Qty	Eco Plan
UC6528xBNQ4GRC-1	ACTIVE	QFN	QFN4x4-16 pins	Tape, 5000	Green (RoHS & no Sb/Br)
UC6528xBNQ4GR7-1	ACTIVE	QFN	QFN4x4-16 pins	Tape, 2500	Green (RoHS & no Sb/Br)
UC6528xBNQ3GRC-1	TBD	QFN	QFN3x3-16 pins	Tape, 5000	Green (RoHS & no Sb/Br)
UC6528xBNQ3GR7-1	TBD	QFN	QFN3x3-16 pins	Tape, 2500	Green (RoHS & no Sb/Br)

GENERAL NOTES

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

CONTACT DETAILS

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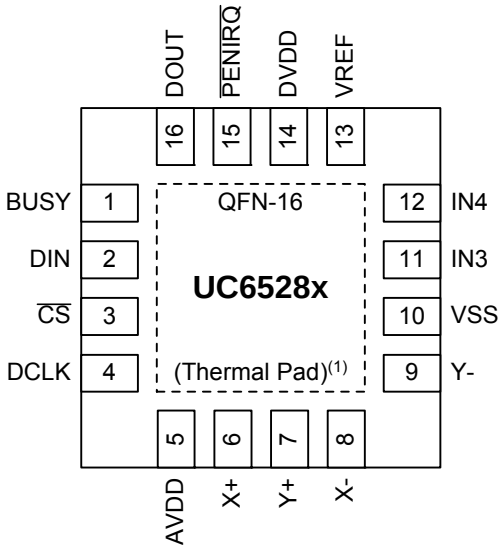
PIN CONFIGURATION



(1) The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	BUSY	Busy Output. This output is high impedance when $\overline{CS}$ is HIGH.
2	DIN	Serial Data Input. If $\overline{CS}$ is LOW, data is latched on rising edge of DCLK.
3	$\overline{CS}$	Chip Select Input. Controls conversion timing and enables the serial input/output register.
4	DCLK	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.
5	AVDD	Power Supply, 2.2V to 3.6V.
6	X+	X+ Position Input. ADC input channel 1.
7	Y+	Y+ Position Input. ADC input channel 2.
8	X-	X- Position Input.
9	Y-	Y- Position Input.
10	VSS	Ground.
11	IN3	Auxiliary Input 1. ADC input channel 3.
12	IN4	Auxiliary Input 2. ADC input channel 4.
13	VREF	Voltage Reference Input.
14	DVDD	Power Supply, 2.2V to 3.6V.
15	$\overline{PENIRQ}$	Pen Interrupt.
16	DOUT	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{CS}$ is HIGH.

ELECTRICAL CHARACTERISTICS

At T_A=-40°C to +85°C, AVDD=DVDD=+2.7V, VREF=+2.5V, F_{SAMPLE}=125kHz, F_{CLK}=16•F_{SAMPLE}=2MHz, 12-bit Mode, and digital inputs = VSS or DVDD, unless otherwise noted.

PARAMETER	CONDITIONS	UC6528x MIN	UC6528x TYP	UC6528x MAX	UNITS
ANALOG INPUT					
Full-Scale Input Scan	Positive Input – Negative Input	0		VREF	V
Absolute Input Range	Positive Input	-0.2		AVDD+0.2	V
	Negative Input	-0.2		+0.2	V
Capacitance			25		pF
Leakage Current			0.1		µA
SYSTEM PERFORMANCE					
Resolution			12		Bits
No Missing Codes		11			Bits
Integral Linearity Error				±2	LSB(1)
Offset Error				±6	LSB
Gain Error				±4	LSB
SAMPLING DYNAMICS					
Conversion Time				12	Clocks
Acquisition Time		3			Clocks
Throughput Rate				125	kHz
Multiplexer Settling Time			500		ns
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 50kHz		100		dB
SWITCH DRIVERS					
On-Resistance					
Y+, X+			5		Ω
Y-, X-			5		Ω
REFERENCE INPUT					
Range		1.0		AVDD	V
Resistance	$\overline{CS}$ = VSS or DVDD		5		GΩ
Input Current			13	40	µA
	$\overline{CS}$ = DVDD		0.001	3	µA
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Logic Levels					
V_{IH}	$\lvert I_{IH} \rvert$ < +5µA	DVDD * 0.7		DVDD + 0.3	V
V_{IL}	$\lvert I_{IL} \rvert$ < +5µA	-0.3		DVDD * 0.3	V
V_{OH}	I_{OH} = -250µA	DVDD – 0.4			V
V_{OL}	I_{OL} = +250µA			0.4	V
POWER SUPPLY					
AVDD & DVDD	Specified Performance	2.7		3.6	V
Quiescent Current			240	600	µA
	Shutdown Mode		0.1	3	µA
Power Dissipation	AVDD = DVDD = 2.7V			1.65	mW

NOTE: (1) LSB means Least Significant Bit. With VREF equal to +2.5V, 1LSB=610µV.

THEORY OF OPERATION

The UC6528x is a classic Successive Approximation Register (SAR) ADC. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6 µm CMOS process. The basic operation of the UC6528x is shown in Figure 1. The device requires an external reference (VREF) and an external clock. It operates from a single supply of 2.2V to 3.6V (where AVDD=DVDD). The VREF can be any voltage between 1V and AVDD. The value of VREF directly sets the input range of the converter. The average VREF input current depends on the conversion rate of the UC6528x.

The analog input to the converter is provided via a 4-channel multiplexer. An unique configuration of low on-resistance switches allows an unselected ADC input channel to provide power and an accompanying pin to provide ground for an external device. By maintaining a differential input to the converter and a differential reference architecture, it's possible to ignore the switch's on-resistance error which should be a source of error for the particular measurement.

ANALOG INPUT

See Figure 2 for a block diagram of the input multiplexer on the UC6528x, the differential input and differential reference of the ADC. Table 1 and Table 2 show the relationship between the A2, A1, A0, & SER/$\overline{\text{DFR}}$ control bits and the configuration of the UC6528x. The control bits are provided serially via the DIN pin - see the Digital Interface section of this data sheet for details.

When the converter enters the hold mode, the voltage difference between the +IN and -IN input (See Figure 2) is captured on the internal capacitor array. The input current on the analog input depends on the conversion rate of the device. During the sa- mple period, the source must charge the internal capacitor array (typically 25pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

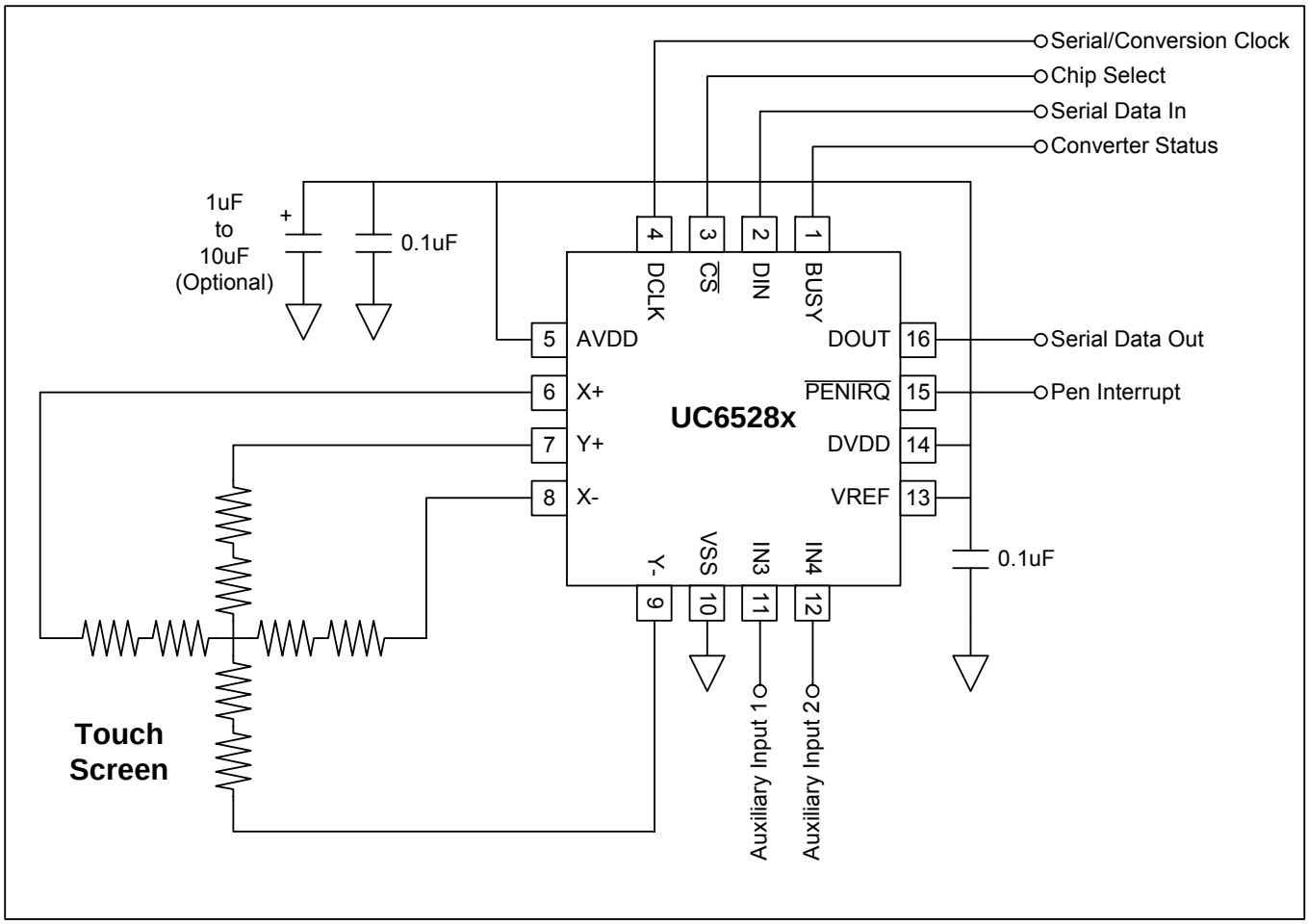


Figure 1. Typical Operation of the UC6528x

TABLE 1. Input Configuration, Single -Ended Reference Mode (SER/$\overline{DFR}$ = HIGH)

A2	A1	A0	X+	Y+	IN3	IN4	IN-(1)	X SWITCHES	Y SWITCHES	REF+(1)	REF-(1)
0	0	1	IN+				VSS	OFF	ON	VREF	VSS
1	0	1		IN+			VSS	ON	OFF	VREF	VSS
0	1	0			IN+		VSS	OFF	OFF	VREF	VSS
1	1	0				IN+	VSS	OFF	OFF	VREF	VSS

TABLE 2. Input Configuration, Single -Ended Reference Mode (SER/$\overline{DFR}$ = LOW)

A2	A1	A0	X+	Y+	IN3	IN4	IN-(1)	X SWITCHES	Y SWITCHES	REF+(1)	REF-(1)
0	0	1	IN+				Y-	OFF	ON	Y+	Y-
1	0	1		IN+			X-	ON	OFF	X+	X-
0	1	0			IN+		VSS	OFF	OFF	VREF	VSS
1	1	0				IN+	VSS	OFF	OFF	VREF	VSS

NOTE (1): Internal node, for clarification only, not directly accessible by the user.

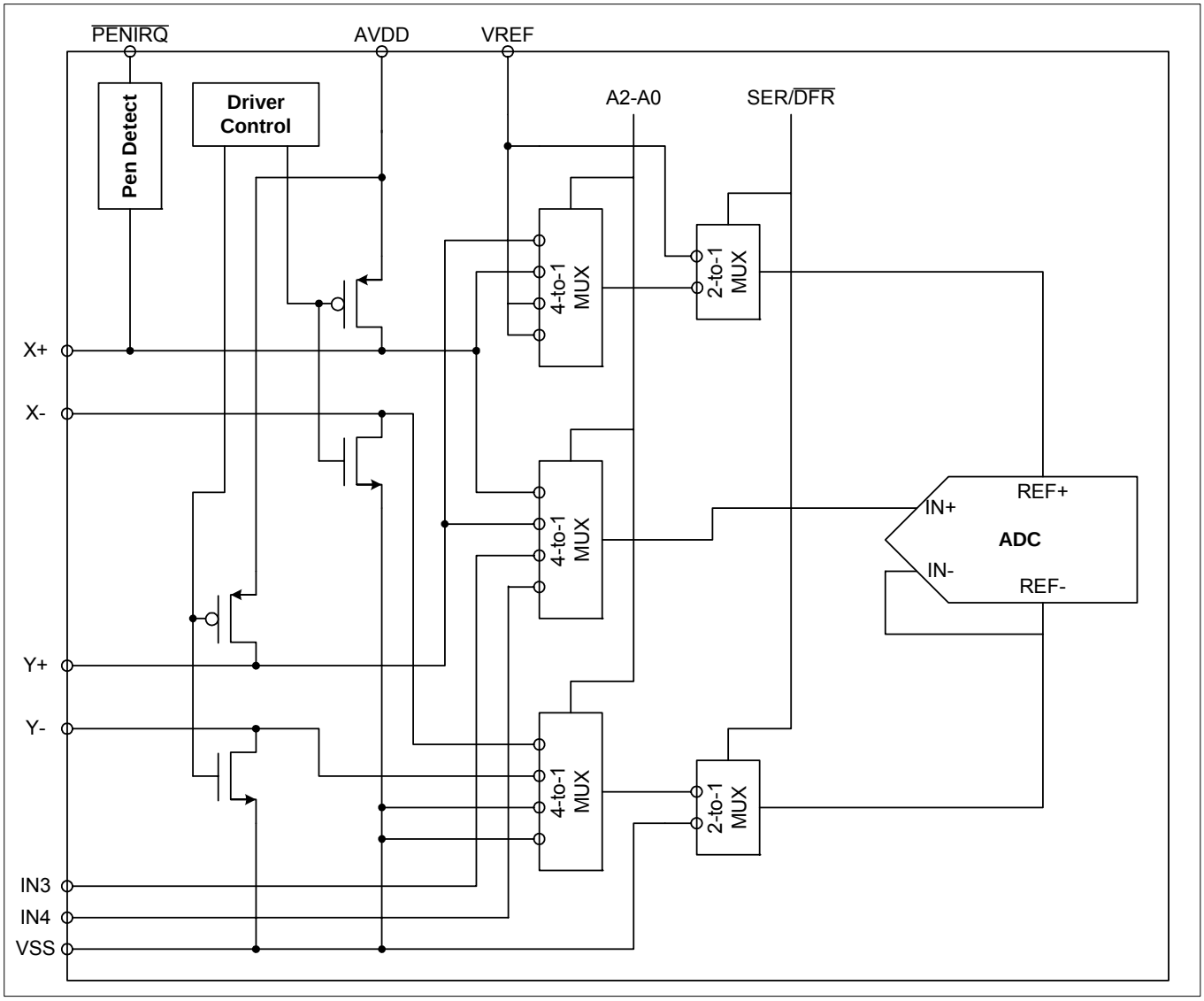


FIGURE 2. Simplified Diagram of Analog Input.

REFERENCE INPUT

The voltage difference between REF+ and REF- (shown in Figure 2) sets the analog input range. The UC6528x will operate with a reference in the range of 1V to AVDD. There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. Any offset or gain error inherent in the ADC will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given ADC is 2LSBs with a 2.5V reference, it will typically be 5LSBs with a 1V reference. In each case, the actual offset of the device is the same, 1.22mV. With a lower reference voltage, more care must be taken to provide a clean PCB layout including adequate bypassing, a clean (low noise, low ripple) power supply, low noise reference and input signal.

The voltage into the VREF input is not buffered and directly drives the Capacitor Digital-to-Analog Converter (CDAC) portion of the UC6528x. Typically, the input current is 13uA with VREF=2.7V and F_{SAMPLE}=125kHz. This value will vary by a few microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce overall current drain from the reference.

There is also a critical item regarding the reference when making measurements where the switch drivers are on. For this discussion, it's useful to consider the basic operation of the UC6528x as shown in Figure 1. This particular application shows the device being used to digitize a resistive touch screen. A measurement of the current Y position of the pointing device is made by connecting the X+ input to the ADC, turning on the Y+ and Y- drivers, and digitizing the voltage on X+ (shown in Figure 3). For this measurement, the resistance in the X+ lead does not affect the conversion (it does affect the settling time, but the resistance is usually small enough so that this is not a concern).

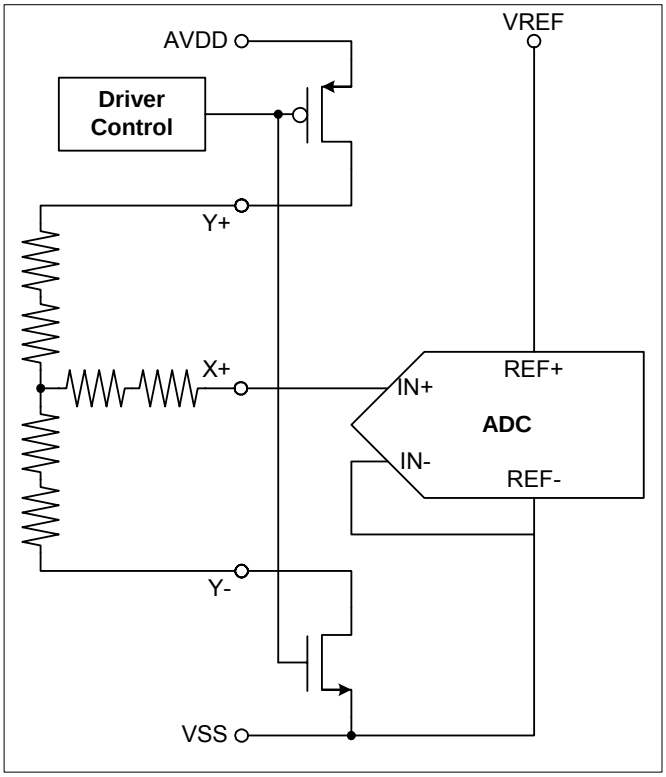


Figure 3. Simplified Diagram of Single-Ended Reference. (SER/$\overline{DFR}$ HIGH, Y Switches Enabled, X+ is Analog Input).

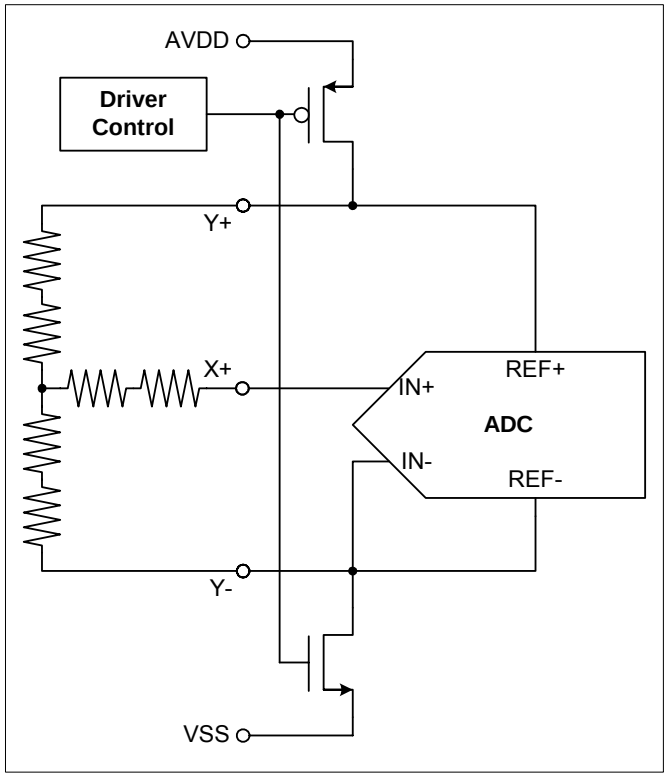


Figure 4. Simplified Diagram of Differetial Reference. (SER/DFR LOW, Y Switches Enabled, X+ is Analog Input).

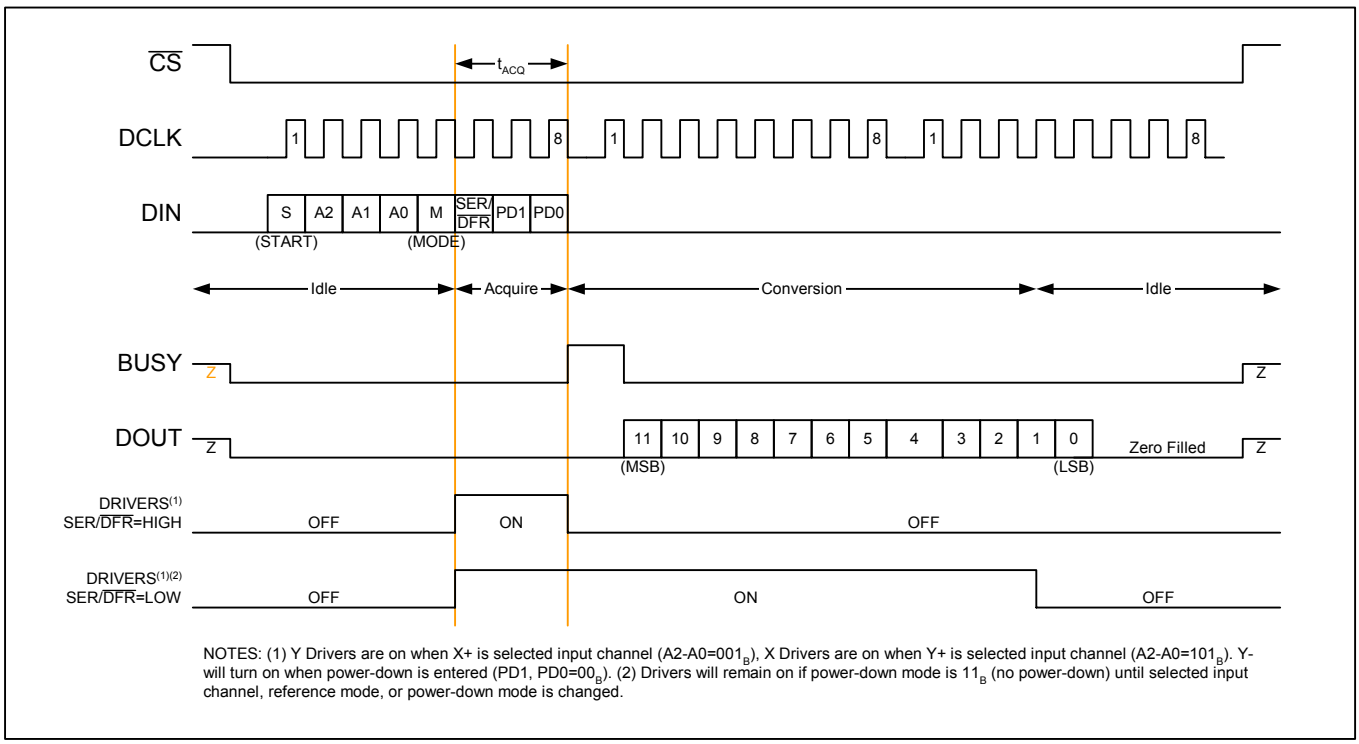
However, since the resistance between Y+ and Y- is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it would not be possible to achieve a 0V input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error.

The situation can be remedied as shown in Figure 4. By setting the SER/$\overline{DFR}$ bit LOW, the REF+ and REF- inputs are connected directly to Y+ and Y-. This makes the A/D conversion ratiometric. The result of the conversion is always a percentage of the external resistance, regardless of how it changes in relation to the on-resistance of the internal switches. Note that there is an important consideration regarding power dissipation when using the ratiometric mode of operation, see the Power Dissipation section for more details.

As a final note about the differential reference mode, it must be used with AVDD as the source of the REF+ voltage and cannot be used with VREF. It's possible to use a high precision reference on VREF and single-ended reference mode for measurements which do not need to be ratiometric. Or, in some cases, it could be possible to power the ADC directly from a precision reference. Most references can provide enough power for the UC6528x, but they might not be able to supply enough current for the external load (such as resistive touch screen).

TOUCH SCREEN SETTLING

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (for example, noise generated by the LCD panel or backlight circuitry). These capacitors provide a low-pass filter to reduce the noise, but cause a settling time requirement when the panel is touched that typically shows up as a gain error. There are several methods for minimizing or eliminating this issue. The problem is that the input and/or reference has not settled to the final steady-state value prior to the ADC sampling the input(s) and providing the digital output. Additionally, the reference voltage may still be changing during the measurement cycle. Option 1 is to stop or slow down the UC6528x DCLK for the required touch screen settling time. This option allows the input and reference to have stable values for the Acquire period (3 clock cycles of the UC6528x; see Figure 5). This option works for both the single-ended and the differential modes. Option 2 is to operate the UC6528x in the differential mode only for the touch screen measurements and command the UC6528x to remain on (touch screen drivers ON) and not go into power-down (PD0=1). Several conversions are made, depending on the settling time required and the UC6528x data rate. Once the required number of conversions have been made, the processor commands the UC6528x to go into its power-down state on the last measurement. This process is required for X-Position ad Y-Position measurements. Option 3 is to operate in the 15 Clock-per-Conversion mode, which overlaps the analog-to-digital conversions and maintains the touch screen drivers on until commanded to stop by the processor (see Figure 10).



NOTES: (1) Y Drivers are on when X+ is selected input channel (A2-A0=001_B), X Drivers are on when Y+ is selected input channel (A2-A0=101_B). Y- will turn on when power-down is entered (PD1, PD0=00_B). (2) Drivers will remain on if power-down mode is 11_B (no power-down) until selected input channel, reference mode, or power-down mode is changed.

Figure 5. Conversion Timing, 24 Clocks per Conversion, 8-bit Bus Interface. No DCLK Delay Required with Dedicated Serial Port.

DIGITAL INTERFACE

Figure 5 shows the typical operation of the UC6528x's digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface. Each communication between the processor and the converter consists of eight clock cycles. One complete conversion can be accomplished with three serial communications, for a total of 24 clock cycles on the DCLK input.

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer, switches, and reference inputs appropriately, the converter enters the acquisition (sample) mode and, if needed, the internal switches are turned on. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the hold mode and the internal switches may turn off. The next 12th clock cycles accomplish the actual A/D conversion. If the conversion is ratiometric (SER/$\overline{\text{DFR}}$ LOW), the internal switches are on during the conversion. A 13th clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be LOW). These will be ignored by the converter.

CONTROL BYTE

See Figure 5 for the placement and order of the control bits within the control byte. Tables 3 & 4 give detailed information about these bits. The first bit, the (S) bit, must always be HIGH and indicates the start of the control byte. The UC6528x will ignore inputs on the DIN pin until the start bit is detected. The next three bits (A2-A0) select the active input channel or channels of the input multiplexer (see Tables 1 & 2 and Figure 2). The MODE bit determines the number of bits for each conversion, either 12 bits (LOW) or 8 bits (HIGH). The SER/$\overline{\text{DFR}}$ bit controls the reference mode: either single-ended (HIGH) or differential (LOW). (The differential mode is also referred to as the ratiometric conversion mode.) In single-ended mode, the converter' s reference voltage is always the difference between the VREF and VSS pins. In differential mode, the reference voltage is the difference between the currently enabled switches. See Tables 1 & 2 and Figures 2 through 4 for more information. The last two bits (PD1-PD0) select the power-down mode as shown in Table 5. If both inputs are HIGH, the device is always powered up. If both inputs are LOW, the device enters a power-down mode between conversions. When a new conversion is initiated, the device will resume normal operation instantly - no delay is needed to allow the device to power up and the very first conversion will be valid. There are two power-down modes: one where $\overline{\text{PENIRQ}}$ is disabled and one where it is enabled.

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	MODE	SER/$\overline{\text{DFR}}$	PD1	PD0

TABLE 3. Order of the Control Bits in the Control Byte.

BIT	NAME	DESCRIPTION
7	S	Start Bit. Control byte starts with first HIGH bit on DIN. A new control byte can start every 16th clock cycle in 12-bit conversion mode or every 12th clock cycle in 8-bit conversion mode.
6-4	A2-A0	Channel Select Bits. Along with the SER/$\overline{\text{DFR}}$ bit, these bits control the setting of the multiplexer input, switches, and reference inputs, see Tables 1 & 2.
3	MODE	12-Bit / 8-Bit Conversion Select Bit. This bit controls the number of bits for the following conversion: 12 bits (LOW) or 8 bits (HIGH).
2	SER/$\overline{\text{DFR}}$	Single-Ended / Differential Reference Select Bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input, switches, and reference inputs, see Tables 1 & 2.
1-0	PD1-PD0	Power-Down Mode Select Bits. See Table 5 for details.

TABLE 4. Descriptions of the Control Bits Within the Control Byte.

16-CLOCKS PER CONVERSION

The control bits for conversion n + 1 can be overlapped with conversion "n" to allow for a conversion every 16 clock cycles, as shown in Figure 6. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer between the processor and the converter.

This is possible provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that has been captured on the input sample-and-hold may droop enough to affect the conversion result. Note that the UC6528x is fully powered while other serial communications are taking place during a conversion.

PD1	PD0	$\overline{\text{PENIRQ}}$	DESCRIPTION
0	0	Enabled	Power-down between conversions. When each conversion is finished, the converter enters a low power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid. The Y- switch is on while in power-down.
0	1	Disabled	Same as mode 00, except $\overline{\text{PENIRQ}}$ is disabled. The Y- switch is off while in power-down mode.
1	0	Disabled	Reserved for future use.
1	1	Disabled	No power-down between conversions, device is always powered.

TABLE 5. Power-Down Selection.

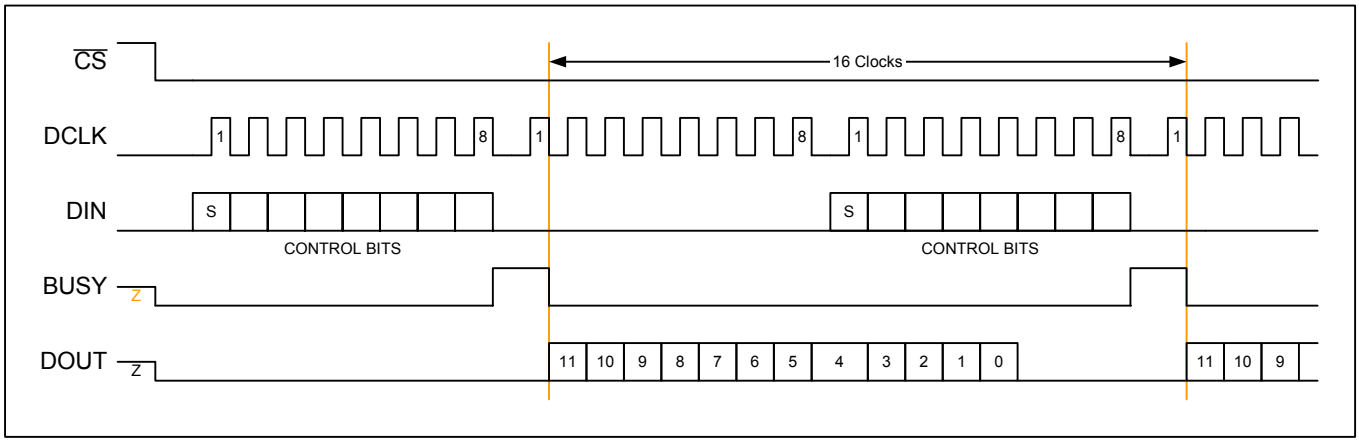


Figure 6. Conversion Timing, 16 Clocks per Conversion, 8-bit Bus Interface. No DCLK Delay Required with Dedicated Serial Port.

DIGITAL TIMING

Figure 7 and Table 6 provide detailed timing for the digital interface of the UC6528x.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	1500			ns
t_{DS}	DIN valid Prior to DCLK Rising	100			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Valid			200	ns
t_{DV}	$\overline{\text{CS}}$ Falling to DOUT Enabled			200	ns
t_{TR}	$\overline{\text{CS}}$ Risng to DOUT Disabled			200	ns
t_{CSS}	$\overline{\text{CS}}$ Falling to First DCLK Rising	100			ns
t_{CSH}	$\overline{\text{CS}}$ Risng to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	200			ns
t_{CL}	DCLK LOW	200			ns
t_{BD}	DCLK Falling to BUSY Rising			200	ns
t_{BDV}	$\overline{\text{CS}}$ Falling to BUSY Enabled			200	ns
t_{BTR}	$\overline{\text{CS}}$ Risng to BUSY Disabled			200	ns

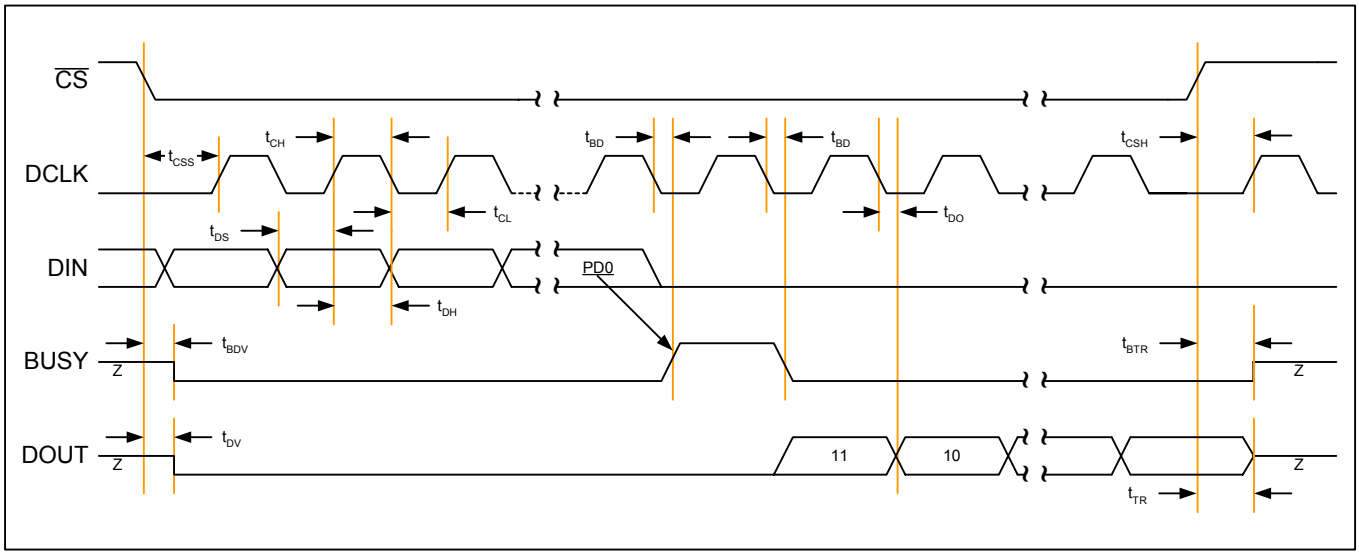


Figure 7. Detailed Timing Diagram.

DATA FORMAT

The UC6528x output data is in Straight Binary format, as shown in Figure 8. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

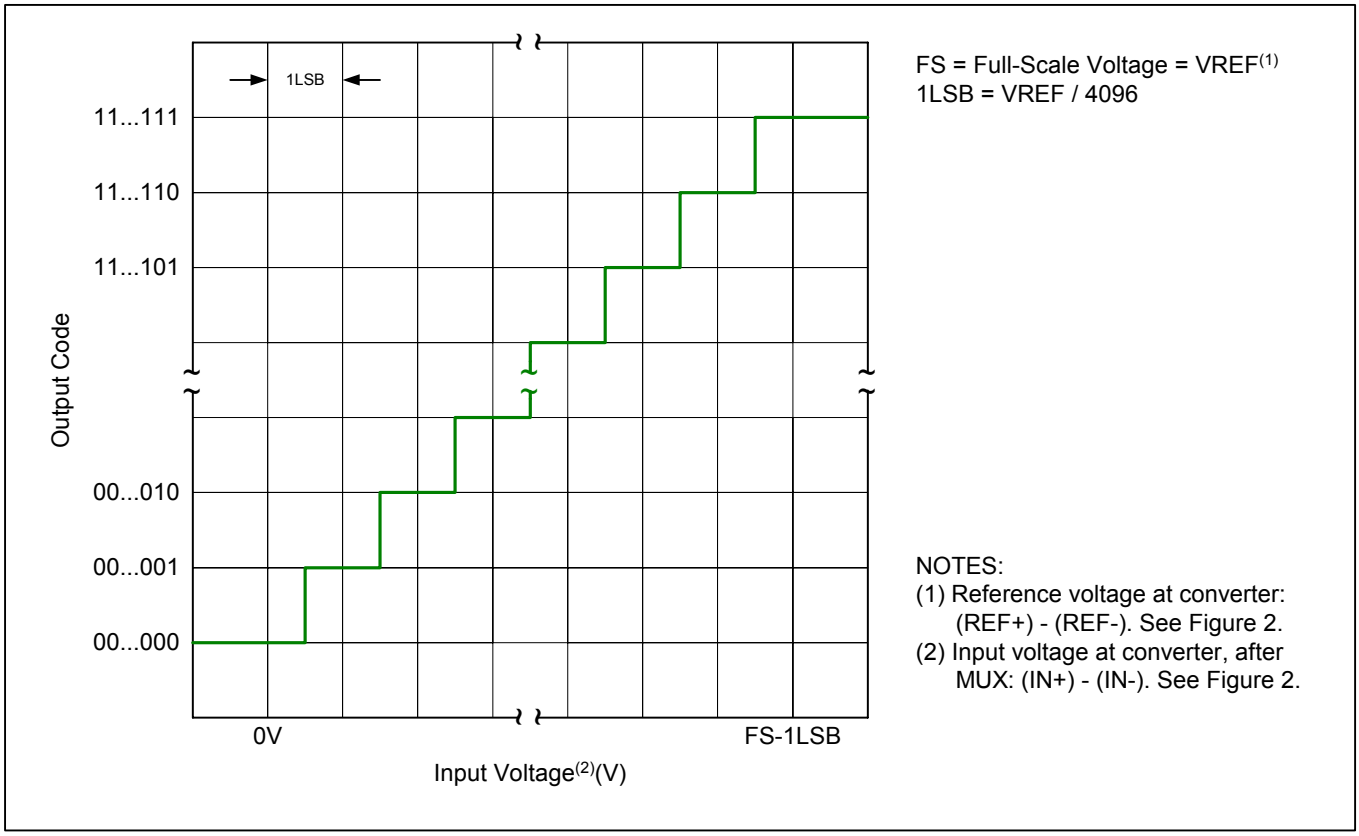


Figure 8. Ideal Input Voltage versus Output Codes.

8-BIT CONVERSION

The UC6528x provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. This could be used in conjunction with serial interfaces that provide 12-bit transfers or two conversions could be accomplished with three 8-bit transfers, as shown in Figure 9. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at a faster clock rate. This is because the internal settling time of the UC6528x is not as critical - settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.

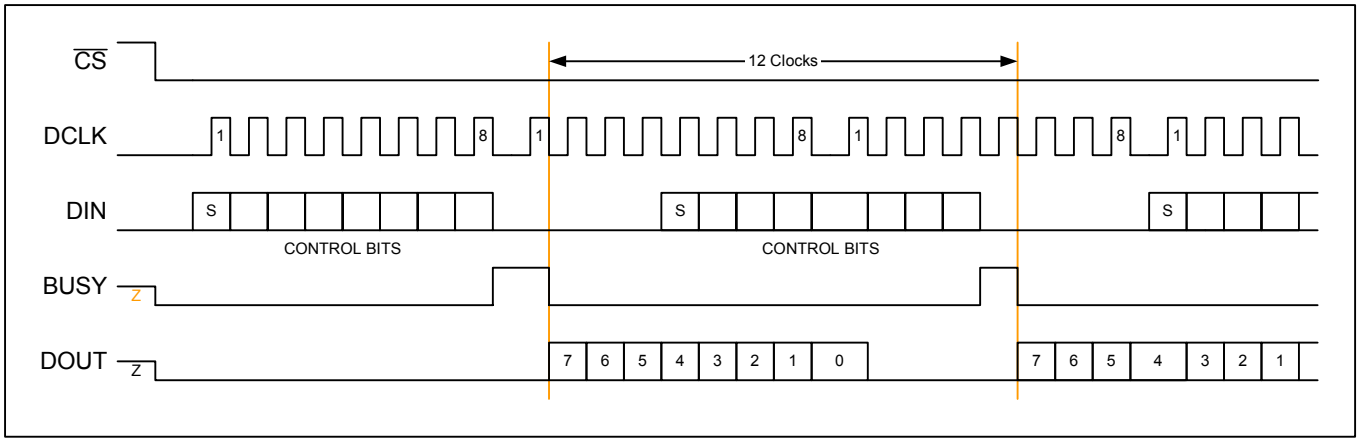


Figure 9. Conversion Timing, 12 Clocks per Conversion, MODE = HIGH, 8-bit Bus Interface. No DCLK Delay Required with Dedicated Serial Port.

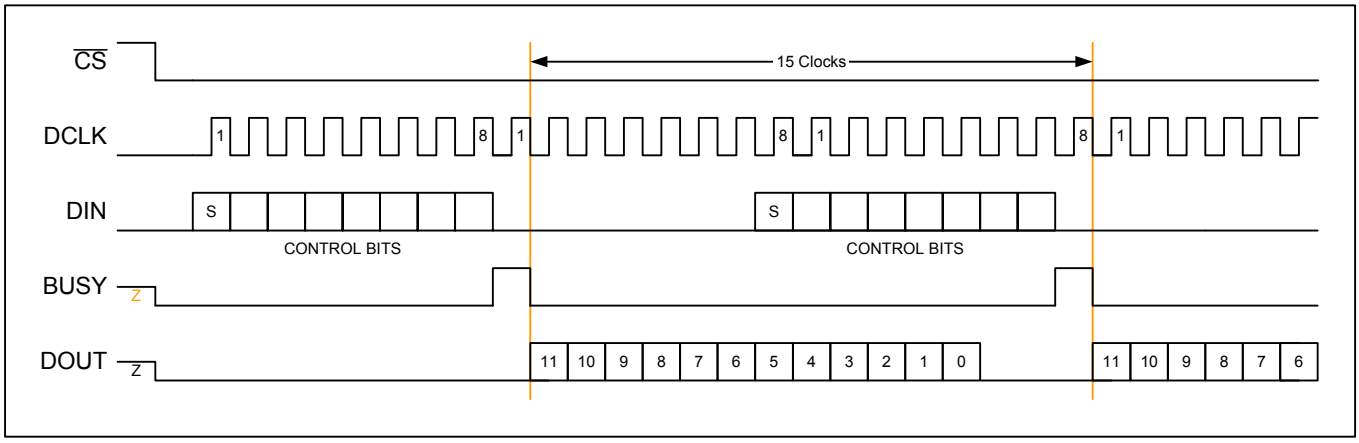


Figure 10. Maximum Conversion Rate, 15 Clocks-per-Conversion, MODE=LOW.

POWER DISSIPATION

There are two major power modes for the UC6528x: full power (PD1-PD0=11_B) and auto power-down (PD1-PD0=00_B). When operating at full speed and 16 clocks per conversion (see Figure 6), the UC6528x spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Therefore, the difference between full power mode and auto power-down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion but conversions are simply done less often, the difference between the two modes is dramatic. Another important consideration for power dissipation is the reference mode of the converter. In the single-ended reference mode, the converter's internal switches are on only when the analog input voltage is being acquired (see Figure 5). Thus, the external device, such as a resistive touch screen, is only powered during the acquisition period. In the differential reference mode, the external device must be powered throughout the acquisition and conversion periods (see Figure 5). If the conversion rate is high, this could substantially increase power dissipation.

$\overline{\text{PENIRQ}}$ OUTPUT

The UC6528x equips a internal pull-up resistor to $\overline{\text{PENIRQ}}$. While in power-down mode with PD1-PD0=00_B, the Y-Driver is on and connects the Y-plane of the touch screen to VSS. The $\overline{\text{PENIRQ}}$ input is connect to the X+ input through a analog switch. When the screen is touched, the X+ input is pulled to ground through the touch screen, and $\overline{\text{PENIRQ}}$ output goes LOW, initiating an interrupt to the processor. During the measurement cycle for X and Y position, the X+ input is disconnected from $\overline{\text{PENIRQ}}$ input. This disconnection is done to eliminate any leakage current from the internal pull-up resistor through the touch screen, thus causing no error.

LAYOUT, GROUNDING, AND BYPASSING

The following layout suggestions provide the most optimum performance from the UC6528x. Many portable applications, however, have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly clean power and grounds because most of the internal components are very low power. This situation means less bypassing for the converter power and less concern regarding grounding. Still, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the UC6528x circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches can originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the UC6528x should be clean and well bypassed. A 0.1uF ceramic bypass capacitor should be placed as close to the device as possible. A 1uF to 10uF capacitor may also be needed if the impedance of the connection between AVDD or DVDD and the power supplies is high. Low-leakage capacitors should be used to minimize power dissipation through the bypass capacitors when the UC6528x is in power-down mode.

The reference should be similarly bypassed with a 0.1uF capacitor. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation. The UC6528x draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of DCLK during a conversion).

The UC6528x architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. Whereas high-frequency noise can be filtered out, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The VSS pin must be connected to a clean ground point. In many cases, this is the analog ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery connection point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Although resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Longer connections are a source of error, much like the on-resistance of the internal switches. Likewise, loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch screen applications (e.g., applications that require a backlit LCD panel). This EMI noise can be coupled through the LCD panel to the touch screen and cause flickering of the converted data. Several things can be done to reduce this error, such as using a touch screen with a bottom-side metal layer connected to ground to shunt the majority of noise to ground. Additionally, filtering capacitors from Y+, Y-, X+, and X- pins to ground can also help. Caution should be observed under these circumstances for settling time of the touch screen, especially operating in the single-ended mode and at high data rates.

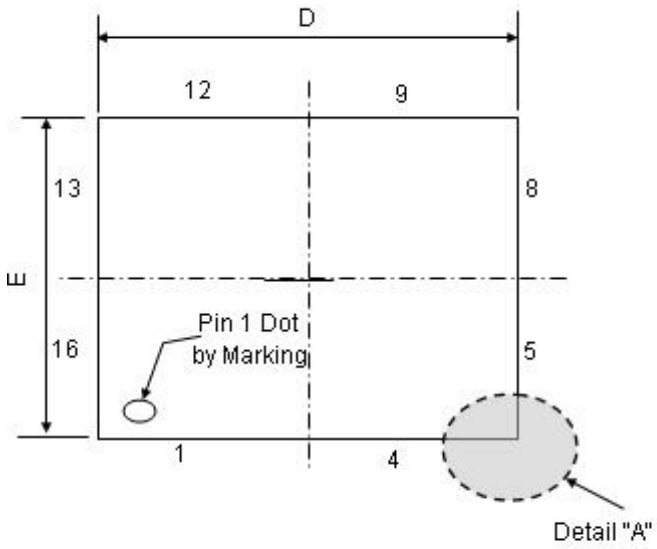
PACKAGE DIMENSION

QFN 4x4 16 PINS

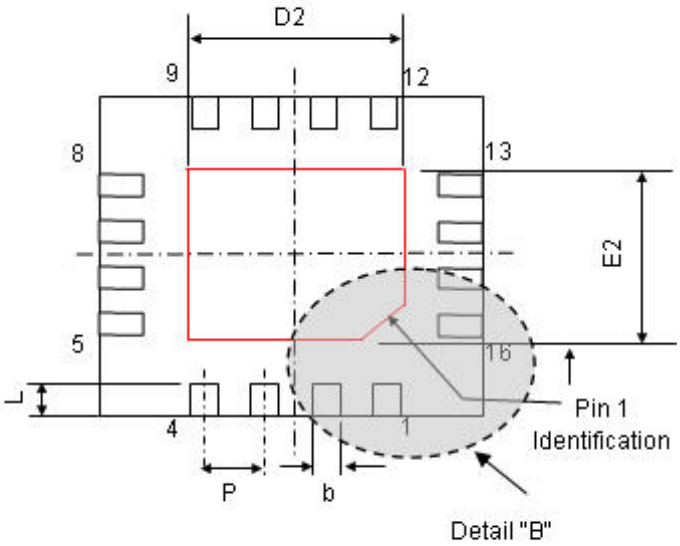
DIMENSION	MIN	TYP	MAX	UNIT
A	0.65	0.75	0.85	mm
A1	0.005	0.020	0.050	mm
A2	0.177	0.203	0.280	mm
b	0.25	0.30	0.35	mm
C	--	0.45REF	--	mm
D	3.95	4.00	4.05	mm

DIMENSION	MIN	TYP	MAX	UNIT
D2	2.35	2.40	2.45	mm
E	3.95	4.00	4.05	mm
E2	2.35	2.40	2.45	mm
L	0.50	0.55	0.60	mm
P	--	0.65BSC	--	mm
S	--	0.2REF	--	mm

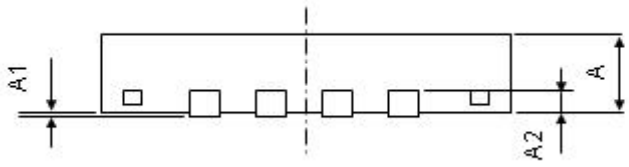
TOP VIEW

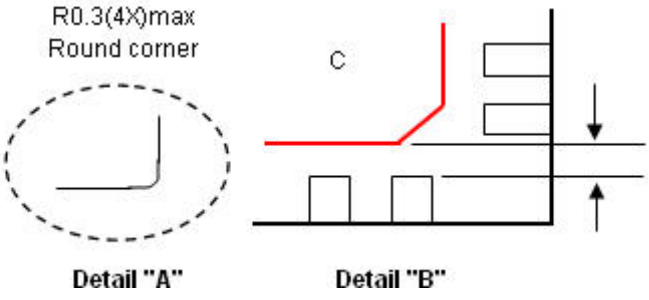


BOTTOM VIEW



Side VIEW



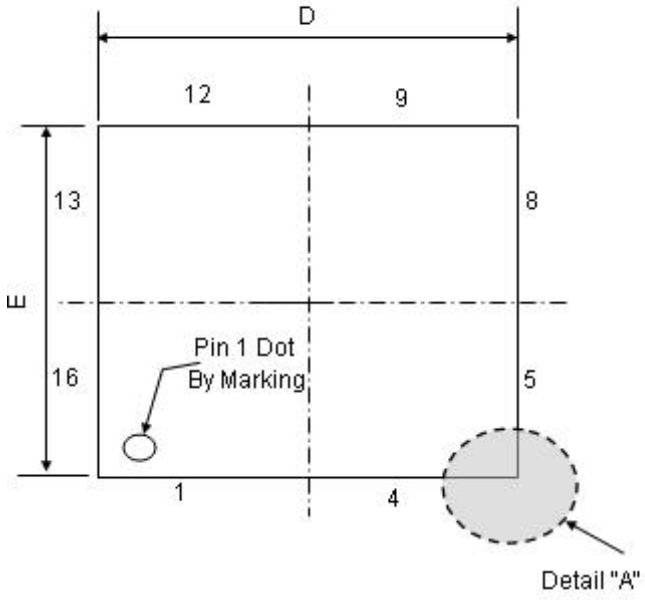


QFN3x3 – 16 PINS

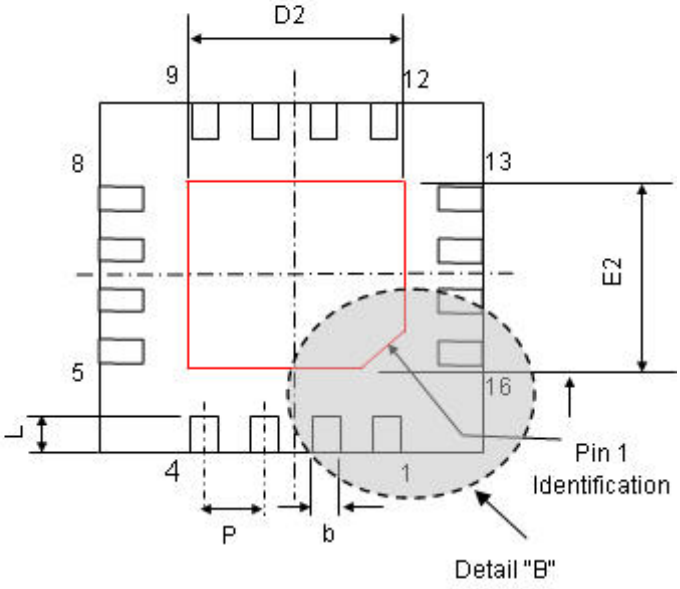
DIMENSION	MIN	TYP	MAX	UNIT
A	0.65	0.75	0.85	mm
A1	0.005	0.020	0.050	mm
A2	0.177	0.203	0.280	mm
b	0.18	0.24	0.30	mm
C	--	0.25REF	--	mm
D	2.95	3.00	3.05	mm

DIMENSION	MIN	TYP	MAX	UNIT
D2	--	1.7REF	--	mm
E	2.95	3.00	3.05	mm
E2	--	1.7REF	--	mm
L	0.30	0.40	0.50	mm
P	0.45	0.50	0.55	mm
S	--	0.25REF	--	mm

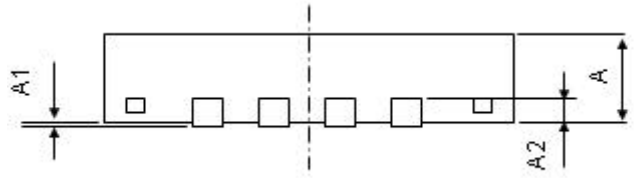
TOP VIEW

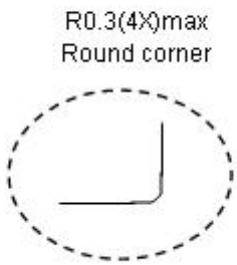


BOTTOM VIEW

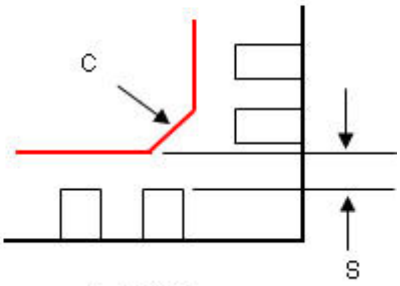


Side VIEW





Detail "A"



Detail "B"