NEC
NEC Electronics Inc.

μPD72065/65B
CMOS Floppy-Disk Controller

T-52-33-61

Description

The μPD72065/65B CMOS Floppy-Disk Controller (FDC) is NEC's follow-on to the μPD765A/B. (μPD72065B is a functionally enhanced version of μPD72065.) The FDC is an LSI chip containing the circuitry and control functions for interfacing a processor to four floppy-disk drives (FDDs). It is capable of either IBM 3740 single-density format (FM) or IBM system 34 double-density format (MFM), including double-sided recording.

Control signals of the FDC simplify the design of an external phase-locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy-disk interface.

Handshaking signals of the FDC make DMA operation easy to incorporate with the aid of an external DMA controller chip, such as the μPD8257. In DMA mode, the processor need only load the command into the FDC; all data transfers occur under control of the FDC and DMA controllers. In non-DMA mode, the FDC generates interrupts to the processor every time a data byte is to be transferred.

The FDC will execute the 19 commands listed below. Most of the commands require multiple 8-bit bytes to fully specify the operation that the processor wants the FDC to perform.

- Read Data
- Read ID
- Specify
- Read Diagnostics
- Scan Equal
- Scan High or Equal
- Scan Low or Equal
- Sense Drive Status
- Reset Standby
- Version
- Read Deleted Data
- Write Data
- Write ID
- Write Deleted Data
- Seek
- Recalibrate
- Sense Interrupt Status
- Set Standby
- Software Reset

Features

Internal address mark detection circuitry of the FDC simplifies the phase-locked loop and read electronics. Track stepping, head load time, and head unload time are user-programmable. Additional features are multitrack and multiside read and write commands plus single- and double-density capabilities.

- 100% 765A/B microcode compatibility
- Sony (ECMA) compatible recording format
- IBM-compatible format (single- and double-density)
- Multisector and multitrack transfer capability
- Interface processor with up to four floppy-disk or microfloppy-disk drives
- Data scan capability: single sector or entire cylinder, comparing host memory and disk data byte-by-byte
- Data transfers in DMA and non-DMA modes
- Parallel seek operations on up to four disk drives
- Compatible with μPD8080/85, μPD8086/88, and μPD780 (Z80®) microprocessors
- Single-phase clock (8 MHz maximum)
- +5-volt power supply
- CMOS technology

Ordering Information

Part Number		Package	Note
μPD72065C		40-pin plastic DIP (600 mil)	
	65G	52-pin plastic miniflat (3.5-mm leads)	3
	65GC	52-pin plastic miniflat (1.8-mm leads)	3
	65L	44-pin PLCC	
μPD72065BC		40-pin plastic DIP (600 mil)	2
	65BGC-3B6	52-pin plastic miniflat (1.8-mm leads)	2, 3
	65BL	44-pin PLCC	2

Notes:

(1) The basic part numbers are μPD72065 and μPD72065B. Suffix codes are added to identify particular packages.

(2) The part is under development.

(3) Surface-mount conditions differ among the miniflat packages, as in reflow soldering. The NEC sales staff can provide details.

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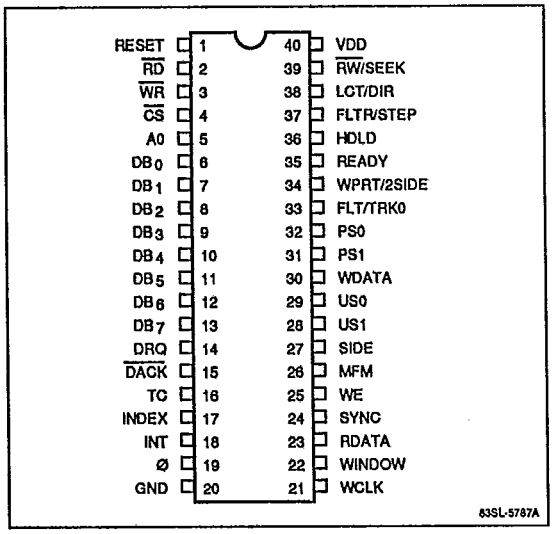
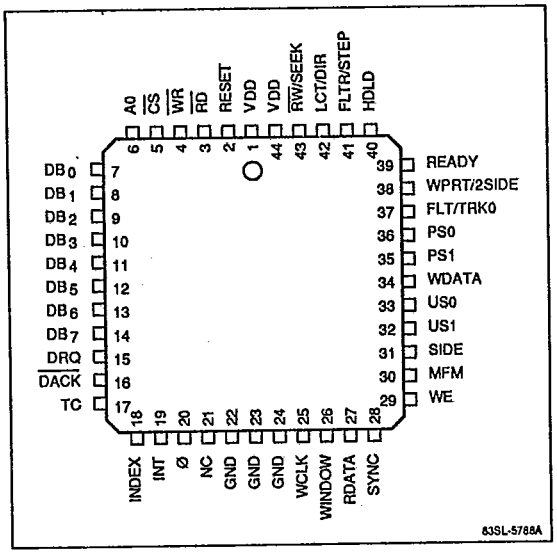
Pin Configurations

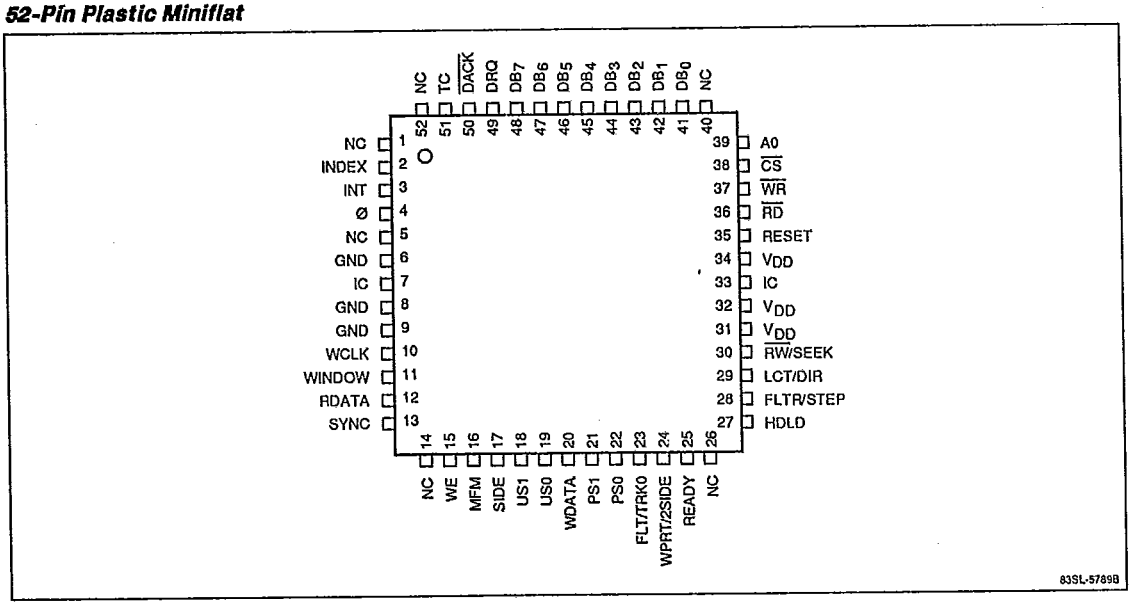
40-Pin Plastic DIP



44-Pin PLCC (Plastic Leaded Chip Carrier)



52-Pin Plastic Miniflat



Pin Identification

Symbol	I/O	Function
A0	In	Via the address bus, selects internal status register (0) or data register (1)
$\overline{CS}$	In	Chip select. Enables RD and WR signals.
$\overline{DACK}$	In	DMA acknowledge.
DB_0-DB_7	I/O	Bidirectional three-state data bus. At reset, bus goes to input mode.
DRQ	Out	DMA request. Request for data transfer in DMA mode.
FLT/TRK0	In	FLT (Fault). In read/write operation (RW/SEEK pin = 0), indicates whether FDD is in fault state. TRK0 (Track 0). In seek operation (RW/SEEK pin = 1), indicates whether FDD read/write head is positioned at cylinder 0.
FLTR/STEP	Out	FLTR (Fault read). In read/write operation (RW/SEEK pin = 0), releases FDD fault state. STEP. In seek operation (RW/SEEK pin = 1), outputs seek pulses.
HDLD	Out	Head load. Sets FDD read/write head to load state.
INDEX	In	Indicates that FDD read/write head is on the physical starting point of the track.
INT	Out	Interrupt request. Requests main system to deal with transfer of data or result of execution.
LCT/DIR	Out	LCT (Low current). In read/write operation (RW/SEEK pin = 0), indicates FDD read/write head is selecting a cylinder beyond the 42nd. DIR. In seek operation (RW/SEEK pin = 1), specifies direction, toward the outside (0) or the inside (1).
MFM	Out	Specifies function mode of VFO circuits: 0 = FM; 1 = MFM.
PS0, PS1	Out	Preshift signal requesting WDATA bit to shift in the opposite direction of expected peak shift to cancel out peak shift created when writing in MFM mode. PS0 PS1 FM MFM 0 0 No No shift 0 1 shift Delays WDATA bit 1 0 Advances WDATA bit 1 1
$\overline{RD}$	In	Control signal used by main system to read out data from FDC to data bus.
RDATA	In	Data (clock and data bits) read out from FDD. Unless both WINDOW and RDATA are input at read operation, FDC will enter deadlock state.
READY	In	Indicates FDD is in ready state.
RESET	In	Sets FDC to idle state as follows. Drive interface outputs except PS0, PS1, and WDATA (undefined) are set to low. In the main system, INT and DRQ are set to low and DB_0-DB_7 are set to input mode.
$\overline{RW}$/SEEK	Out	Selects read/write operation (0) or seek operation (1).
SIDE	Out	Selects head 0 (SIDE = 0) or head 1 (SIDE = 1) in a double-sided FDD.
SYNC	Out	VFO synchronize. Indicates FDC functional mode: read operation (1) or read operation inhibited (0).
TC	In	Terminal count. Request for data transfer termination.
US0, US1	Out	Unit select. One of four FDDs is selected by decoding US0 and US1.
WCLK	In	Write clock. Timing signal for data transfer in write operation; should also be input in read operation. Rising edges of WCLK and ϕ must be synchronized for μPD72065 but not for μPD72065B. WCLK = 16 ϕ cycles in FM mode and 8 ϕ cycles in MFM mode.
WDATA	Out	Write data (clock and data bits) to FDD.
WE	Out	Write enable. Requests write operation to FDD.
WINDOW	In	Data window signal generated by VFO circuit and used for sampling the clock and data bits of RDATA. Discrimination between clock and data bits is done in the FDC.
WPRT/2SIDE	In	WPRT (Write protected). In read/write operation (RW/SEEK pin = 0), indicates whether media is in write inhibit state. 2SIDE. In seek operation (RW/SEEK pin = 1), indicates whether a double-sided floppy disk is inserted.

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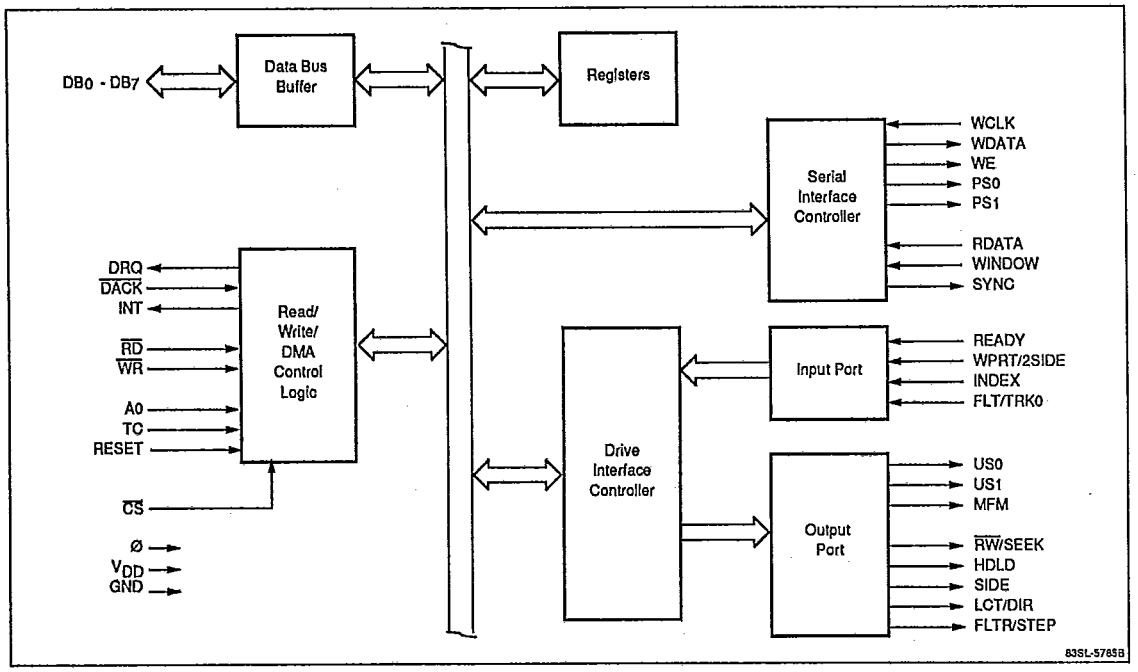
Pin Identification (cont)

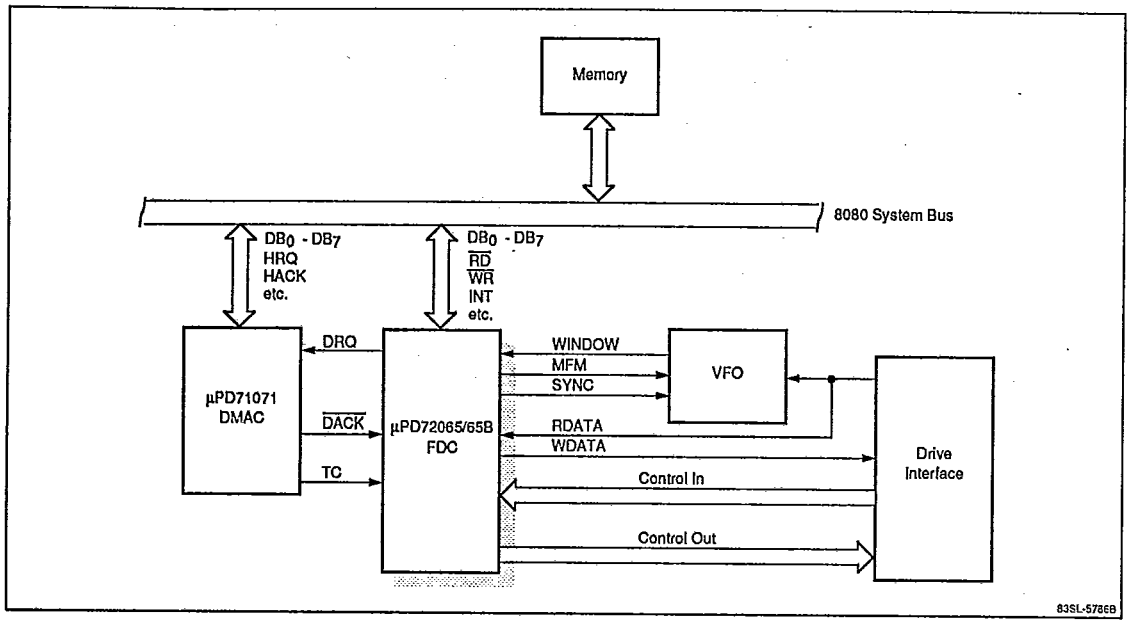
Symbol	I/O	Function
$\overline{WR}$	In	Control signal used by main system to write data on data bus to FDC.
ϕ	In	Single-phase clock: standard floppy, 8 MHz; minifloppy, 4 MHz.
GND		Ground
V_{DD}	In	+5-volt power supply
IC		Internal connection; must be left open.
NC		No connection.

Note: At reset, all output pins go to the low state except for pins PS0 and PS1, whose state is undefined.

μPD72065/65B Block Diagram



System Configuration



Absolute Maximum Ratings

T_A = +25°C

Voltage on any pin	−0.5 to +7 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Capacitance

T_A = +25°C; V_{DD} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Conditions
Clock capacitance	C_ϕ		20	pF	Unmeasured pins returned to 0 V.
Input capacitance	C_{IN}		10	pF	
Output capacitance	C_{OUT}		20	pF	

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DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Min	Max	Unit	Conditions
Input voltage, low	VI_{IL}	−0.5	0.8	V	
Input voltage, high	VI_{IH}	2.2	V_{DD} + 0.5	V	
Input voltage, low (ϕ, WCLK)	V_{IL}	−0.5	0.65	V	
Input voltage, high (ϕ, WCLK)	V_{IH}	2.2	V_{DD} + 0.5	V	
Output voltage, low	V_{OL}		0.45	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4	V_{DD}	V	I_{OH} = −200 μA
Input leakage current, low	I_{LIL}		−10	μA	V_{IN} = 0 V
Input leakage current, high	I_{LIH}		+10	μA	V_{IN} = V_{DD}
Output leakage current, low	I_{LOL}		−10	μA	V_{OUT} = +0.45 V
Output leakage current, high	I_{LOH}		+10	μA	V_{OUT} = V_{DD}
V_{DD} supply current	I_{DD}		10	mA	ϕ_{CY} = 125 ns
	I_{DD1}		500	μA	ϕ_{CY} = 125 ns
			250	μA	ϕ_{CY} = 250 ns
			100	μA	Clock stopped

AC Characteristics; Main System Side

T_A = −10 to +70°C; V_{DD} = +5 V ±10%; MFM data transfer = 500 kb/s (8 MHz), 250 kb/s (4 MHz)

Parameter	Figure	Symbol	8-MHz Operation Min	Typ	Max	4-MHz Operation Min	Typ	Max	Unit	Conditions
Clock cycle	2	ϕ_{CY}	120	125	500	240	250	500	ns	
Clock width, high/low	2	ϕ_θ	40			40			ns	
Clock rise time	2	ϕ_R			20			20	ns	
Clock fall time	2	ϕ_F			20			20	ns	
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{RD}$	3	t_{AR}	0			0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}$	3	t_{RA}	0			0			ns	
$\overline{RD}$ pulse width	3	t_{RR}	200			200			ns	
Data access time from $\overline{RD}$ ↓	3	t_{RD}			140			140	ns	
Data float delay time from $\overline{RD}$ ↑	3	t_{DF}	10		85	10		85	ns	
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{WR}$	4	t_{AW}	0			0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time to $\overline{WR}$	4	t_{WA}	0			0			ns	
$\overline{WR}$ pulse width	4	t_{WW}	200			200			ns	
Data setup time to $\overline{WR}$	4	t_{DW}	100			100			ns	
Data hold time from $\overline{WR}$	4	t_{WD}	0			0			ns	
INT delay time from $\overline{RD}$ ↑	3	t_{RI}			400			400	ns	Data transfer in non-DMA mode
INT delay time from $\overline{WR}$ ↑	4	t_{WI}			400			400	ns	
DRQ cycle time	5	t_{MCY}	13			26			μs	8-MHz: ϕ_{CY} = 125 ns 4-MHz: ϕ_{CY} = 250 ns
$\overline{DACK}$ ↓ response time from DRQ ↑	5	t_{MA}	200			400			ns	
$\overline{RD}$ ↓ response time from DRQ ↑	5	t_{MR}	125			250			ns	
$\overline{WR}$ ↓ response time from DRQ ↑	5	t_{MW}	250			500			ns	
DRQ delay time from $\overline{DACK}$ ↓	5	t_{AM}			140			140	ns	
$\overline{DACK}$ pulse width	5	t_{AA}	2			2			ϕ_{CY}	
$\overline{WR}$/$\overline{RD}$ response time from DRQ ↑	5	t_{MRW}			12			12	μs	
TC pulse width	5	t_{TC}	60			60			ns	
RESET pulse width	6	t_{RST}	14			14			ϕ_{CY}	
Clock hold time at standby	7	t_{WC}	32			32			ϕ_{CY}	
Clock setup time at standby release	7	t_{CW}	16			16			ϕ_{CY}	
INT response time from DRQ ↓	8	t_{MI}	60		77	60		77	ϕ_{CY}	μPD72065B only
INT ↑ to $\overline{DACK}$ ineffective	8	t_{IA}			1			1	ϕ_{CY}	

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AC Characteristics; Drive Side

T_A = −10 to +70°C; V_{DD} = +5 V ±10%; MFM data transfer = 500 kb/s (8 MHz), 250 kb/s (4 MHz)

Parameter	Figure	Symbol	8-MHz Operation Min	8-MHz Operation Typ	8-MHz Operation Max	4-MHz Operation Min	4-MHz Operation Typ	4-MHz Operation Max	Unit	Conditions
WCLK cycle time	9	t_{CY}		16			16		ϕ_{CY}	MFM = 0
				8			8		ϕ_{CY}	MFM = 1
WCLK width, high	9	t_ϕ	80	250	350	160	500	700	ns	8-MHz: ϕ_{CY} = 125 ns 4-MHz: ϕ_{CY} = 250 ns
WCLK, RDATA, WINDOW rise time	9	t_R			20			20	ns	
WCLK, RDATA, WINDOW fall time	9	t_F			20			20	ns	
PS0, PS1 delay time from WCLK	9	t_{CP}	10		80	10			ns	
WDATA delay time from WCLK	9	t_{CD}	10		80	10			ns	
WE delay time from WCLK	9	t_{CWE}	10		80	10			ns	
WDATA width	9	t_{WDD}	t_ϕ − 50			t_ϕ − 50			ns	
RDATA active time high	10	t_{RDD}	40			40			ns	
WINDOW cycle time	10	t_{WCY}		2			4		μs	MFM = 0
				1			2		μs	MFM = 1
WINDOW setup time to RDATA	10	t_{WRD}	15			15			ns	
WINDOW hold time from RDATA	10	t_{RDW}	15			15			ns	
US0, US1 setup time to SEEK	11	t_{US}	12			24			μs	8-MHz: ϕ_{CY} = 125 ns 4-MHz: ϕ_{CY} = 250 ns (Note 1)
SEEK setup time to DIR	11	t_{SD}	7			14			μs	
DIR setup time to STEP	11	t_{DST}	1			2			μs	
US0, US1 hold time from STEP	11	t_{STU}	5			10			μs	
STEP active time high	11	t_{STP}	6	7	8	12	14	16	μs	
US0, US1 hold time after SEEK	11	t_{SU}	15			30			μs	
SEEK hold time from DIR	11	t_{DS}	30			60			μs	
DIR hold time after STEP	11	t_{STD}	24			48			μs	
STEP cycle time	11	t_{SC}	33			66			μs	
FLTR active time high	11	t_{FR}	8		10	16		20	μs	
INDEX level high	12	t_{IDK}	4			4			ϕ_{CY}	

Notes:

(1) For the parameters on figures 11 and 12, the minimum values are 50 ns less than the values (μs) specified in the table. For example, 10 μs is actually 9.950 μs.

(2) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

Figure 1. Voltage Thresholds for Timing Measurements

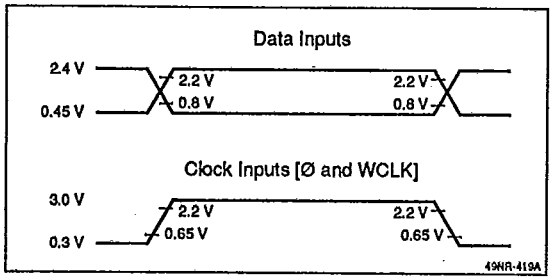


Figure 2. Clock Waveform

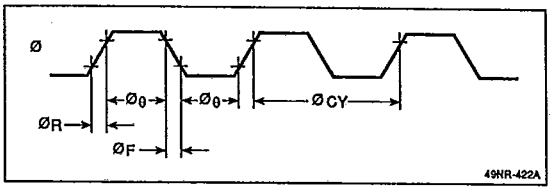


Figure 3. Read Operation

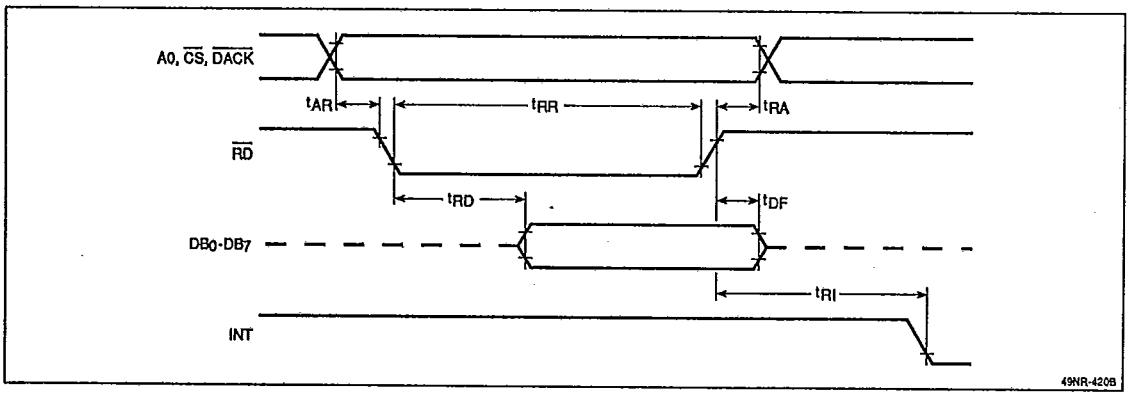


Figure 4. Write Operation

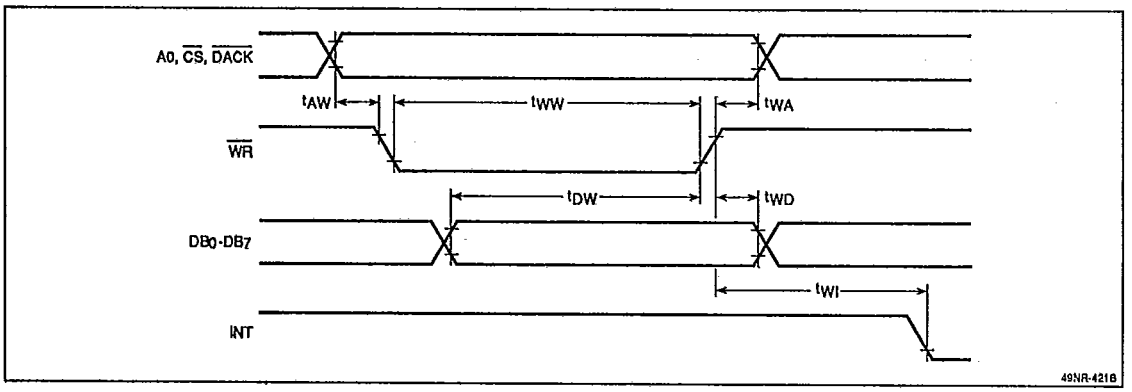


Figure 5. DMA Operation

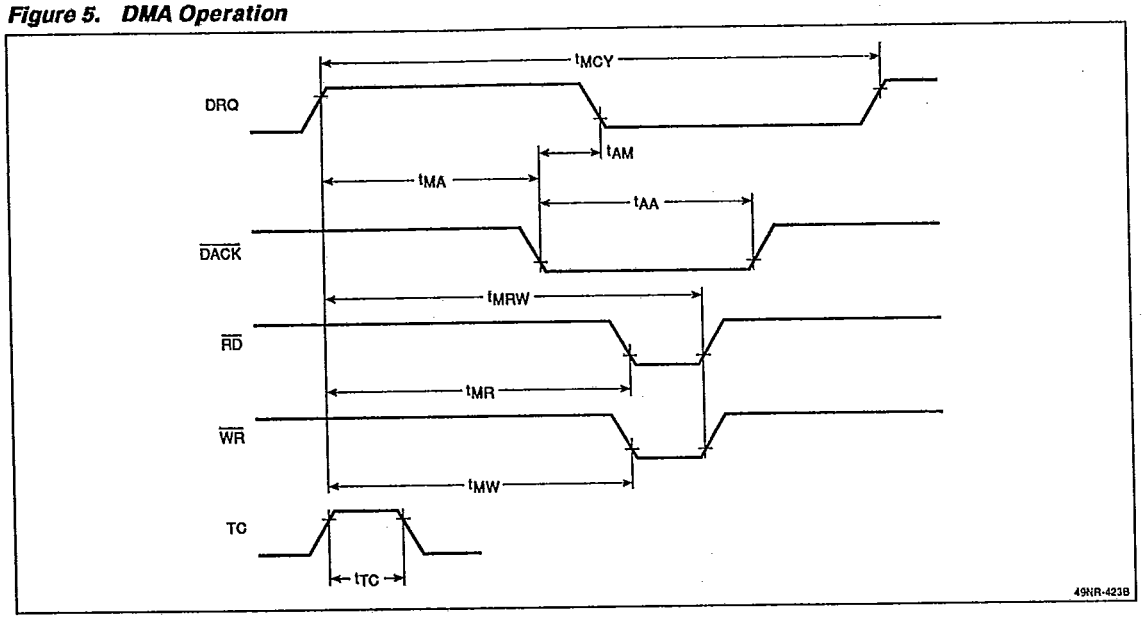


Figure 6. RESET Waveform

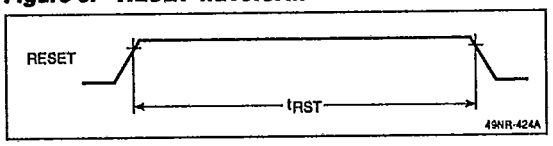


Figure 7. Standby Operation

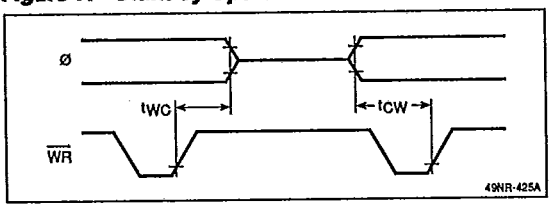


Figure 8. Overrun Operation (μPD72065B)

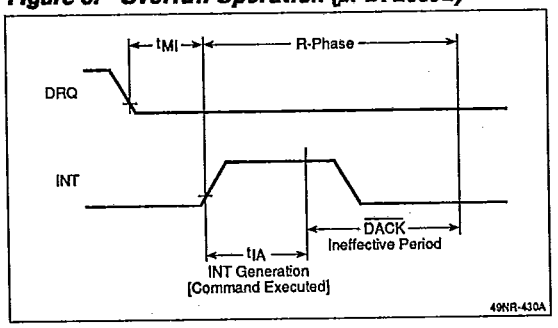


Figure 9. FDD Write Operation

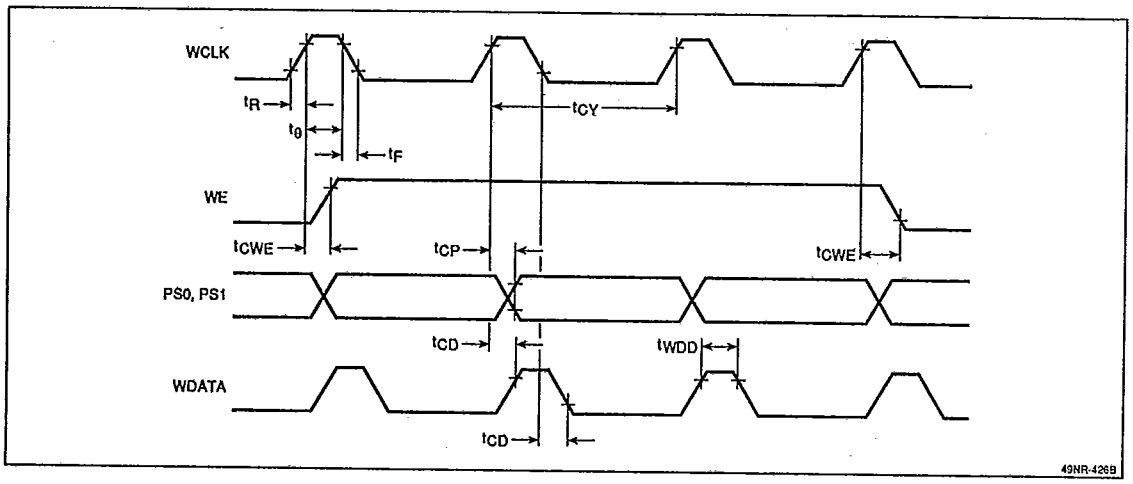


Figure 10. FDD Read Operation

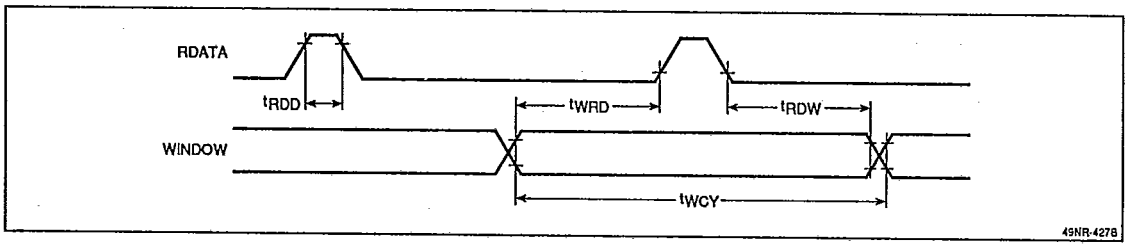


Figure 11. Seek Operation

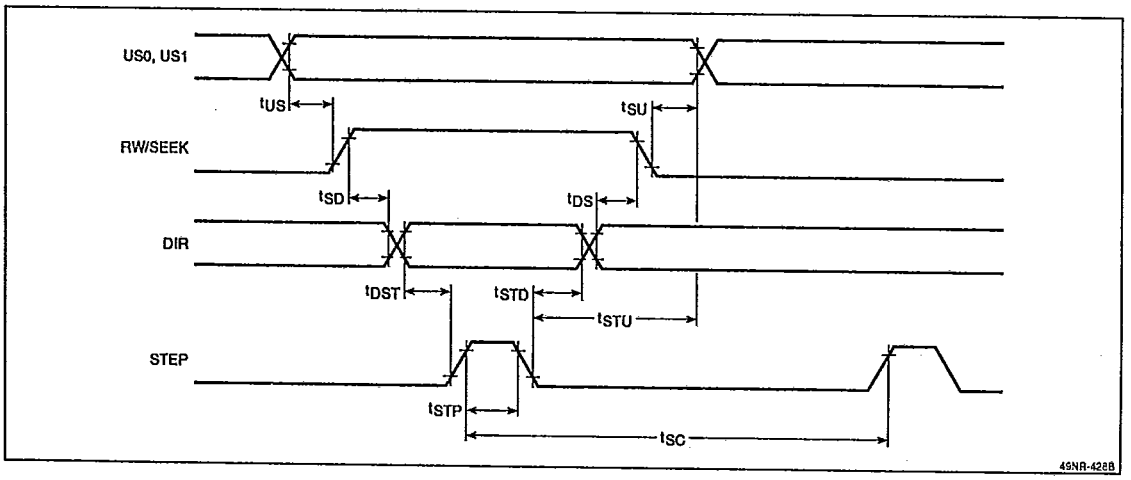
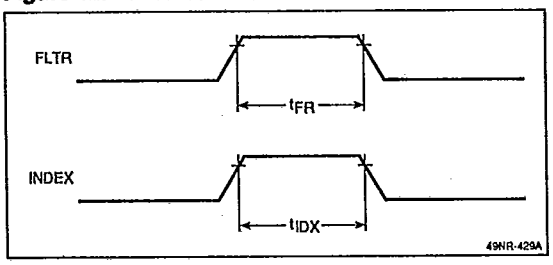


Figure 12. FLTR and INDEX Waveforms



COMPARISON, μPD72065 VS μPD72065B

The μPD72065B is a functionally enhanced version of the μPD72065. Differences are explained below.

Overrun Bit (OR)

In the μPD72065, when executing a read- or write-type command (except READ ID and SCAN types), the result status OR bit is not set if there is an overrun on the final byte of a sector. An improvement in the μPD72065B allows it to set the OR bit in any situation.

DRQ Reset

When an overrun occurs, the μPD72065 needs the $\overline{DACK}$ input to reset DRQ. If $\overline{DACK}$ is not available, an external DMA controller continues operating even after the FDC enters the R-phase, and stored result status may be transferred accidentally as ordinary data.

On the other hand, the μPD72065B resets DRQ automatically just before the R-phase entry and independent of the $\overline{DACK}$ input. See AC Characteristics for DRQ reset timing.

Clock Synchronization

The μPD72065 does not require synchronization between the ϕ clock and WCLK inputs.

VERSION Command

The VERSION command distinguishes the μPD72065B from other devices. The ST0 response to the command is:

Part No.	ST0 Value
μPD72065	80H
μPD72065B	90H

COMPARISON, μPD72065/65B VS μPD765A/B

Table 1 shows differences in the parameters and features of the FDCs.

Table 1. μPD72065/65B and μPD765A/B

Parameter	μPD72065/65B	μPD765A/B
Track format	IBM	IBM
Tracks to be recalibrated	255	77
Skipping time after index pulse detection	0.2 ms (4 MHz)	1.2 ms (4 MHz)
DRQ ↑ to RD ↓ response time		
ϕ_{CY} = 125 ns	1 x ϕ_{CY}	0.8 μs
ϕ_{CY} = 250 ns	1 x ϕ_{CY}	1.6 μs
FDD response latency after Unit select signal		
ϕ_{CY} = 125 ns	2.5 μs	0.5 μs
ϕ_{CY} = 250 ns	5.0 μs	1.0 μs
Multitrack write by tunnel erase head	Yes	No
Standby function (Standby command)	Yes	No
SOFTWARE RESET command	Yes	No

ϕ_{CY} = clock cycle time

DATA FORMAT

Figure 13 shows the data format for FM and MFM modes

Figure 13. Data Format and Timing.