Prepared Checked Approved

Product Specifications AN17850A

Ref No.ATotal Page17Page No.1

Structure	Silicon Monolithic Bipolar IC
Appearance	SIL-12 Pins Plastic Package (FP-12S Power Type With Fin)
Application	Audio
Function	70W (6Ω) x 1ch BTL Power Amplifier Built-in Standby and Muting Features Incorporating Various Protection Circuits

A	Absolute Maximum Ratings								
No.	Item	Symbol	Ratings	Unit	Note				
1	Storage Temperature	Tstg	-55 ~ +150	° C					
2	Operating Ambient Temperature	Topr	-25 ~ +75	° C					
3	Operating Ambient Pressure	Popr	$1.013 \text{x} 10^5 \pm 0.61 \text{x} 10^5$	Ра					
4	Operating Constant Acceleration	Gopr	9,810	m / s ²					
5	Operating Shock	Sopr	4,900	m / s ²					
6	Power Supply Voltage	Vcc	33	V	1				
7	Power Supply Current	Icc	8.0	А					
8	Power Dissipation	Pd	37.5	W	2				

Operating Supply Voltage Range	Vcc	10 V ~ 32V

Note: 1) Without input signal, Vcc is up to 33V 2) Ta = 75° C with infinite heatsink

 Eff. Date
 Eff. Date
 Eff. Date

 15-AUG-03

FMSC-PSDA-002-01 REV 1

Prepared	
Checked	
Approved	

Product Specifications AN17850A

В	Electrical Characteristics (Unless otherwise specified, the ambient temperature is $25^{\circ}C\pm 2^{\circ}C$, Vcc= $30V$, frequency= $1kHz$ and RL= 6Ω .)										
Na	T.	G 1 1	Test	Condition		Limit	TT	Nata			
No.	Item	Symbol	Cir- cuit.	Condition	Min	Тур	Max	Unit	Note		
1	Quiescent Circuit Current	Icq	1	No input ; Vstby = 5V Vmute = 5V;	-	100	300	mA			
2	Output Noise Voltage	Vno	1	No Input, $Rg=20k\Omega$ Vstby = 5V;Vmute = 5V	-	0.54	1	mVrms	1		
3	Voltage Gain	Gvc	1	Vin=20mV; Vstdby=5V Vmute = 5V	38	40	42	dB			
4	Total Harmonic Distortion	THD	1	Vin=20mV; Vstdby=5V Vmute = 5V;	-	0.07	0.4	%	2		
5	Maximum Output Power	Ро	1	THD_OUT=10% Vstdby=5V;Vmute= 5V;	55	70	-	W			
6	Output Offset Voltage	Voff	1	Rg=20kΩ; No input Vstdby=5V;Vmute=5V;	-350	0	350	mV			
7	Ripple Rejection	RR	1	Vripple=1Vrms * freq=120Hz, Rg=20kΩ	45	55	-	dB	1		
8	Standby Current	I _{STB}	1	No input ; vstdby=0V; Vmute=5V;	-	1	100	μΑ			
9	Muting Effects	MT	1	Vin=20mV; Vstby=5V; Vmute = 0 to 5V**	65	75	-	dB	2		

* The measurement is by taking the ratio of output voltage with reference to the Vripple. ** The measurement is by taking the ratio of output (at Vmute = 0 V) to the output(at Vmute = 5V)

Note : 1) With a filter band 20Hz ~20kHz (12 dB/OCT) used.

2) With a filter band 400Hz ~30kHz used.

Eff. Date	Eff. Date	Eff. Date	Eff. Date
15-AUG-03			

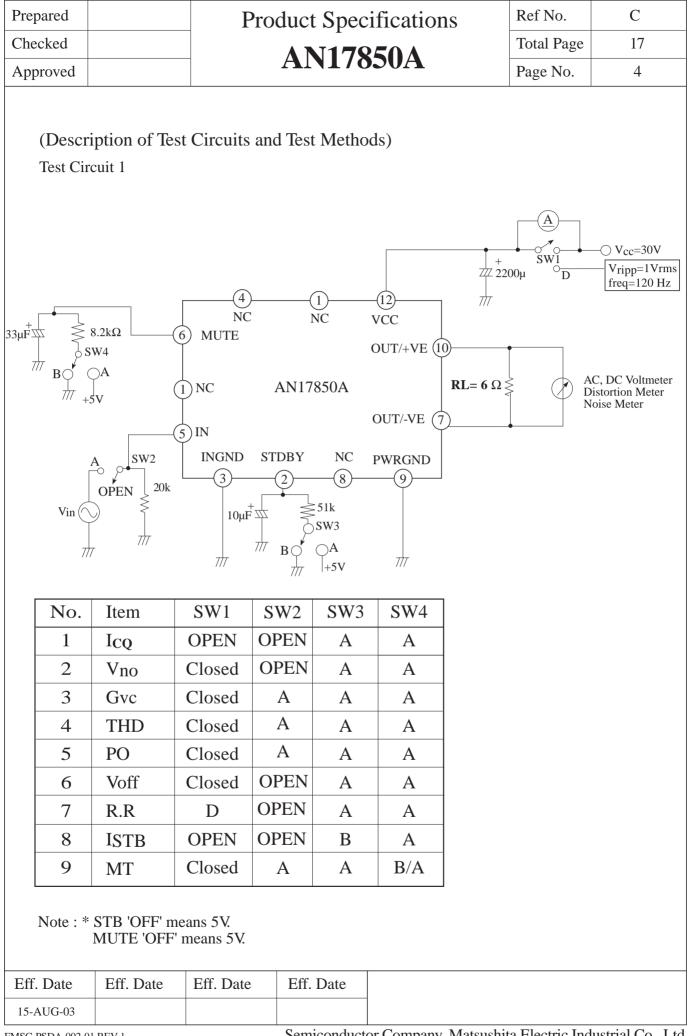
Prepared	
Checked	
Approved	

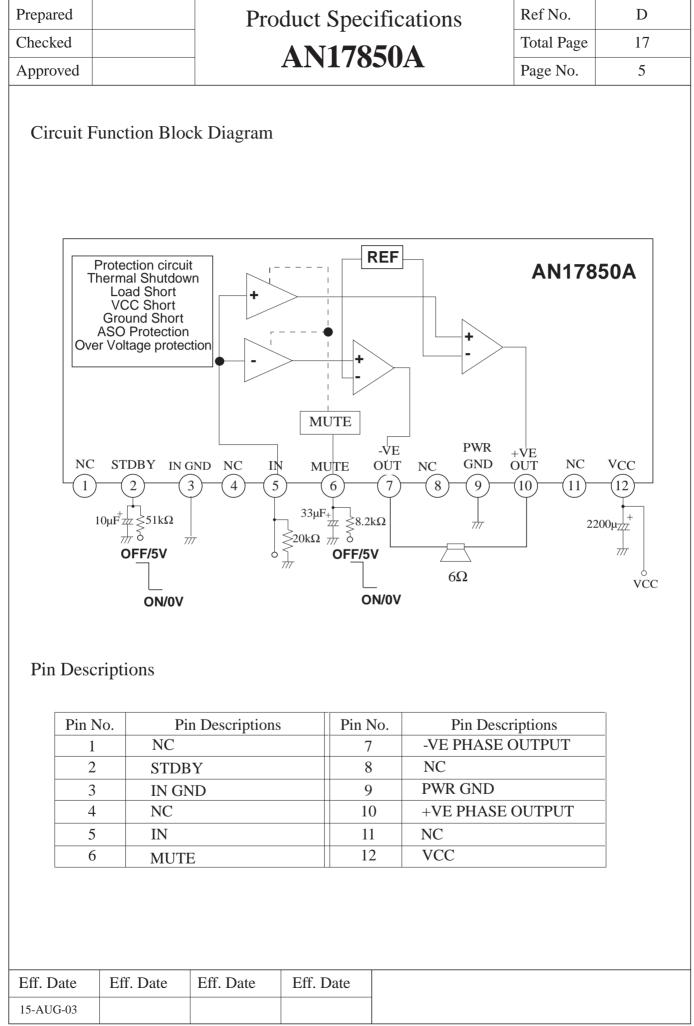
Ref No.	B-2
Total Page	17
Page No.	3

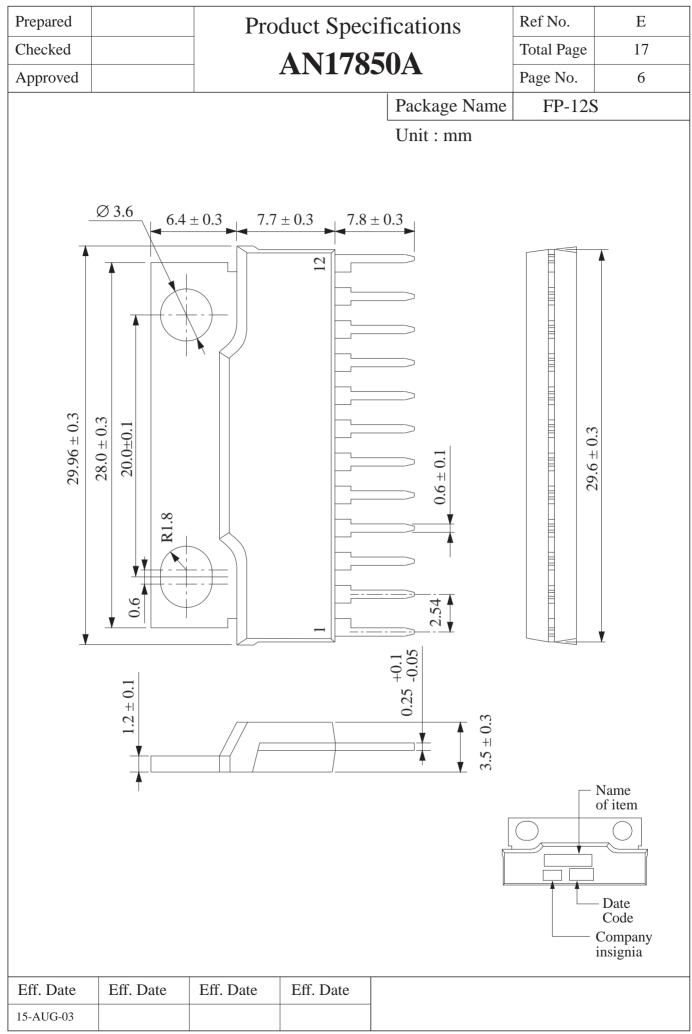
В	Electrical Characteristics (Unless otherwise specified, the ambient temperature is $25^{\circ}C\pm 2^{\circ}C$, Vcc= $30V$, frequency= $1kHz$ and RL= 6Ω .)									
No	Item	Symbol	Test	Conditions		Limits	5	Unit	Note	
	Itelli	Symbol	cuit			typ	max	Ullit	11010	
1	Standby on voltage	Vstdon	1	Vmute = 5V; Vin = $20mV$; Istb < $100uA$	-	-	1	V		
2	Standby off voltage	Vstd0ff	1	Vmute = 5V; Vin = 20mV; Gvc > 38 dB	4.5	-	-	V		
3	Mute on voltage	Vmon	1	VStdby = 5V; Vin = $20mV$; MT > 70 dB	-	-	1	V		
4	Mute off voltage	Vmoff	1	VStdby = 5V; Vin = 20mV; Gvc > 38 dB	4	-	-	V		

Note) The above characteristics are reference values determined for IC design, but not guaranteed values for shipping inspection. If problems were to occur, counter measures will be sincerely discussed.

Eff. Date	Eff. Date	Eff. Date	Eff. Date
15-AUG-03			





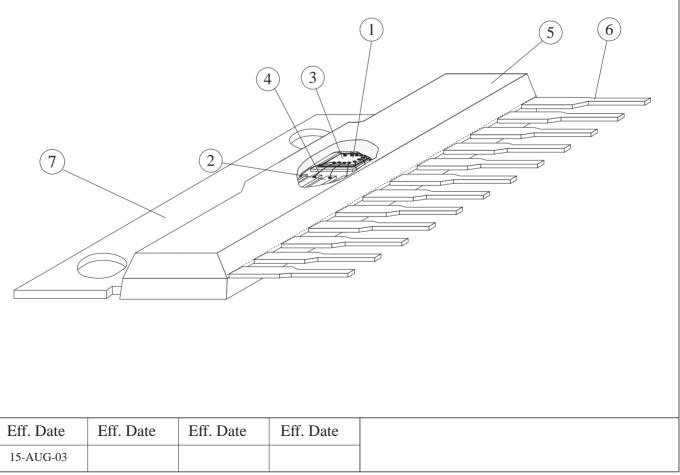


Prepared	Product Specifications	Ref No.	F
Checked	A NI17050 A	Total Page	17
Approved	AN17850A	Page No.	7

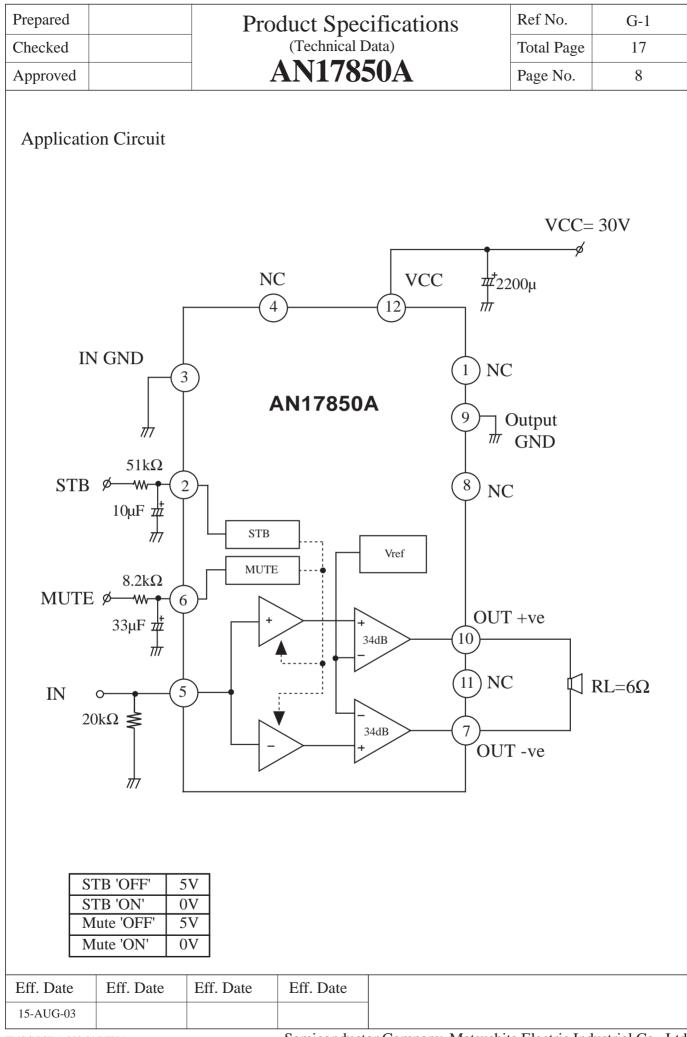
(Structure Description)

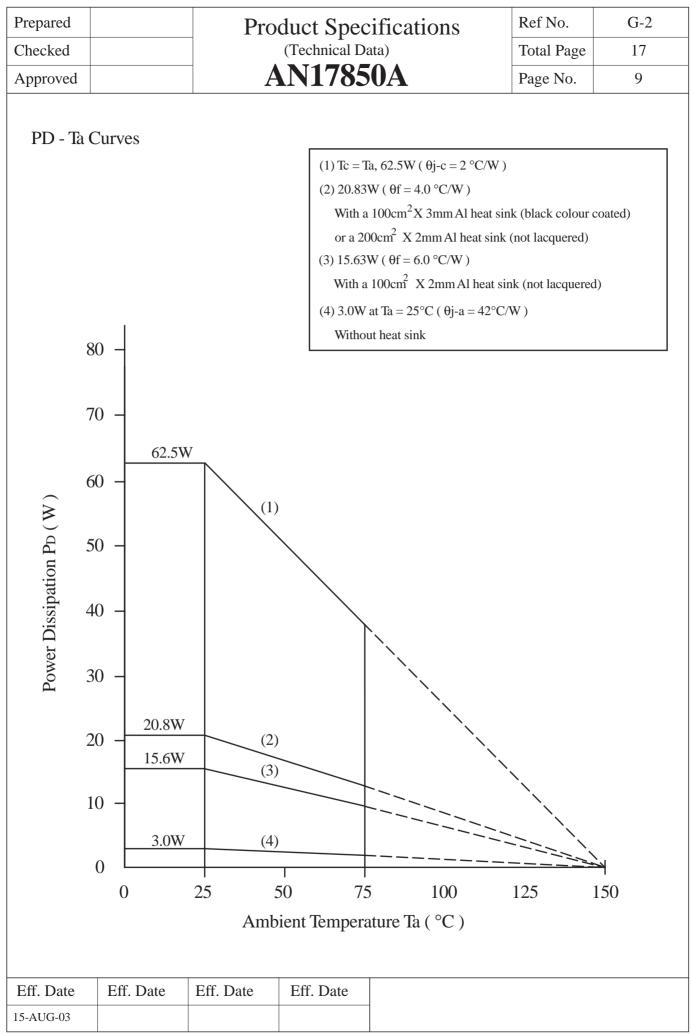
Chip surface passivation	SiN,	PSG,	Others ()	1
Lead frame material	Fe group,	Cu group,	Others ()	2,6
Inner lead surface process	Ag plating,	Au plating,	Others ()	2
Outer lead surface process	Solder plating,	Solder dip,	Others ()	6
Chip mounting method	Ag paste,	Au-Si alloy, Solder,	Others ()	3
Wire bonding method	Thermalsonic box	nding,	Others ()	4
Wire material	Au		Others ()	4
Mold material	Epoxy,		Others ()	5
Molding method	Transfer mold,	Multiplunger mold,	Others ()	5
Fin material	Cu Group		Others ()	(7)

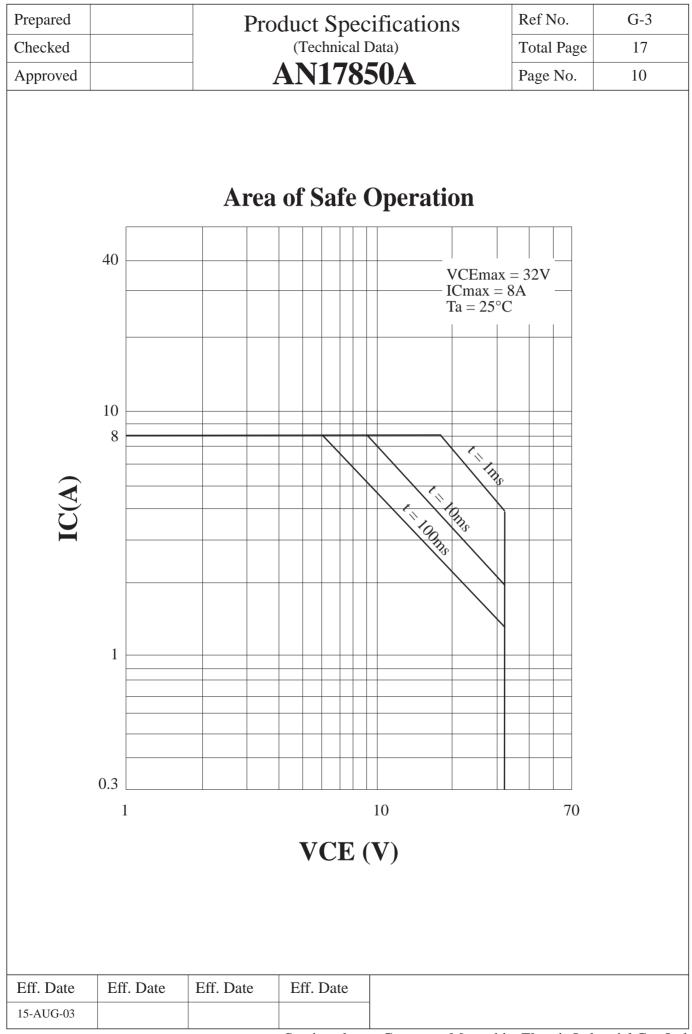
Package FP-12S

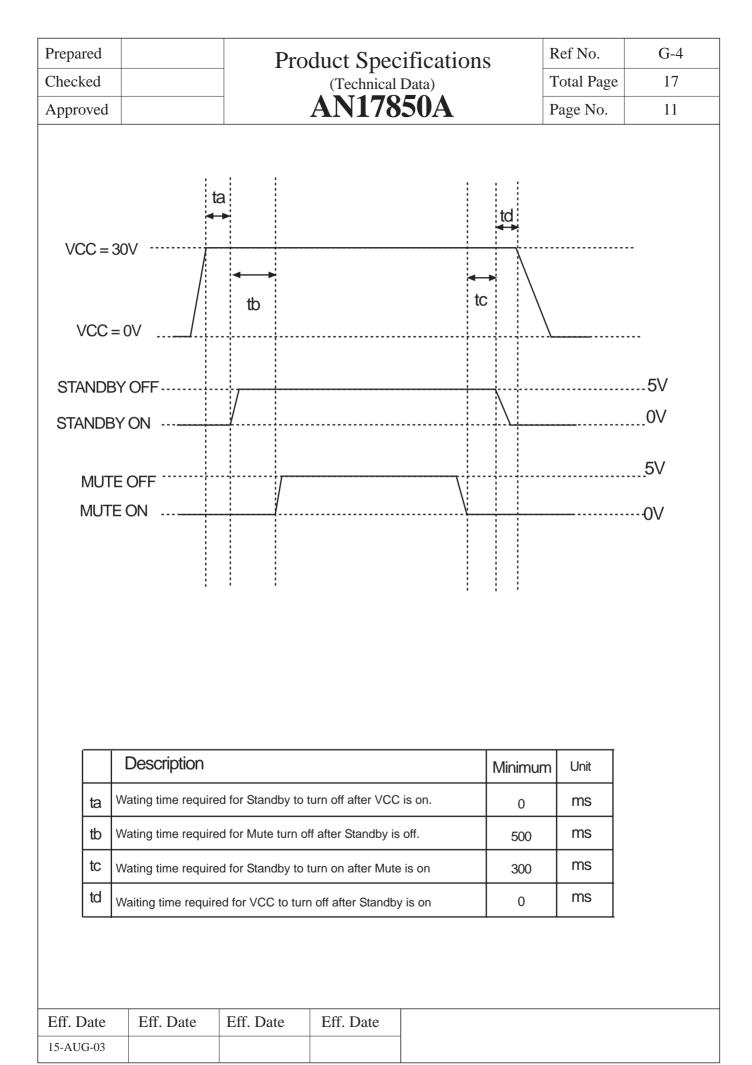


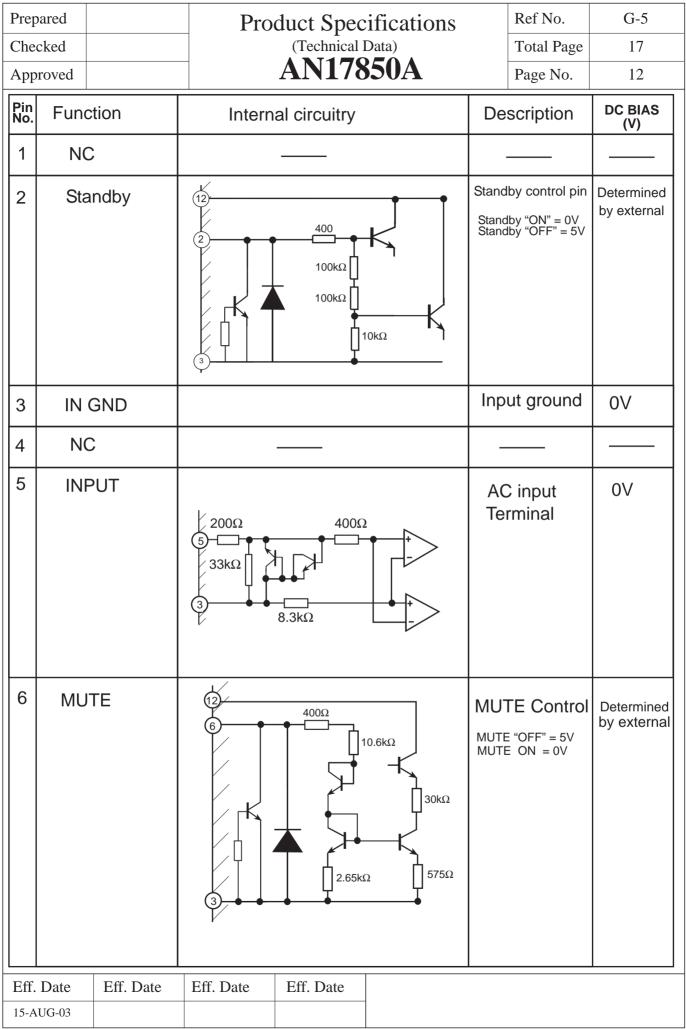
FMSC-PSDA-002-01 REV 1











Prepared		Pro	Product Specifications Ref No.					
Cheo	cked			(Technical	Data)		Total Page	17
App	roved			AN178	50A		Page No.	13
Pin No.	Func	tion	Intern	al circuitry		De	scription	DC BIAS (V)
7	Outp		Pre Amp 	Driver cct 15kΩ			jative output ninal	VCC/2
8	NC							
9	PWF	R GND				Out _i	out Power Ground	0V
10	Outpu		Pre Amp VCC/2 250Ω $10k\Omega$				itive output ninal	VCC/2
11	NC	C	-			_		
12	12 VCC					Pow Pin	er Supply	Typ 30V
	Date UG-03	Eff. Date	Eff. Date	Eff. Date				

Prepared		Pro	duct	Spec	ificatio	ons	Ref No.	G-6	
Checked			(Te	chnical	Data)	-	Total Page	17	
Approved			AN	178	50A		Page No.	14	
Power d	lissipation a	nd Heat Sir	nk		Га	Тс	TJ		
				HEA	T SINK	CASE	DIE]	
Definit	ion of term	S		L	θсΑ	→ ←	θјс	1	
Tj: Junc Tc: Cas TA: Amb θJC: The θCA: Th The follo	able and lon	ature ure rature ance of jund tance of cas quations rep c) / θJC = I ΓA) / θCA = g-term, cont	se to a preser PD PD' tinuou	to cas ambie nt the i (us ope	G1. Simp and F e nt, norm relations 1) 2) ration, ju	leat Sink at ally throug of these unction te	ration of IC ttached gh heat sin terms. mperature	should not	
in Equa	125 ^o C and tion 1. After e no heat los	specify the	Pd, T	c can	be dete	rmined.			
through	heat sink, w determine t	hich is quit	e true	. So F	D = PD'.	Since To	: is also kn	own,	
	ating of hea naximum op								
A more	general equ	uation can b	e use	ed for	ough ca	alculation.			
		$(T_J - T_A) / \theta_{JA} = \theta_{CA}$			(3) (4)				
Therefo	case, θJA is ore, for spec ng ambient t	ified power	dissip	pation,	either h	leat sink r	ating or ma	kage. aximum	
	Take note that it's essential to know PD value before hand in order to work out other quantities. PD calculation is as shown.								
	PD	= Vcc x lcc	: - Po	_total	(5)				
Icc: RI	C supply vo MS value of al: Total out	IC current							
Eff. Date	Eff. Date	Eff. Date	Eff. I	Date					
15-AUG-03									

Product Specifications	Ref No.	G-6
(Technical Data)	Total Page	17
AN17850A	Page No.	15
Input DC bi	ocina	
	AN17850A	(Technical Data) Total Page

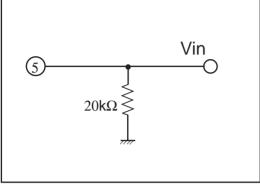


FIG2. Input DC Biasing

input DC biasing

Input DC bias is maintained at ground level. If the input signal contains DC bias voltage, AC coupling should be included on the application circuit.

The value of $20k\Omega$ resistor is set in order to achieve the minimum output DC offset.

Output Zobel Network

It should be noted that this device is designed such that the Zobel network (RC pair) at the output pins is not necessary for stable operation.

In practical application, the Zobel network may be applied optionally for two reasons:

a) Ensuring stability for different PCB layout and speaker types.

b) Ability to withstand to high ESD levels.

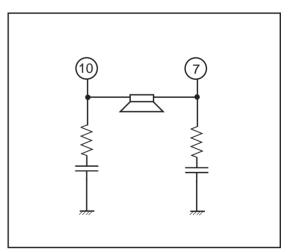
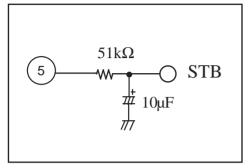


FIG3. Output Zobel Network

Eff. Date	Eff. Date	Eff. Date	Eff. Date
15-AUG-03			

FMSC-PSDA-002-01 REV 1

Prepared	Product Specifications	Ref No.	G-6
Checked	(Technical Data)	Total Page	17
Approved	AN17850A	Page No.	16



Standby operation

Standby pin should be connected with carefully selected components in order to avoid "Pop Noise" during Standby ON/OFF transient.

The 51k resistor and 10uF capacitor pair can delay the rising of voltage at pin 5 to reach the Standby threshold. When Standby is switching on together with supply, this delay would be very useful to ensure no "Pop Noise".

FIG4. Standby Application circuit

If the Standby voltage is provided by a microcontroller, the suppression of "Pop" could even be better.

For further details of timing and delay for standby circuit, please refer to page 11.

Mute operation

Mute pin should be connected with carefully selected components in order to avoid "Pop Noise" during MUTE ON/OFF transient.

The 8.2k resistor and 33uF capacitor pair can delay the rising of voltage at pin 6 to reach the Mute threshold. When Mute is switching on together with supply, this delay would be very useful to ensure no "Pop Noise".

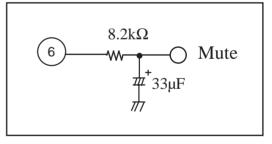


FIG5. Mute application circuit

For further details of timing and delay for Mute application circuit, please refer to page 11.

Eff. Date	Eff. Date	Eff. Date	Eff. Date
15-AUG-03			

Prepared	
Checked	
Approved	

(Precaution for use)

- 1) Ground the radiation fin so that there will be no difference in electric potential between the radiation fin and ground.
- 2) The thermal protection circuit operates at Tj at approximately 150°C. Thermal protection circuit is reset automatically when the temperature drops.
- 3) Be sure to attach heatsink to the IC before use. Make sure that the heatsink is secured to the chassis.
- 4) In order to prevent IC from being damaged during the fault test, prior to standby switching from on to off or vice versa, it is important to assert the mute on. Please refer to the timing diagram on page 11.

Eff. Date	Eff. Date	Eff. Date	Eff. Date				
15-AUG-03							