IR3527

DATA SHEET

XPHASE3™ DUAL PHASE IC

DESCRIPTION

The IR3527 Dual Phase IC combined with an IR *XPhase3*™ Control IC provides a full featured and flexible way to implement multiphase power solutions. The Control IC provides overall system control and interfaces with any number of IR3527 Phase ICs which each drive and monitor 2 phases of a Synchronous Buck converter.

The IR3527 implement an independent power savings function for each power stage and sequential phase timing for use in single output multiphase converters. When power saving mode is enabled, the power stage will disable its output thus eliminating its switching loss while proper converter operation is maintained by the single power stage or in conjunction with other converter power stages. The IR3527 current sense amplifiers remain active when in power savings to support adaptive voltage positioning.

FEATURES

- 7V/1.3A gate drivers (2.6A GATEL sink current)
- Converter output voltage up to 5.1 V (Limited to VCCL-1.4V)
- Loss-less inductor current sensing
- Feed-forward voltage mode control
- Integrated boot-strap synchronous PFET
- Self-calibration of PWM ramp, current sense amplifier, and current share amplifier
- Single-wire bidirectional average current sharing
- Only three external components per phase, plus common decoupling capacitors
- Power State Indicator (PSI) interface provides the capability to maximize the efficiency at light loads.
- Debugging function isolates phase from the converter
- Small thermally enhanced 24L 4 x 4mm MLPQ package
- RoHS compliant

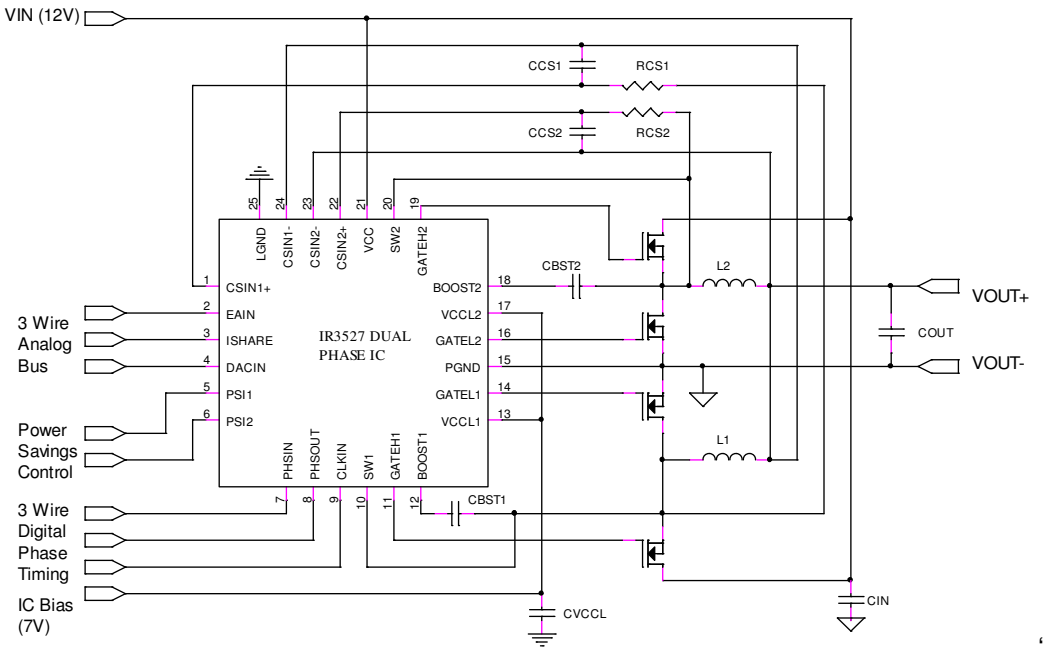


Figure 1 – IR3527 Application Circuit

ORDERING INFORMATION

Part Number	Package	Order Quantity
IR3527MTRPBF	24 Lead MLPQ (4 x 4 mm body)	3000 per reel
* IR3527MPBF	24 Lead MLPQ (4 x 4 mm body)	100 piece strips

* Samples only

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	CSIN1+	Phase1 current sense amplifier non-inverting input and input to debug comparator
2	EAIN	PWM comparator input from the error amplifier output of Control IC. Body Braking mode is initiated if the voltage on this pin is less than V(DACIN) threshold.
3	ISHARE	Output of the Current Sense Amplifiers are connected to this pin through 3kΩ resistors. Voltage on this pin is equal to approximately V(DACIN) + 16 [(V_{CSIN1+} – V_{CSIN1-}) + (V_{CSIN2+} – V_{CSIN2-})]. Connecting all Phase IC ISHARE pins together creates a share bus which provides an indication of the average current being supplied by all the phases. The signal is used by the Control IC for voltage positioning, over-current protection, and in some cases current reporting. OVP mode is initiated if the voltage on this pin rises above V(VCCL)- 0.8V.
4	DACIN	Reference voltage input from the Control IC. The Current Sense signal and PWM ramps are referenced to the voltage on this pin.
5	PSI1	Input to Phase 1 PSI comparator. Logic low stops the phase from switching (low = low power state)
6	PSI2	Input to Phase 2 PSI comparator. Logic low stops the phase from switching (low = low power state)
7	PHSIN	Phase timing clock input.
8	PHSOUT	Phase timing clock output.
9	CLKIN	Clock input.
10	SW1	Return for Phase1 high-side driver and reference for GATEL1 non-overlap comparator.
11	GATEH1	Phase1 High-side driver output and input to GATEL1 non-overlap comparator.
12	BOOST1	Supply for Phase1 high-side driver. Internal bootstrap synchronous PFET is connected between this pin and the VCCL1 pin.
13	VCCL1	Supply for Phase1 low-side driver. Internal bootstrap synchronous PFET is connected from this pin to the BOOST1 pin.
14	GATEL1	Phase1 Low-side driver output and input to GATEH1 non-overlap comparator.
15	PGND	Return for low side drivers and reference for GATEH non-overlap comparators.
16	GATEL2	Phase2 Low-side driver output and input to GATEH2 non-overlap comparator.
17	VCCL2	Supply for Phase2 low-side driver. Internal bootstrap synchronous PFET is connected from this pin to the BOOST pin.
18	BOOST2	Supply for Phase2 high-side driver. Internal bootstrap synchronous PFET is connected between this pin and the VCCL1 pin.

19	GATEH2	Phase2 High-side driver output and input to GATEL2 non-overlap comparator.
20	SW2	Return for Phase2 high-side driver and reference for GATEL2 non-overlap comparator.
21	VCC	Supply for internal IC circuits. Input to PWM feed-forward.
22	CSIN2+	Phase2 current sense amplifier non-inverting input and input to debug comparator
23	CSIN2-	Phase2 current sense amplifier inverting input
24	CSIN1-	Phase1 current sense amplifier inverting input
25	LGND	Ground for internal IC circuits. IC substrate is connected to this pin.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed below may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. All voltages are absolute voltages referenced to the LGND pin.

Operating Junction Temperature…….. 0 to 150°C
Storage Temperature Range……..-65°C to 150°C
MSL Rating……2
Reflow Temperature…….260°C

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	CSIN1+	8V	-0.3V	1mA	1mA
2	EAIN	8V	-0.3V	1mA	1mA
3	ISHARE	8V	-0.3V	1mA	1mA
4	DACIN	3.3V	-0.3V	1mA	1mA
5	PSI1	8V	-0.3V	1mA	1mA
6	PSI2	8V	-0.3V	1mA	1mA
7	PHSIN	8V	-0.3V	1mA	1mA
8	PHSOUT	8V	-0.3V	2mA	2mA
9	CLKIN	8V	-0.3V	1mA	1mA
10	SW1	34V	-0.3V DC, -5V for 100ns	3A for 100ns, 100mA DC	n/a
11	GATEH1	40V	-0.3V DC, -5V for 100ns	3A for 100ns, 100mA DC	3A for 100ns, 100mA DC
12	BOOST1	40V	-0.3V	1A for 100ns, 100mA DC	3A for 100ns, 100mA DC
13	VCCL1	8V	-0.3V	n/a	5A for 100ns, 200mA DC
14	GATEL1	8V	-0.3V DC, -5V for 100ns	5A for 100ns, 200mA DC	5A for 100ns, 200mA DC
15	PGND	0.3V	-0.3V	5A for 100ns, 200mA DC	n/a
16	GATEL2	8V	-0.3V DC, -5V for 100ns	5A for 100ns, 200mA DC	5A for 100ns, 200mA DC
17	VCCL2	8V	-0.3V	n/a	5A for 100ns, 200mA DC
18	BOOST2	40V	-0.3V	1A for 100ns, 100mA DC	3A for 100ns, 100mA DC

19	GATEH2	40V	-0.3V DC, -5V for 100ns	3A for 100ns, 100mA DC	3A for 100ns, 100mA DC
20	SW2	34V	-0.3V DC, -5V for 100ns	3A for 100ns, 100mA DC	n/a
21	VCC	34V	-0.3V	n/a	20mA
22	CSIN2+	8V	-0.3V	1mA	1mA
23	CSIN2-	8V	-0.3V	1mA	1mA
24	CSIN1-	8V	-0.3V	1mA	1mA
25	LGND	n/a	n/a	n/a	n/a

Note:
1. Maximum GATEHx – SWx = 8V
2. Maximum BOOSTx – GATEHx = 8V

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

$8.0V \le V_{CC} \le 28V$, $4.75V \le V_{CCL} \le 7.5V$, $0\,^{o}C \le T_J \le 125\,^{o}C$

ELECTRICAL CHARACTERISTICS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C. 0.5V ≤ V(DACIN) ≤ 1.6V, 500kHz ≤ CLKIN ≤ 9MHz, 250kHz ≤ PHSIN ≤1.5MHz, C_{GATEH} = 3.3nF, C_{GATEL} = 6.8nF (unless otherwise specified).

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Gate Drivers					
GATEHx Source Resistance	BOOSTx – SWx = 7V. Note 1		1.3	3.3	Ω
GATEHx Sink Resistance	BOOSTx – SWx = 7V. Note 1		1.3	3.3	Ω
GATELx Source Resistance	VCCLx – PGND = 7V. Note 1		1.3	3.3	Ω
GATELx Sink Resistance	VCCLx – PGND = 7V. Note 1		0.5	1.3	Ω
GATEHx Source Current	BOOSTx=7V, GATEHx=2.5V, SW=0V. Note 1		1.3		A
GATEHx Sink Current	BOOSTx=7V, GATEHx=2.5V, SWx=0V. Note 1		1.3		A
GATELx Source Current	VCCLx=7V, GATELx=2.5V, PGND=0V. Note 1		1.3		A
GATELx Sink Current	VCCLx=7V, GATELx=2.5V, PGND=0V. Note 1		2.6		A
GATEHx Rise Time	BOOSTx – SWx = 7V, measure 1V to 4V transition time		6	13	ns
GATEHx Fall Time	BOOSTx - SWx = 7V, measure 4V to 1V transition time		6	13	ns
GATELx Rise Time	VCCLx – PGND = 7V, Measure 1V to 4V transition time		12	26	ns
GATELx Fall Time	VCCLx – PGND = 7V, Measure 4V to 1V transition time		6	13	ns

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
GATELx low to GATEHx high delay	BOOSTx = VCCLx = 7V, SWx = PGND = 0V, measure time from GATELx falling to 1V to GATEHx rising to 1V	10	20	40	ns
GATEHx low to GATELx high delay	BOOSTx = VCCLx = 7V, SWx = PGND = 0V, measure time from GATEHx falling to 1V to GATELx rising to 1V	10	20	40	ns
Disable Pull-Down Resistance	Note 1	30	80	130	kΩ
Clock & Daisy Chain					
CLKIN Threshold	Compare to V(VCCLx)	40	45	57	%
CLKIN Bias Current	CLKIN = V(VCCLx)	-0.5	0.0	0.5	µA
CLKIN Phase Delay	Measure time from CLKIN<1V to GATEHx>1V	40	75	125	ns
PHSIN Threshold	Compare to V(VCCLx)	35	50	55	%
PHSOUT Propagation Delay	Measure time from CLKIN > (VCCLx*50%) to PHSOUT>(VCCLx*50%). 10pF@125°C	4	15	35	ns
PHSIN Pull-Down Resistance		30	100	170	kΩ
PHSOUT High Voltage	I(PHSOUT) = -5mA, measure VCCLx – PHSOUT	2	0.6		V
PHSOUT Low Voltage	I(PHSOUT) = 5mA		0.4	2	V
PWM Comparators					
PWM Ramp Slope	Vin=12V	42	52.5	57	mV/ %DC
EAIN Bias Current	0 ≤ EAIN ≤ 3V	-5	-0.3	5	µA
Minimum Pulse Width	Note 1		65	75	ns
Minimum GATEHx Turn-off Time		20	80	160	ns
OVP Comparator					
OVP Threshold	Step V(ISHARE) up until GATELx drives high. Compare to V(VCCLx)	-1.0	-0.8	-0.4	V
Propagation Delay	V(VCCLx)=5V, Step V(ISHARE) up from V(DACIN) to V(VCCLx). Measure time to V(GATELx)>4V.	15	40	70	ns
Body Brake Comparator					
Threshold Voltage with EAIN falling.	Measured relative to PWM Ramp Floor Voltage	-340	-235	-130	mV
Threshold Voltage with EAIN rising.	Measured relative to PWM Ramp Floor Voltage	-240	-135	-30	mV
Hysteresis		70	105	130	mV
Propagation Delay	VCCLx = 5V. Measure time from EAIN < V(DACIN) (200mV overdrive) to GATELx transition to < 4V.	40	65	90	ns

Current Sense Amplifiers					
CSINx+/- Bias Current		-200	0	200	nA
CSINx+/- Bias Current Mismatch	Note 1	-50	0	50	nA
Input Offset Voltage	CSINx+ = CSINx- = DACIN. Measure input referred offset from DACIN	-1		1	mV
Gain	0.5V ≤ V(DACIN) < 1.6V	30	32.5	35	V/V
Unity Gain Bandwidth	C(ISHARE)=10pF. Measure at ISHARE. Note 1	4.8	6.8	8.8	MHz
Slew Rate	Note 1		6		V/µs
Differential Input Range	0.8V ≤ V(DACIN) ≤ 1.6V, Note 1	-10		50	mV
Differential Input Range	0.5V ≤ V(DACIN) < 0.8V, Note 1	-5		50	mV
Common Mode Input Range	Note 1	0		Note2	V
Rout at T_J = 25°C	Note 1	2.3	3.0	3.7	kΩ
Rout at T_J = 125°C		3.6	4.7	5.4	kΩ
ISHARE Source Current		.5	1.7	2.9	mA
ISHARE Sink Current		.5	1.7	2.9	mA
Share Adjust Amplifiers					
Input Offset Voltage	Note 1	-3	0	3	mV
Gain	CSINx+ = CSINx- = DACIN.	3.6	4.7	5.8	V/V
Unity Gain Bandwidth	Note 1	4	8.5	17	kHz
PWM Ramp Floor Voltage	ISHARE unconnected Measured Relative to DACIN	-116	0	+116	mV
Maximum PWM Ramp Floor Voltage	ISHARE = DACIN - 200mV Measured relative to FLOOR with ISHARE unconnected	120	180	240	mV
Minimum PWM Ramp Floor Voltage	ISHARE = DACIN + 200mV Measured relative to FLOOR with ISHARE unconnected	-220	-160	-100	mV
Synchronous Rectification Disable Comparators					
Threshold Voltage	The ratio of V(CSINx-) / V(DACIN), below which V(GATELx) is always low.	66	75	86	%
Negative Current Comparators					
Input Offset Voltage	Note 1	-16	0	16	mV
Propagation Delay Time	Apply step voltage to V(CSINx+) – V(CSINx-). Measure time to V(GATELx)< 1V.	100	200	400	ns
Bootstrap Diodes					
Forward Voltage	I(BOOSTx) = 30mA, VCCL=6.5V	360	520	960	mV
Debug Comparators					
Threshold Voltage	Compare to V(VCCLx)	-250	-150	-50	mV

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
PSI Comparator					
Rising Threshold Voltage		520	620	700	mV
Falling Threshold Voltage		400	550	650	mV
Hysteresis		50	70	120	mV
Resistance		200	500	850	kΩ
Floating Voltage		800		1150	mV
General					
VCC Supply Current	8V≤V(VCC)≤10V	2.2	8.0	12.2	mA
VCC Supply Current	10V≤V(VCC)≤16V	2.2	4.0	8.0	mA
VCCLx Supply Current		3.1	8.0	12.1	mA
BOOSTx Supply Current	4.75V ≤ V(BOOSTx)-V(SWX) ≤ 8V	0.5	1.5	3	mA
DACIN Bias Current		-3.0	-1.5	1	μA
SW Floating Voltage		0.1	0.3	0.4	V

Note 1: Guaranteed by design, but not tested in production
Note 2: VCCL-0.5V or VCC – 2.5V, whichever is lower

SYSTEM THEORY OF OPERATION

PWM Control Method

The PWM block diagram of the *XPhase3*™ architecture is shown in Figure 2. Feed-forward voltage mode control with trailing edge modulation is used. A high-gain and wide-bandwidth voltage type error amplifier is used for the voltage control loop. Input voltage is sensed by phase to monitor any changes in amplitude. The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to the wire and PCB-trace voltage drop related to changes in load current.

Frequency and Phase Timing Control

The oscillator is located in the Control IC and the system clock frequency is programmable from 250 kHz to 9 MHZ by an external resistor. The control IC system clock signal (CLKOUT) is connected to CLKIN of all the phase ICs. The phase timing of the phase ICs is controlled by the daisy chain loop, where control IC phase clock output (PHSOUT) is connected to the phase clock input (PHSIN) of the first phase IC, and PHSOUT of the first phase IC is connected to PHSIN of the second phase IC, etc. and PHSOUT of the last phase IC is connected back to PHSIN of the control IC.

The switching frequency is set by the Control IC. The clock frequency equals the total number of phases multiplied by the switching frequency. During power up, the control IC sends out clock signals from both CLKOUT and PHSOUT pins and detects the feedback at PHSIN pin to determine the phase number and monitor any fault in the daisy chain loop.

The IR3527 combines 2 Phase ICs in a single package. IR3527 internally connect the PHSOUT1 pin to the PHSIN2 so the firing order is always sequential. Figure 3 shows the phase timing for a four phase converter implemented by two IR3527 Phase ICs. The dotted lines indicate the PHSOUT1 to PHSIN2 waveform that would be internal to the IR3527.

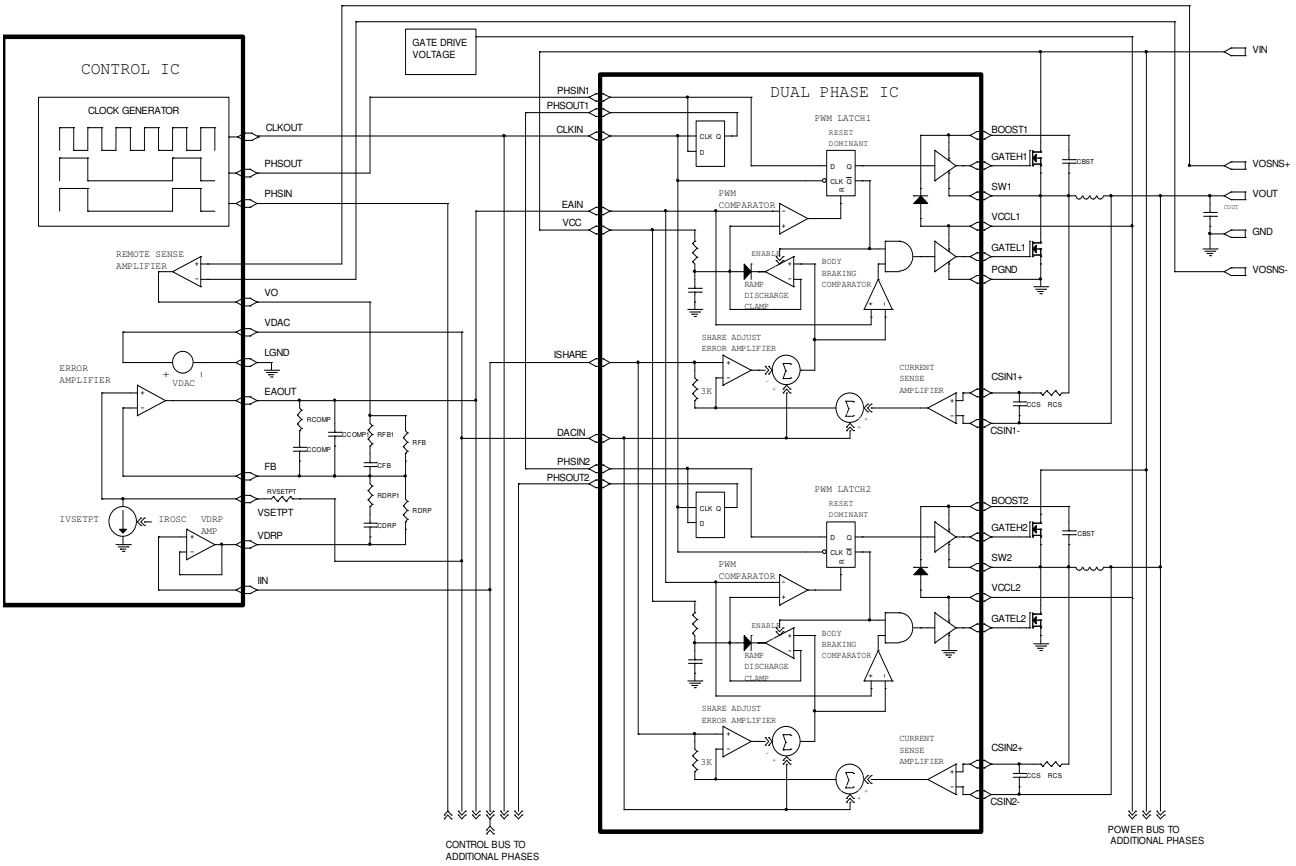


Figure 2 - PWM Block Diagram

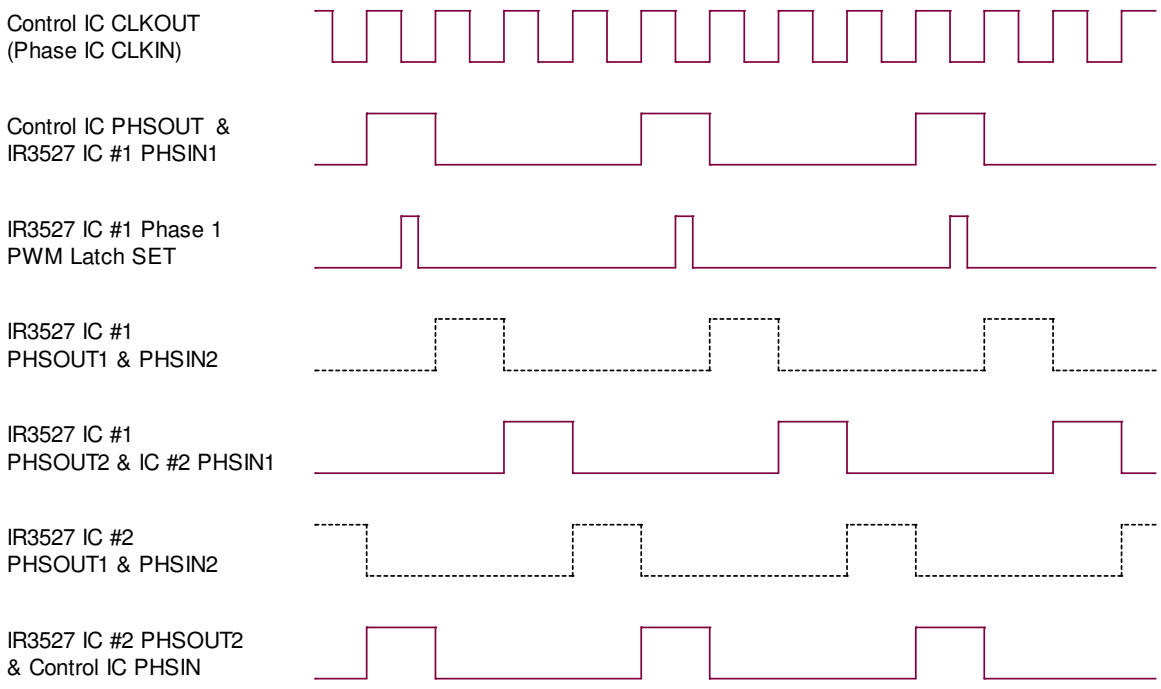


Figure 3 - Four Phase Oscillator Waveforms implemented with two IR3527

PWM Operation

The PWM comparator is located in the phase IC. Upon receiving the falling edge of a clock pulse, the PWM latch is sets and the PWM ramp voltage begins to increase. In conjunction, the low side driver is turned off and the high side driver is turned on after the non-overlap time expires. When the PWM ramp voltage exceeds the error amplifier's output voltage, the PWM latch is reset. This turns off the high side driver, turns on the low side driver after the non-overlap time, and activates the ramp discharge clamp. The clamp drives the PWM ramp voltage to the level set by the share adjust amplifier until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go to a 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An error amplifier output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the error amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients. An additional advantage of this PWM modulator is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC.

Figure 4 depicts PWM operating waveforms under various conditions.

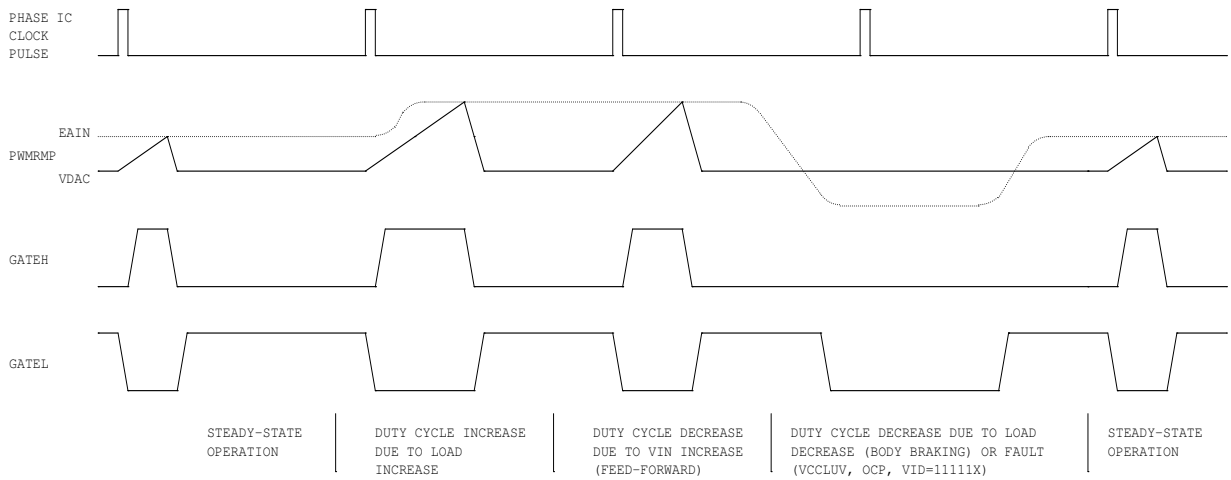


Figure 4 - PWM Operating Waveforms

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODYDIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O + V_{BODYDIODE}}$$

Since the voltage drop in the body diode is often comparable to the output voltage, the inductor current slew rate can be increased significantly. This patented technique is referred to as “body braking” and is accomplished through the “body braking comparator” located in the phase IC. If the error amplifier’s output voltage drops below the output voltage of the share adjust amplifier in the phase IC, this comparator turns off the low side gate driver.

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 5. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)\frac{R_L+sL}{1+sR_{CS}C_{CS}}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR (R_L). If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

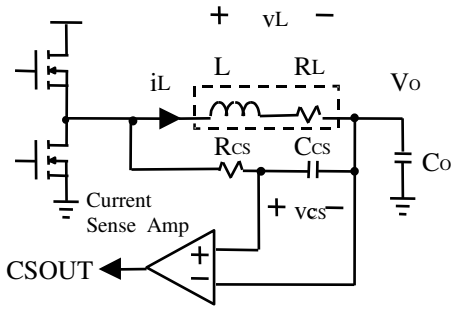


Figure 5 - Inductor Current Sensing and Current Sense Amplifier

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is located in the phase IC, as shown in Figure 5. Its gain is nominally 32.5 and the 3850 ppm/ºC increase in inductor DCR should be compensated in the voltage loop feedback path.

The current sense amplifier can accept positive differential input up to 50mV and negative up to -10mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the control IC and other phases through an on-chip 3KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the average current through all the inductors and is used

by the control IC for voltage positioning and current limit protection. The input offset of this amplifier is calibrated to +/- 1mV in order to reduce the current sense error.

The input offset voltage is the primary source of error for the current share loop. In order to achieve very small input offset error and superior current sharing performance, the current sense amplifier continuously calibrates itself. This calibration algorithm creates ripple on ISHARE bus with a frequency of $f_{sw}/(32*28)$ in a multiphase architecture.

Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each phase IC. The output of the current sense amplifier is compared with the average current at the share bus. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will pull down the starting point of the PWM ramp thereby increasing its duty cycle and output current; if current in a phase is larger than the average current, the share adjust amplifier of the phase will pull up the starting point of the PWM ramp thereby decreasing its duty cycle and output current. The current share amplifier is internally compensated so that the crossover frequency of the current share loop is much slower than that of the voltage loop and the two loops do not interact.

IR3527 THEORY OF OPERATION

Block Diagram

A detailed IR3527 block diagram is enclosed (Figure 6) to help clearly illustrate the following theory of operation.

Tri-State Gate Drivers

The gate drivers can deliver up to 1.3A peak current (2.6A sink current for bottom driver). An adaptive non-overlap circuit monitors the voltage on the GATEH and GATEL pins to prevent MOSFET shoot-through current while minimizing body diode conduction. The non-overlap latch is added to eliminate the error triggering caused by the switching noise. An enable signal is provided by the control IC to the phase IC without the addition of a dedicated signal line. The error amplifier output of the control IC drives low in response to any fault condition such as VCCL under voltage or output overload. The IR3527 Body Braking™ comparator detects this and drives both gate outputs low. This tri-state operation prevents negative inductor current and negative output voltage during power-down.

A synchronous rectification disable comparator is used to detect converter CSIN- pin voltage, which represents local converter output voltage. If the voltage is below 75% of VDAC and negative current is detected, GATEL drives low, which disables synchronous rectification and eliminates negative current during power-up.

The gate drivers pull low if the supply voltages are below the normal operating range. An 80kΩ resistor is connected across the GATEH/GATEL and PGND pins to prevent the GATEH/GATEL voltage from rising due to leakage or other causes under these conditions.

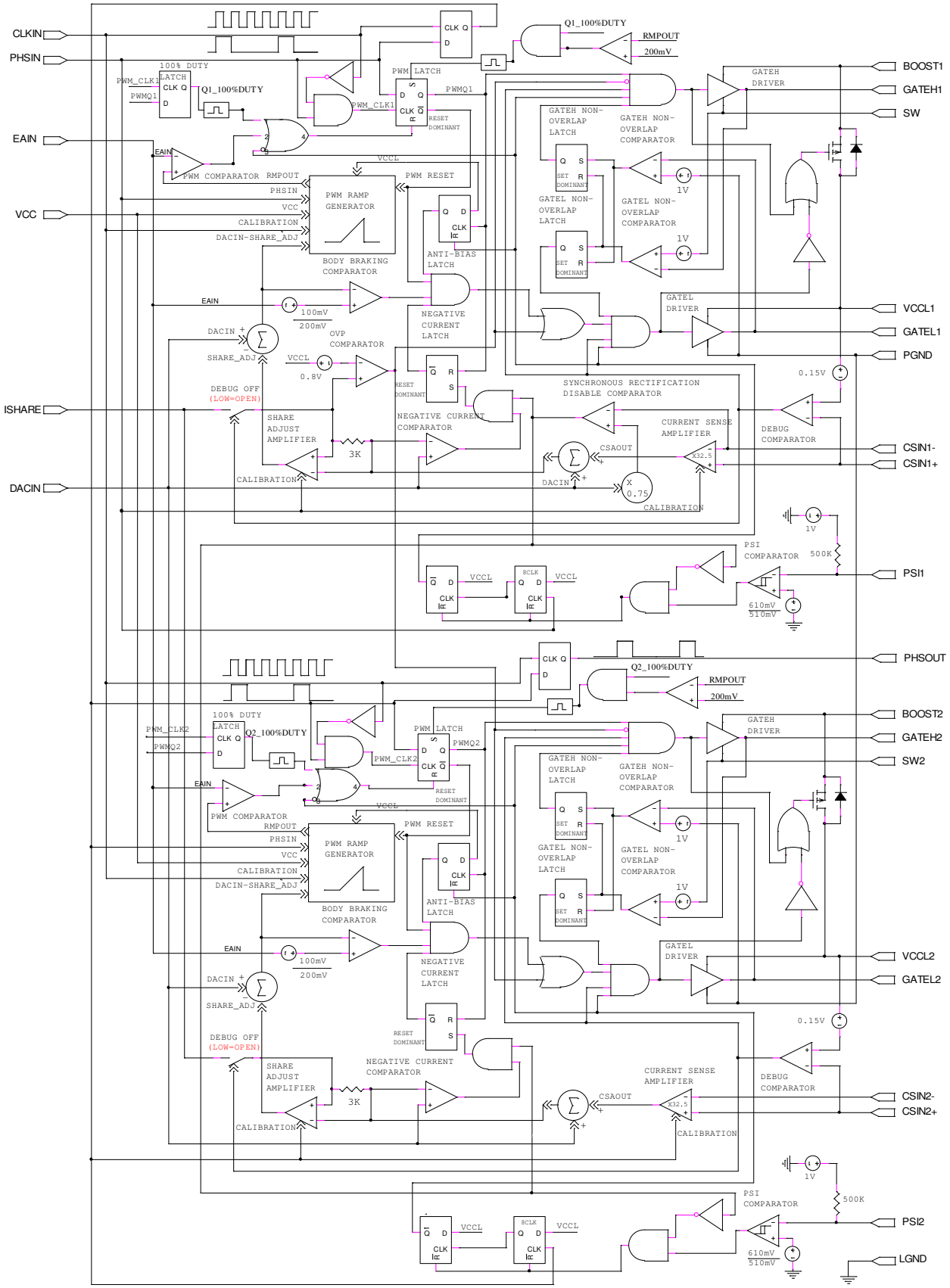


Figure 6 – IR3527 Block diagram

Over Voltage Protection (OVP)

The IR3527 includes over-voltage protection that turns on the low side MOSFET to protect the load in the event of a shorted high-side MOSFET, converter out of regulation, or connection of the converter output to an excessive output voltage. As shown in Figure 7, if ISHARE pin voltage is above V(VCCL) – 0.8V, which represents over-voltage condition detected by control IC, the over-voltage latch is set. GATEL drives high and GATEH drives low. The OVP circuit overrides the normal PWM operation and within approximately 150ns will fully turn-on the low side MOSFET, which remains ON until ISHARE drops below V(VCCL) – 0.8V when over voltage ends. The over voltage fault is latched in control IC and can only be reset by cycling the power to control IC. The error amplifier output (EAIN) is pulled down by control IC and will remain low. The lower MOSFETs alone can not clamp the output voltage however an SCR or N-MOSFET could be triggered with the OVP output to prevent load damage.

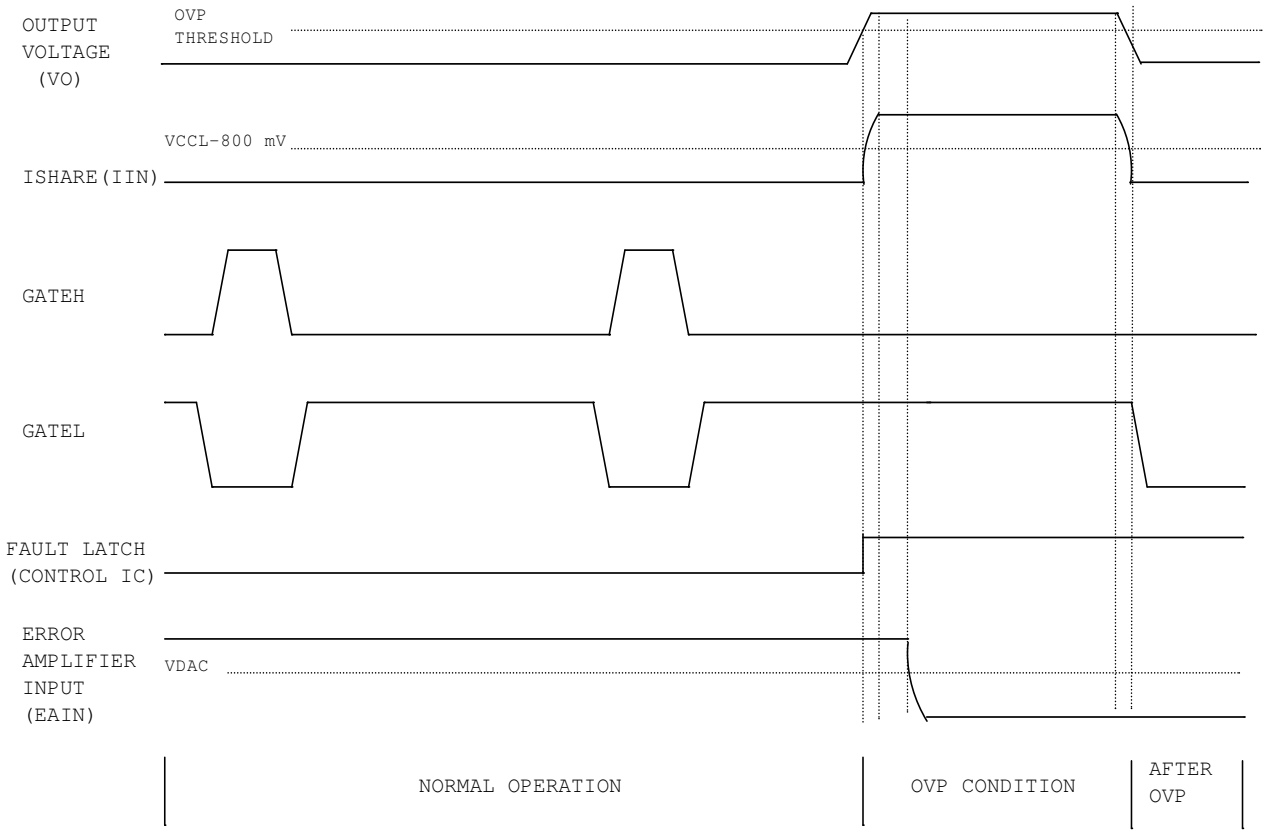


Figure 7 - Over-voltage protection waveforms

PWM Ramp

Every time the phase IC is powered up PWM ramp magnitude is calibrated to generate a 52.5 mV/%DC (typical) ramp for a VCC=12V. For example, for a 15% duty ratio the ramp amplitude is 787.5mV for VCC=12V. Feed-forward control is achieved because the PWM ramp varies with VCC voltage proportionally after calibration.

Debugging Mode

If CSIN+ pin is pulled up to VCCL voltage, IR3527 enters into debugging mode. Both drivers are pulled low and ISHARE output is disconnected from the current share bus, which isolates this phase IC from other phases. However, the phase timing from PHSIN to PHSOUT does not change.

Emulated Bootstrap Diode

IR3527 integrates a PFET to emulate the bootstrap diode. An external bootstrap diode connected from VCCL pin to BOOST pin can be added to reduce the drop across the PFET but is not needed in most applications.

PSI Mode

In order to increases the efficiency under light load condition, the IR3527 employs a power state indicator (PSI) signal to switch off the phase IC at light load. An active low on the PSI indicates the low power state and can be used to switch off the phase IC. Once the PSI signal is asserted, the IR3527 waits for 8 PHSIN cycles to disable the gate drives. When the PSI signal is de-asserted again the anti-bias latch circuit ensures that the topFET is switched on first. The maximum de-assert delay is determined by the CLKIN period.

Operation at Higher Output Voltage

The proper operation of the phase IC is ensured for output voltage up to 5.1V. Similarly, the minimum VCC for proper operation of the phase IC is 8 V. If the condition [$V_{CCL} \geq V_{DACIN} + 35(V_{CSIN+x} - V_{CSIN-x}) + 1.4V$] is violated, the current sharing performance of the phase IC is affected.

APPLICATIONS INFORMATION

IR3527 EXTERNAL COMPONENTS

Inductor Current Sensing Capacitor *CCS* and Resistor *RCS*

The DC resistance of the inductor is utilized to sense the inductor current. Usually the resistor RCS and capacitor CCS in parallel with the inductor are chosen to match the time constant of the inductor, and therefore the voltage across the capacitor CCS represents the inductor current. If the two time constants are not the same, the AC component of the capacitor voltage is different from that of the real inductor current. The time constant mismatch does not affect the average current sharing among the multiple phases, but does affect the current signal ISHARE as well as the output voltage during the load current transient if adaptive voltage positioning is adopted.

Measure the inductance L and the inductor DC resistance RL. Pre-select the capacitor CCS and calculate RCS as follows.

$$R_{CS} = \frac{L/R_L}{C_{CS}} \qquad (1)$$

Bootstrap Capacitor *CBST*

Depending on the duty cycle and gate drive current of the phase IC, a capacitor in the range of 0.1uF to 1uF is needed for the bootstrap circuit.

Decoupling Capacitors for Phase IC

A 0.1uF-1uF decoupling capacitor is required at the VCCL pin.

CURRENT SHARE LOOP COMPENSATION

The internal compensation of current share loop ensures that crossover frequency of the current share loop is at least one decade lower than that of the voltage loop so that the interaction between the two loops is eliminated. The crossover frequency of current share loop is approximately 8 kHz.

IC Die Temperature

To ensure proper operation, the IC die should never operate at or above 150°C. For the vast majority of applications, the IR3527 dual phase IC will not require any type of heat sink to achieve temperatures well below 150°C. The IR3527 die is housed in a 24 lead MLPQ with exposed pad (Epad) which will provide excellent thermal conduction. By soldering the Epad to a minimal copper area of 1"x 1", the internal die temperature will rise at a rate of approximately 30.5°C/W (θ_{JA}).

The die temperature can be derived by first calculating the power dissipation of the phase IC. The IC has two types of conduction losses: quiescent current and driver losses. The quiescent losses are made up of VCC, VCCL, and boost (V_{BST}) supplies, while driving the top and bottom FETs contribute to the second loss.

The IC quiescent power losses can be calculated by the following equations:
$Pvccl = 2(Vccl \times Ivccl)$, $Pvcc = Vcc \times Ivcc$, and $Pbst = 2(Vbst \times Ibst)$. *Ivccl, Ivcc,* and *Ibst* are the input supplies quiescent currents which are listed in the Electrical Specifications Table. Driver power losses (P_{TOP} *and* P_{BOT}) are equal to Q_G x V_G x *Fo*, where Q_G is the FET's gate charge, V_G is the gate voltage, and *Fo* is the operational frequency. Both top and bottom FET power losses needs to be calculated and doubled to account for both internal drivers. Hence, the total phase IC power loss (P_{TOTAL}) is: $P_{VCCL} + P_{VCC} + P_{BST} + 2(P_{TOP}) + 2(P_{BOT})$.

The die temperature can now be calculated with the following formula:

$$T_{DIE} = (\theta_{JA} \times P_{TOTAL}) + T_A,$$

Where, T_A is the ambient temperature and θ_{JA} is the junction to air thermal impedance of the 24 pin MLPQ package.

LAYOUT GUIDELINES

The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout; therefore, minimizing the noise coupled to the IC.

- Separate analog bus (EAIN, DACIN, and IOUT) from digital bus (CLKIN, PSI, PHSIN, and PHSOUT) to reduce the noise coupling.
- Place current sense resistors and capacitors (R_{CS} and C_{CS}) close to phase IC. Use Kelvin connection for the inductor current sense wires, but separate the two wires by ground polygon. The wire from the inductor terminal to CSIN- should not cross over the fast transition nodes, i.e., switching nodes, gate drive outputs, and bootstrap nodes.
- Place the decoupling capacitors C_{VCC} and C_{VCCL} as close as possible to VCC and VCCL pins of the phase IC respectively.
- Place the phase IC as close as possible to the MOSFETs to reduce the parasitic resistance and inductance of the gate drive paths.
- Place the input ceramic capacitors close to the drain of top MOSFET and the source of bottom MOSFET. Use combination of different packages of ceramic capacitors.
- There are four switching power loops. Two loops include the input capacitors, top MOSFET, inductor, output capacitors and the load; two other loops consist of bottom MOSFET, inductor, output capacitors and the load. Route the switching power paths using wide and short traces or polygons; use multiple vias for connections between layers.

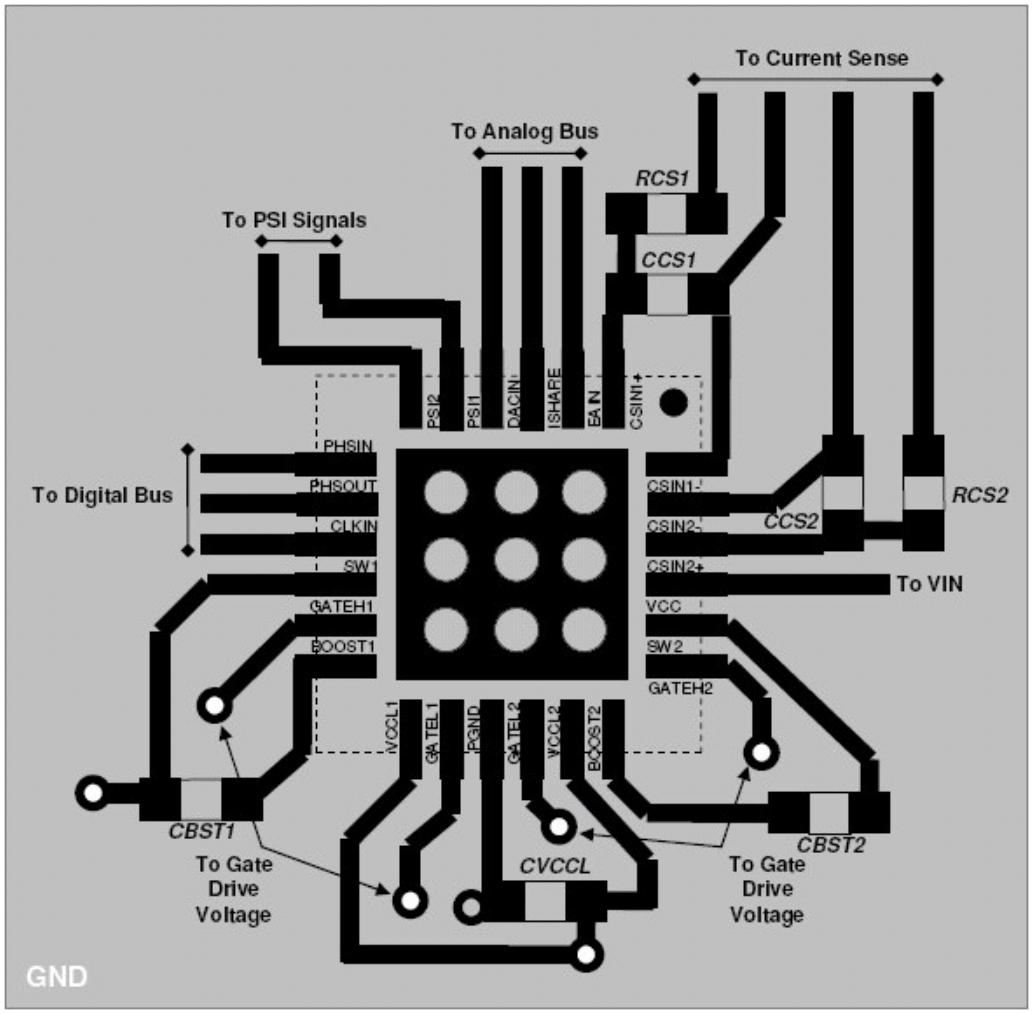
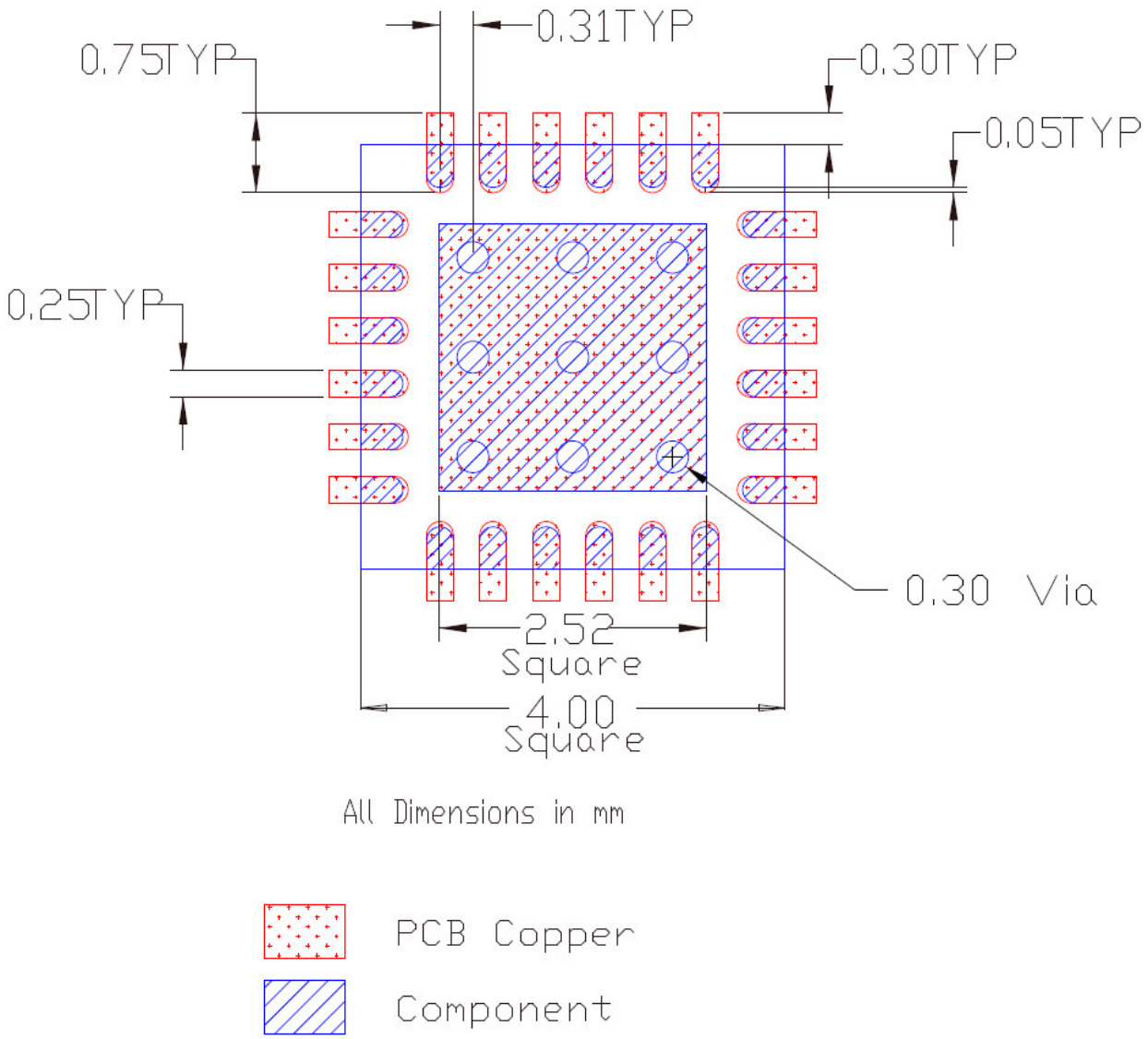


Figure 8 - Layout Guidelines for IR3527

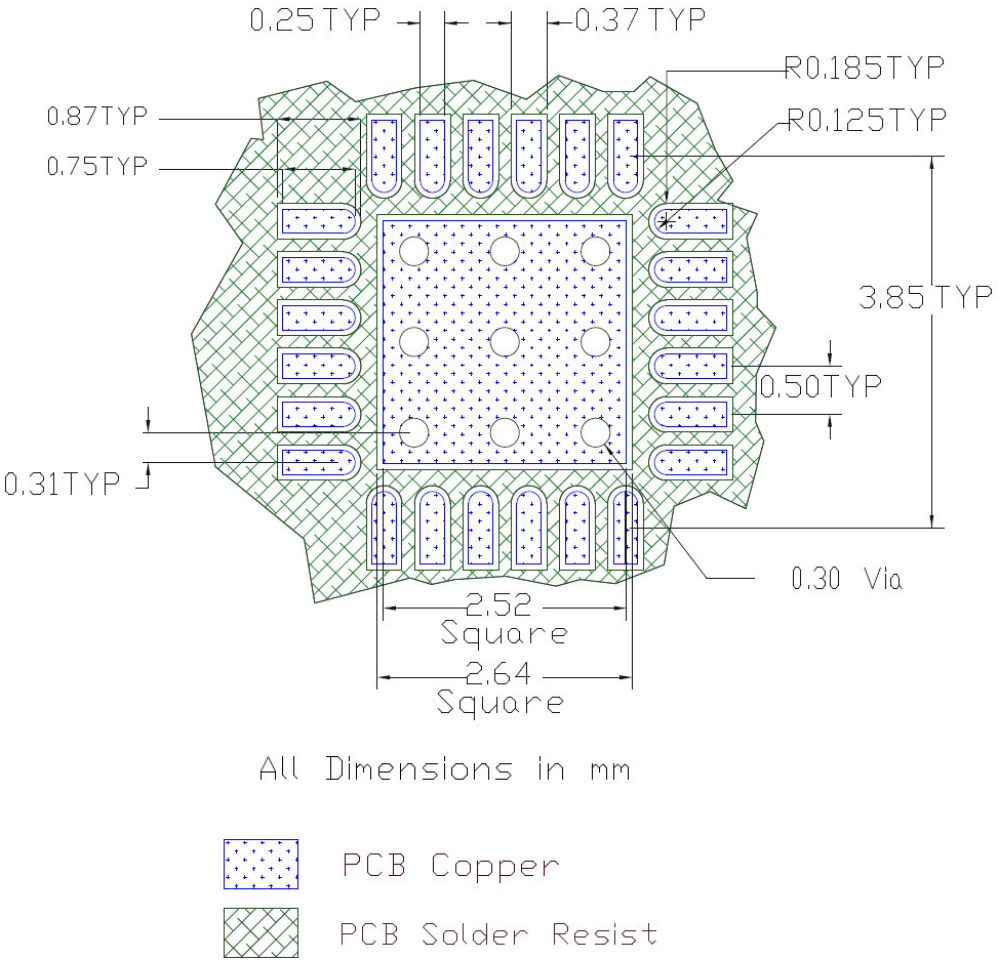
PCB Metal and Component Placement

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to prevent shorting.
- Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- Nine 0.3mm diameter vias shall be placed in the pad land spaced at 0.94 mm center to center, and connected to ground to minimize the noise effect on the IC and to transfer heat to the PCB.
- No pcb traces should be routed nor Vias placed under any of the 4 corners of the IC package. Doing so can cause the IC to raise up from the pcb resulting in poor solder joints to the IC leads.



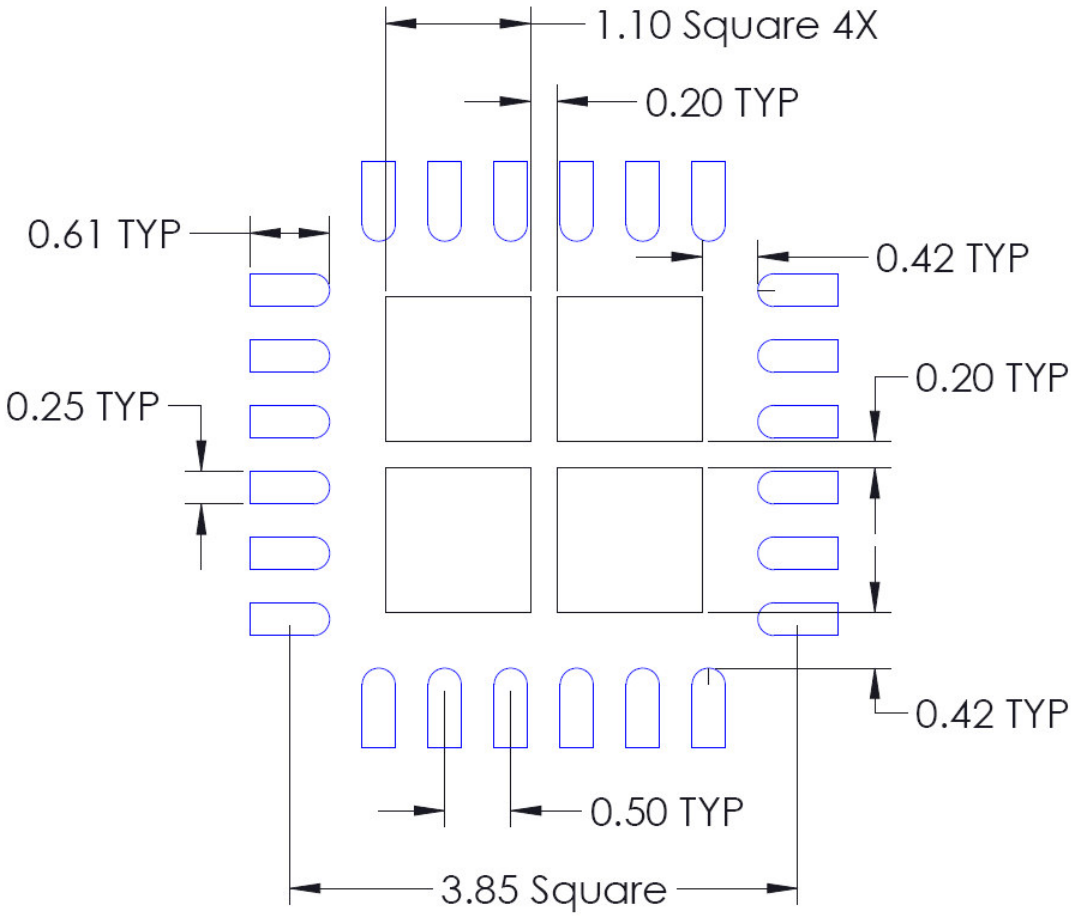
Solder Resist

- The solder resist should be pulled away from the metal lead lands and center pad by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore, pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm. At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The 9 vias in the land pad should be tented with solder resist 0.4mm diameter, or 0.1mm larger than the diameter of the via.



Stencil Design

- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be 4 square openings of 1.1 mm sides and spaced at 0.2 mm to deposit approximately 76% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.

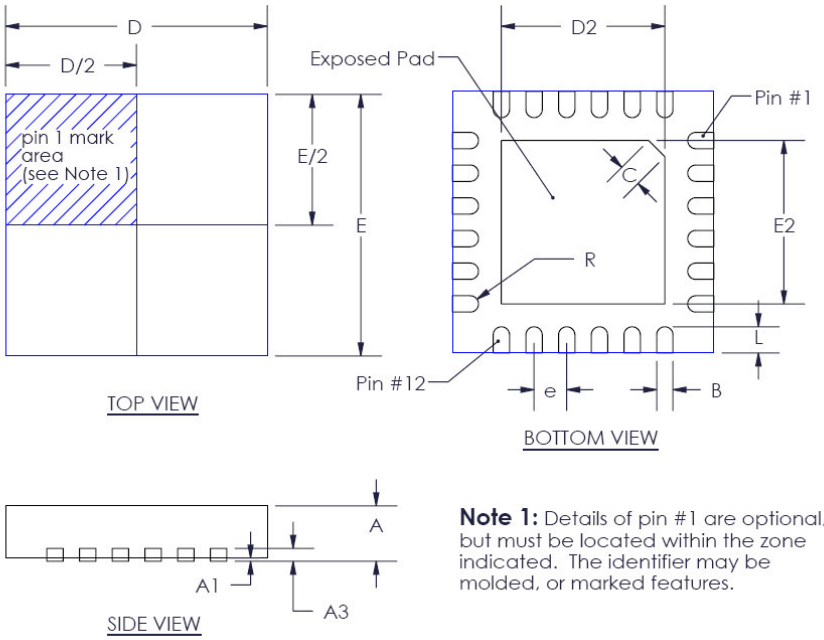


Stencil Aperture

All Dimensions in mm

PACKAGE INFORMATION

24L MLPQ (4 x 4 mm Body) – θ_{JA} = 30.5°C/w, θ_{JC} = 1.8°C/W



Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.

SYMBOL	24-PIN 4X4		
DESIG	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
B	0.20	0.25	0.30
D	3.90	4.00	4.10
D2		2.50 REF	
E	3.90	4.00	4.10
E2		2.50 REF	
e		0.50 TYP	
L	0.30	0.40	0.50
R		0.13 MIN	
C		0.35 TYP	

NOTE: ALL MEASUREMENTS ARE IN MILLIMELTERS.

Data and specifications subject to change without notice.
This product will be designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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