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Inverting High-Speed Operational Amplifier

OP-01

FEATURES

- **Fast Settling Time** . . . . . **1μsec to 0.1% Max.**
- **High Slew Rate** . . . . . **12V/μsec Min.**
- **Power Bandwidth** . . . . . **150kHz Min.**
- **Internally Compensated**

APPLICATIONS

- **D/A Converters**
- **Pin-for-Pin High-Performance 741 Replacement**
- **Fast Inverting Amplifier**

DESCRIPTION

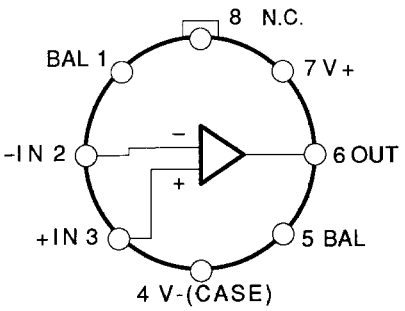
The OP-01 is an internally compensated, inverting, high-speed, high-slew rate amplifier with fast settling time and excellent DC characteristics. The OP-01 has input and output protection. Its use as a direct replacement for 741 operation amplifier results in significant performance enhancement without the need for circuit redesign. Military temperature devices, OP-01 and OP-01G, are available in 8-pin hermetic packages. Commercial temperature range devices, OP-01C and OP-01H, are also available in 8-pin plastic DIP packages.

ORDERING INFORMATION†

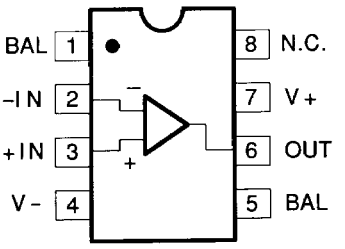
	PACKAGE				
T_A=25°C ΔV_{OS} MAX (mV)	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	PLASTIC SOIC 8-PIN	OPERATING TEMPERATURE RANGE
0.7	OP01J*	OP01Z*			MIL
0.7	OP01JH	OP01HZ	OP01HP	OP01HS	COM
5.0	OP01GJ*	OP01GZ*			MIL
5.0	OP01CJ	OP01CZ	OP01CP	OP01CS	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
†All commercial and industrial temperature range parts are available with burn-in.

Pin Connections (Top View)



TO-99 (J-Suffix)



EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP (Z-Suffix)
8-PIN PLASTIC SOIC (S-Suffix)

ABSOLUTE MAXIMUM RATINGS (Note 2)

Total Supply Voltage, OP-01, OP-01H, OP-01N, OP-01NT,
OP-01G, OP-01GT ..... ±22V
OP-01G, OP-01C, OP-01GR ..... ±20V
Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 3) ..... ±15V
Short-Circuit Duration ..... Indefinite
Operating Temperature Range
OP-01, OP-01G ..... −55°C to +125°C
OP-01H, OP-01C ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range
J and Z Packages ..... −65°C to +150°C
P Package ..... −65°C to +125°C
Lead Temperature (Soldering, 60 sec.) ..... 300°C

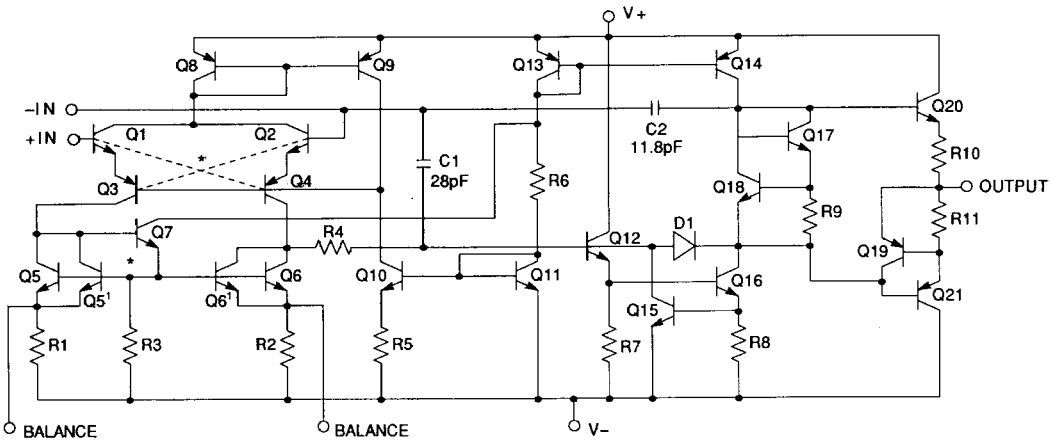
NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	35°C	5.6mW/°C

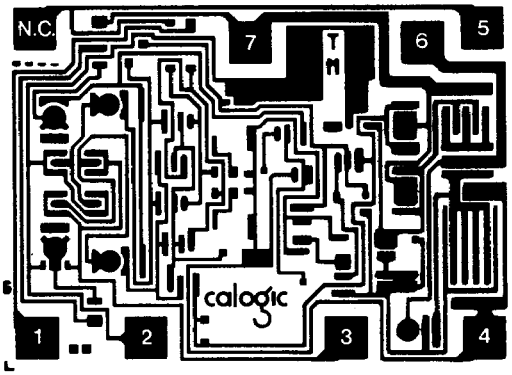
2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
3. For supply voltages less than ±15V, the maximum input voltage is the supply voltage.

Simplified Schematic Diagram



*Q1, Q2, Q3, AND Q4 FORM A THERMALLY CROSS-COUPLED QUAD. Q5, Q5', Q6, AND Q6' COMPRISE A SIMILAR THERMALLY CROSS-COUPLED QUAD.

Die Dimensions and Pad Connections



1. BALANCE
2. (−) INPUT
3. (+) INPUT
4. V−
5. BALANCE
6. OUTPUT
7. V+

DIE SIZE 0.063×0.047 inch, 2961 sq. mils
(1.6×1.194mm, 1.91 sq. mm)

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-01, OP-01H MIN.	OP-01, OP-01H TYP.	OP-01, OP-01H MAX.	OP-01G, OP-01C MIN.	OP-01G, OP-01C TYP.	OP-01G, OP-01C MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.7	—	2.0	5.0	mV
Input Offset Current	I_{OS}		—	0.5	2.0	—	2.0	20	nA
Input Bias Current	I_B		—	18	30	—	25	100	nA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$, $R_S \leq 20k\Omega$	85	110	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$, $R_S \leq 20k\Omega$	—	10	60	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±13.5 ±13.0	— —	±12.5 ±12.0	±13.5 ±13.0	— —	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	100	—	25	75	—	V/mV
Power Consumption	P_d	$V_{OUT} = 0$	—	50	90	—	50	90	mW
Settling Time to 0.1% (Summing Node Error)	t_S	$A_V = -1$ (Notes 1, 2), $V_{IN} = 5V$	—	0.7	1.0	—	0.7	1.0	μs
Slew Rate (Notes 2, 3)	SR	$A_V = -1$, $R_S = 3k$ to $5k\Omega$	12	18	—	12	18	—	V/μs
Large-Signal Bandwidth (Notes 3, 4)			150	250	—	150	250	—	kHz
Small-Signal Bandwidth (Notes 3, 4)			1.5	2.5	—	1.5	2.5	—	MHz
Risetime	t_r	$A_V = -1$, $V_{IN} = 50mV$	—	150	—	—	150	—	ns
Overshoot	OS		—	2	—	—	2	—	%

NOTES:
1. $R_L = 25k\Omega$; $C_L = 50pF$. See Settling Time Test Circuit
2. Sample Tested.
3. See applications information.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-01, OP-01G and $0°C \leq T_A \leq +70°C$ for OP-01H, OP-01C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-01, OP-01H MIN.	OP-01, OP-01H TYP.	OP-01, OP-01H MAX.	OP-01G, OP-01C MIN.	OP-01G, OP-01C TYP.	OP-01G, OP-01C MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.0	—	3.0	6.0	mV
Input Offset Current	I_{OS}		—	1	4	—	4	40	nA
Input Bias Current	I_B		—	30	50	—	50	200	nA
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	dB
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$, $R_S \leq 20k\Omega$	85	110	—	80	100	—	V
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$, $R_S \leq 20k\Omega$	—	10	60	—	100	150	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	30	60	—	15	50	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±13.5 ±13.0	— —	±12.5 ±12.0	±13.5 ±13.0	— —	V
Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S \leq 5k\Omega$	—	2	8	—	5	20	μV/°C

NOTE:
1. Sample Tested.

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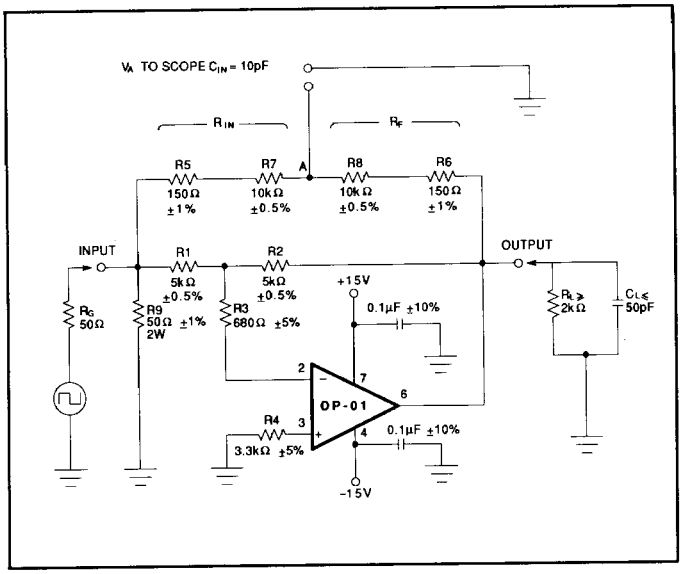
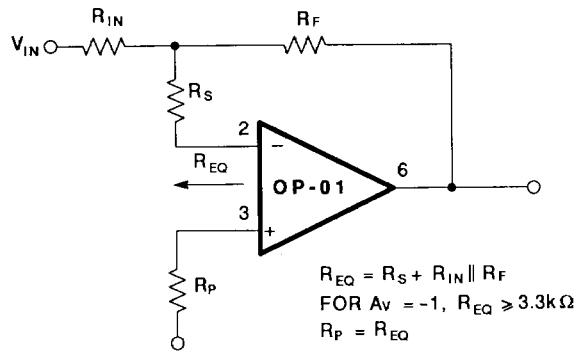
SETTLING-TIME TEST CIRCUIT

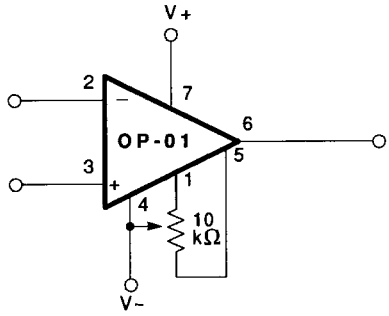
Settling time may be measured using the circuit shown below. This circuit incorporates the "false sum node" technique to produce accurate, repeatable results. For a 5V input step, 0.1% settling will be achieved when the false sum node settles to within ±2.5mV of its final value. The oscilloscope used for observation of the false sum node should have wide bandwidth, fast overload recovery time, and be used with a low capacity probe (≤10pF, including strays). A Tektronix 7504 scope with a 7A11 probe or equivalent is suggested. The pulse generator should have a 50Ω output impedance and be capable of a 5V rise time in ≤20ns with ringing less than 2.5mV after 0.5μs. Measurements to 0.1% require R_{IN} to equal R_F within 0.01%; R_5 and R_6 are used as trimming resistors to achieve this matching.



Fast Inverting Amplifier



Offset Nulling Circuit



APPLICATIONS INFORMATION

The OP-01 incorporates an internal feed-forward compensation network to provide fast slewing and settling times in all inverting and moderate-to-high-gain noninverting applications. Unity-gain bandwidth is a function of the total equivalent source resistance seen by the inverting terminal. Proper choice of this resistance will allow the user to maximize bandwidth while assuring proper stability. The equivalent-inverting-terminal-resistance is defined as $R_{IN}||R_F$, and it must be greater than 3.3kΩ to assure stability in all closed-loop gain configurations including unity gain. Should $R_{IN}||R_F \leq 3.3k\Omega$, a resistor ($R_S$) may be placed between the inverting input and the sum node to provide the required resistance. (See Fast inverting Amplifier Diagram.) Lower values to total equivalent resistance may be used to improve bandwidth in higher closed-loop gain configurations.

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