

SED1351F

CMOS GRAPHIC LCD CONTROLLER

DESCRIPTION

The SED1351F is a high-duty dot matrix graphic display LCD controller. It can interface with an 8bits or 16bits MPU having a READY (WAIT) input pin. Cycle steal mode is used to have the MPU access the VRAM so that the display is not disturbed. The SED1351F contains circuits that control all data and addresses for cycle steal operations and requires no external data/address control circuit. Furthermore, the device has a chip select output pin for VRAM. This makes it possible to directly connect up to eight 64K SRAMs or two 256K SRAMs to the SED1351F without using an external decoder.

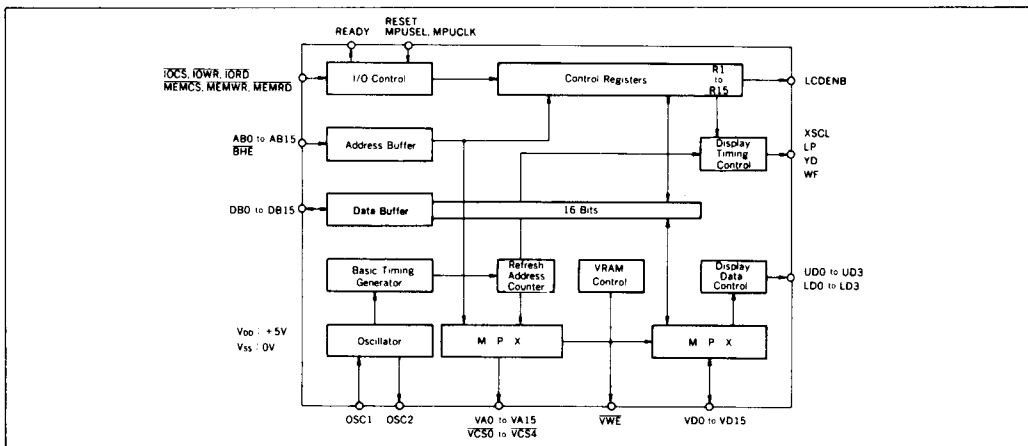
The VRAM addresses are mapped in the MPU memory space. This feature enables the MPU to directly address any display data for efficient data manipulation especially when the user is drawing a picture.

The SED1351F is available with two display modes to choose from, binary mode (on/off only) and gray mode (on/off and two gray steps). Use of the full 64K bytes capacity of VRAM makes it possible to display a maximum of 524,288 dots in the binary mode and 262,144 dots in the gray mode.

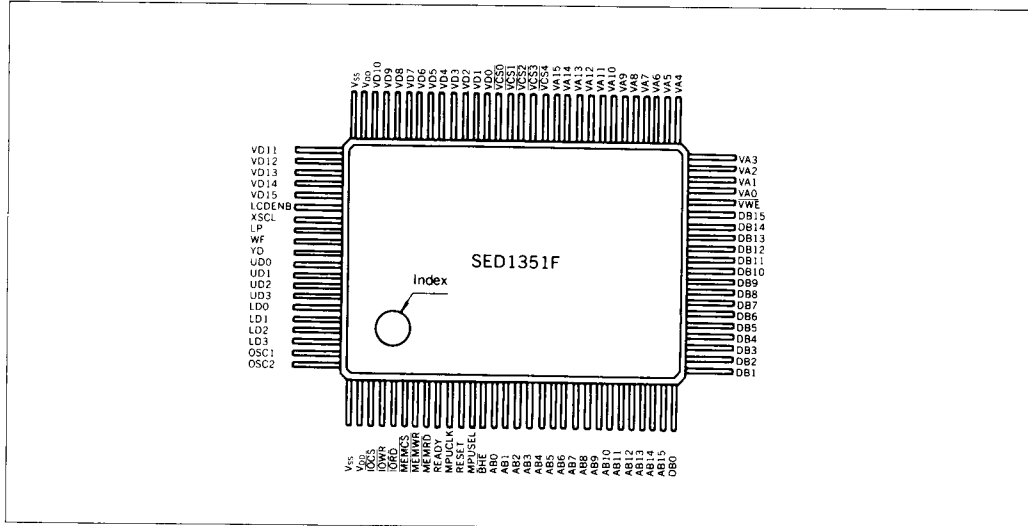
FEATURES

- VRAM capacity64K bytes (Mapping : MPU memory space)
- LCD display modesBinary (ON/OFF only)
Gray (ON/OFF + two gray steps)
- LCD panel1-screen configuration (4bits or 8bits data transfer)
2-screen configuration (4bits data transfer for each display)
- Maximum number of horizontal256 characters
2,048 dots (Binary display mode) / 1,024 dots (Gray display mode)
- Maximum number of vertical lines1,024 lines (1-screen drive) / 2,048 lines (2-screen drive)
- Panel division/OR functionEither to be selected in 1-screen drive mode
- Interface with MPU through use of READY (WAIT) signal
- Capability of using virtual display panel
- Smooth vertical scrolling
- Chip select output for VRAM
- Single power supply5V \pm 10%
- Package.....100pin QFP (Plastic)

BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

Pin Name	Pin No.	Functions	Pin Name	Pin No.	Functions
DB0 to DB15	30 to 45	MPU data bus	VCS0 to VCS4	67 to 63	VRAM chip select
AB0 to AB15	14 to 29	MPU address bus	VWE	46	VRAM write enable signal output
BHE	13	Bus high enable	UD0 to UD3	91 to 94	Upper panel dot data
IOCS	3	Control register chip select	LD0/UD4 to LD3/UD7	95 to 98	Lower/upper panel dot data
IOWR	4	Control register write enable signal input	XSCL	87	Dot data shift clock
IORD	5	Control register read enable signal input	LP	88	Dot data latch pulse
MEMCS	6	VRAM control chip select	WF	89	Frame signal (LCD AC signal)
MEMWR	7	VRAM control write enable signal input	YD	90	Scan data output
MEMRD	8	VRAM control read enable signal input	LCDENB	86	LCD control signal
READY	9	Ready (wait) signal	OSC1	99	Oscillator terminal (Input)
MPUCLK	10	MPU clock	OSC2	100	Oscillator terminal (Output)
MPUSEL	12	MPU selection (16bits/8bits)	VDD	2	Supply voltage (+5V)
RESET	11	Reset signal	VSS	1	GND
VD0 to VD15	68 to 78 81 to 85	VRAM data bus			
VA0 to VA12	47 to 59	VRAM address bus			
VA13/VCS7 to VA15/VCS5	60 to 62	VRAM address/chip select			

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{DD}	V _{SS} - 0.3 to 7.0	V
Input voltage	V _I	V _{SS} - 0.3 to V _{DD} + 0.3	V
Output voltage	V _O	V _{SS} - 0.3 to V _{DD} + 0.3	V
Output current/pin	I _O	±10	mA
Power dissipation	P _D	200	mW
Supply current	I _{DD} /I _{SS}	±40	mA
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature and time	T _{sol}	260°C, 10s (at lead)	—

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V _{DD}		4.5	5.0	5.5	V
Input voltage	V _I		V _{SS}	—	V _{DD}	V
Operating temperature	T _{opr}		-20	—	75	°C

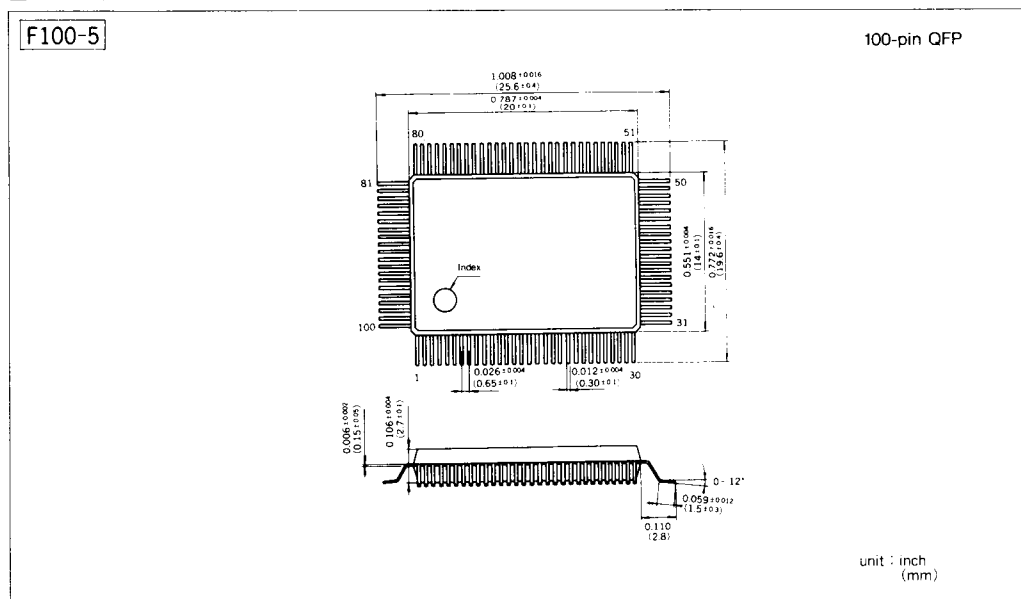
ELECTRICAL CHARACTERISTICS

DC Characteristics

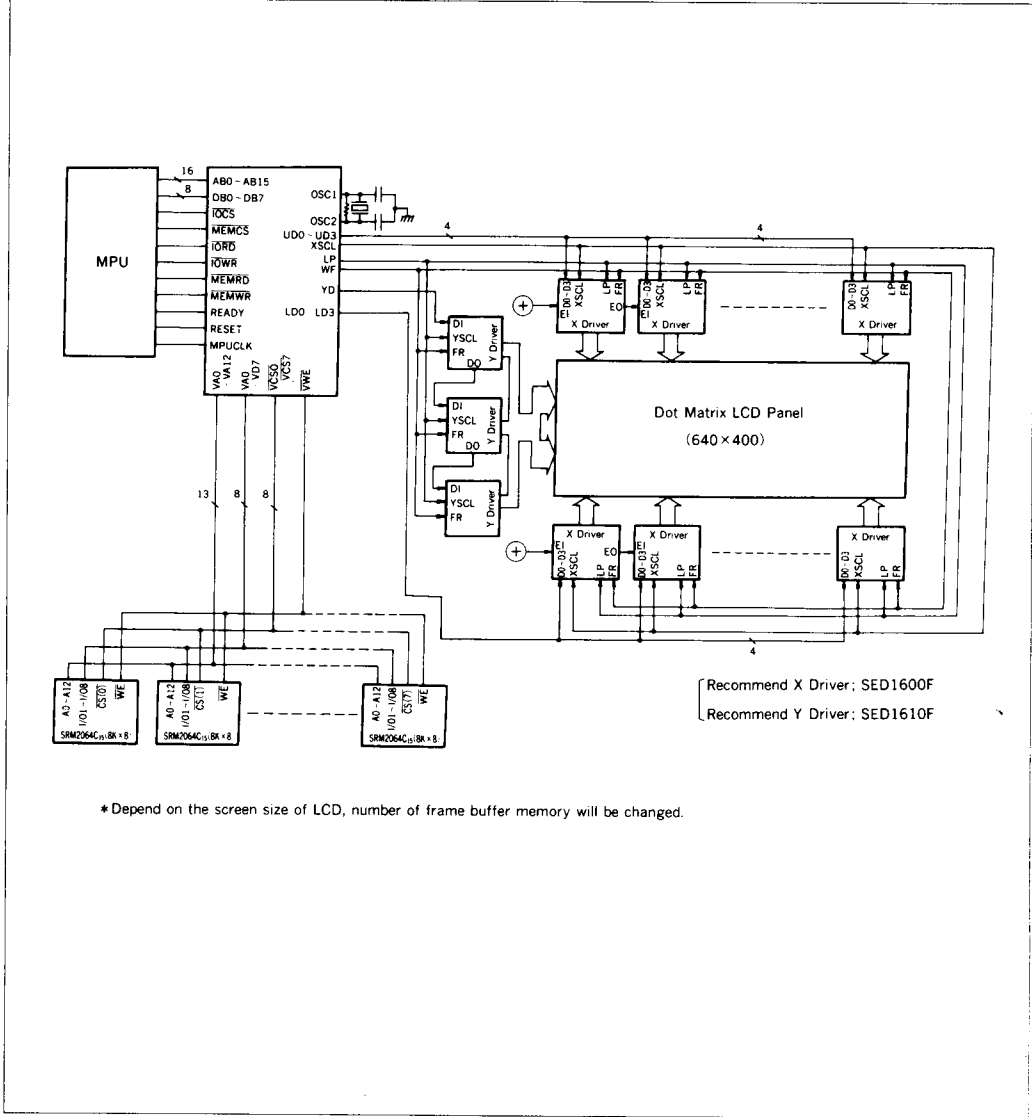
(T_a = -20°C to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Static current	I _{DDS}	V _{IN} = V _{DD} , V _{SS} I _{OH} = I _{OL} = 0	—	—	100	μA
Input leakage current	I _{L1}	V _{DD} = 5.5V V _{IH} = V _{DD} V _{IL} = V _{SS}	-10	—	10	μA
High level input voltage 1	V _{IH1}	V _{DD} = 5.5V	3.5	—	—	V
Low level input voltage 1	V _{IL1}	V _{DD} = 4.5V	—	—	1.0	V
High level input voltage 2	V _{IH2}	V _{DD} = 5.5V	2.0	—	—	V
Low level input voltage 2	V _{IL2}	V _{DD} = 4.5V	—	—	0.8	V
High level input voltage 3	V _{T+}	V _{DD} = 5.5V	—	—	4.0	V
Low level input voltage 3	V _{T-}	V _{DD} = 4.5V	0.8	—	—	V
Hysteresis voltage	V _H	V _{DD} = 5V	0.3	—	—	V
High level output voltage 1	V _{OH1}	V _{DD} = 4.5V I _{OH} = -2mA	V _{DD} - 0.4	—	—	V
Low level output voltage 1	V _{OL1}	I _{OL} = 6mA	—	—	V _{SS} + 0.4	V
High level output voltage 2	V _{OH2}	V _{DD} = 4.5V I _{OH} = -50μA	V _{DD} - 0.4	—	—	V
Low level output voltage 2	V _{OL2}	I _{OL} = 50μA	—	—	V _{SS} + 0.4	V

PACKAGE DIMENSIONS



EXAMPLE OF APPLICATION (When using an 8bits MPU)



* Depend on the screen size of LCD, number of frame buffer memory will be changed.