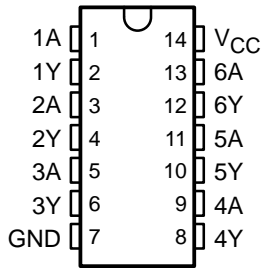


# SN54AHCT14, SN74AHCT14 HEX SCHMITT-TRIGGER INVERTERS

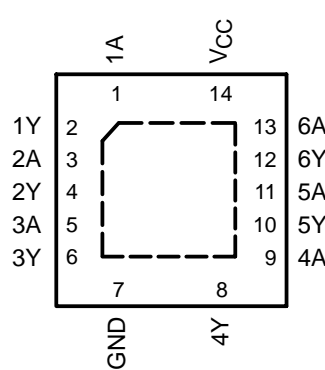
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- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

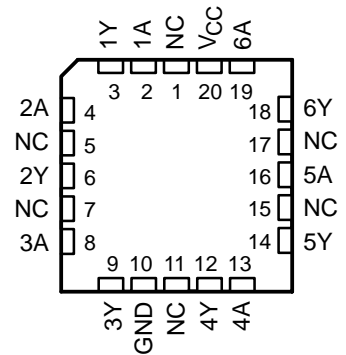
SN54AHCT14 . . . J OR W PACKAGE  
SN74AHCT14 . . . D, DB, DGV, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74AHCT14 . . . RGY PACKAGE  
(TOP VIEW)



SN54AHCT14 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'AHCT14 devices contain six independent inverters. These devices perform the Boolean function  $Y = \bar{A}$ . Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going ( $V_{T+}$ ) and for negative-going ( $V_{T-}$ ) signals.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74AHCT14RGYR	HB14
	PDIP – N	Tube	SN74AHCT14N	SN74AHCT14N
	SOIC – D	Tube	SN74AHCT14D	AHCT14
		Tape and reel	SN74AHCT14DR	
	SOP – NS	Tape and reel	SN74AHCT14NSR	AHCT14
	SSOP – DB	Tape and reel	SN74AHCT14DBR	HB14
	TSSOP – PW	Tube	SN74AHCT14PW	HB14
Tape and reel		SN74AHCT14PWR		
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHCT14DGVR	HB14
	CDIP – J	Tube	SNJ54AHCT14J	SNJ54AHCT14J
	CFP – W	Tube	SNJ54AHCT14W	SNJ54AHCT14W
	LCCC – FK	Tube	SNJ54AHCT14FK	SNJ54AHCT14FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

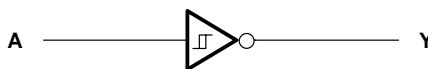
# SN54AHCT14, SN74AHCT14 HEX SCHMITT-TRIGGER INVERTERS

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**FUNCTION TABLE**  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): N package	80°C/W
(see Note 2): NS package	76°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.  
3. The package thermal impedance is calculated in accordance with JESD 51-5.

**recommended operating conditions (see Note 4)**

	SN54AHCT14		SN74AHCT14		UNIT
	MIN	MAX	MIN	MAX	
$V_{CC}$ Supply voltage	4.5	5.5	4.5	5.5	V
$V_I$ Input voltage	0	5.5	0	5.5	V
$V_O$ Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$ High-level output current		-8		-8	mA
$I_{OL}$ Low-level output current		8		8	mA
$T_A$ Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54AHCT14, SN74AHCT14 HEX SCHMITT-TRIGGER INVERTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHCT14		SN74AHCT14		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>T+</sub> Positive-going input threshold voltage		4.5 V	0.9		1.9	0.9	1.9	0.9	1.9	V
		5.5 V	1		2.1	1	2.1	1	2.1	
V <sub>T-</sub> Negative-going input threshold voltage		4.5 V	0.5		1.5	0.5	1.5	0.5	1.5	V
		5.5 V	0.6		1.7	0.6	1.7	0.6	1.7	
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )		4.5 V	0.4		1.4	0.4	1.4	0.4	1.4	V
		5.5 V	0.4		1.5	0.4	1.5	0.4	1.5	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		4.4		V
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1		0.1	V
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44		0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V				±0.1		±1*		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V				2		20		μA
ΔI <sub>CC</sub> †	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V				1.35		1.5		mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10				10	pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

switching characteristics over recommended operating free-air temperature range  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHCT14		SN74AHCT14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF		4**	7**	1**	8**	1	8	ns
t <sub>PHL</sub>					4**	7**	1**	8**	1	8	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF		5.5	8	1	9	1	9	ns
t <sub>PHL</sub>					5.5	8	1	9	1	9	

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 5)

PARAMETER		SN74AHCT14			UNIT
		MIN	TYP	MAX	
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.9		V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		-0.7		V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>		4.3		V
V <sub>IH(D)</sub>	High-level dynamic input voltage		2.1		V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.5	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

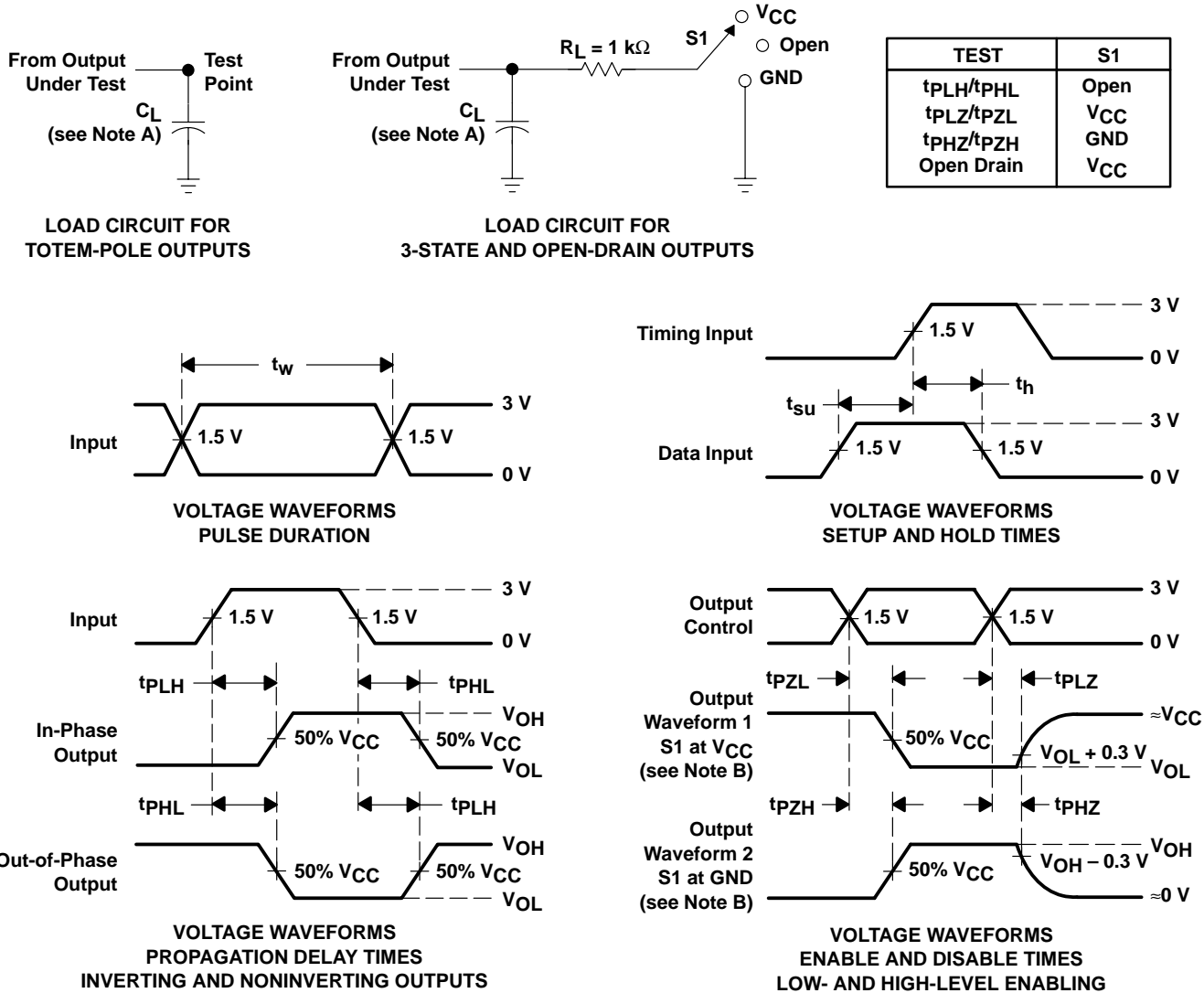
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load, f = 1 MHz	12	pF



# SN54AHCT14, SN74AHCT14 HEX SCHMITT-TRIGGER INVERTERS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 3 ns, t<sub>f</sub> ≤ 3 ns.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9680101Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
5962-9680101QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
5962-9680101QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
5962-9680101VCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI
5962-9680101VDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI
SN74AHCT14D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74AHCT14DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14DGV	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14DGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHCT14NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHCT14NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74AHCT14PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT14PWG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
						no Sb/Br)		
SN74AHCT14RGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74AHCT14RGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SNJ54AHCT14FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54AHCT14J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
SNJ54AHCT14W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

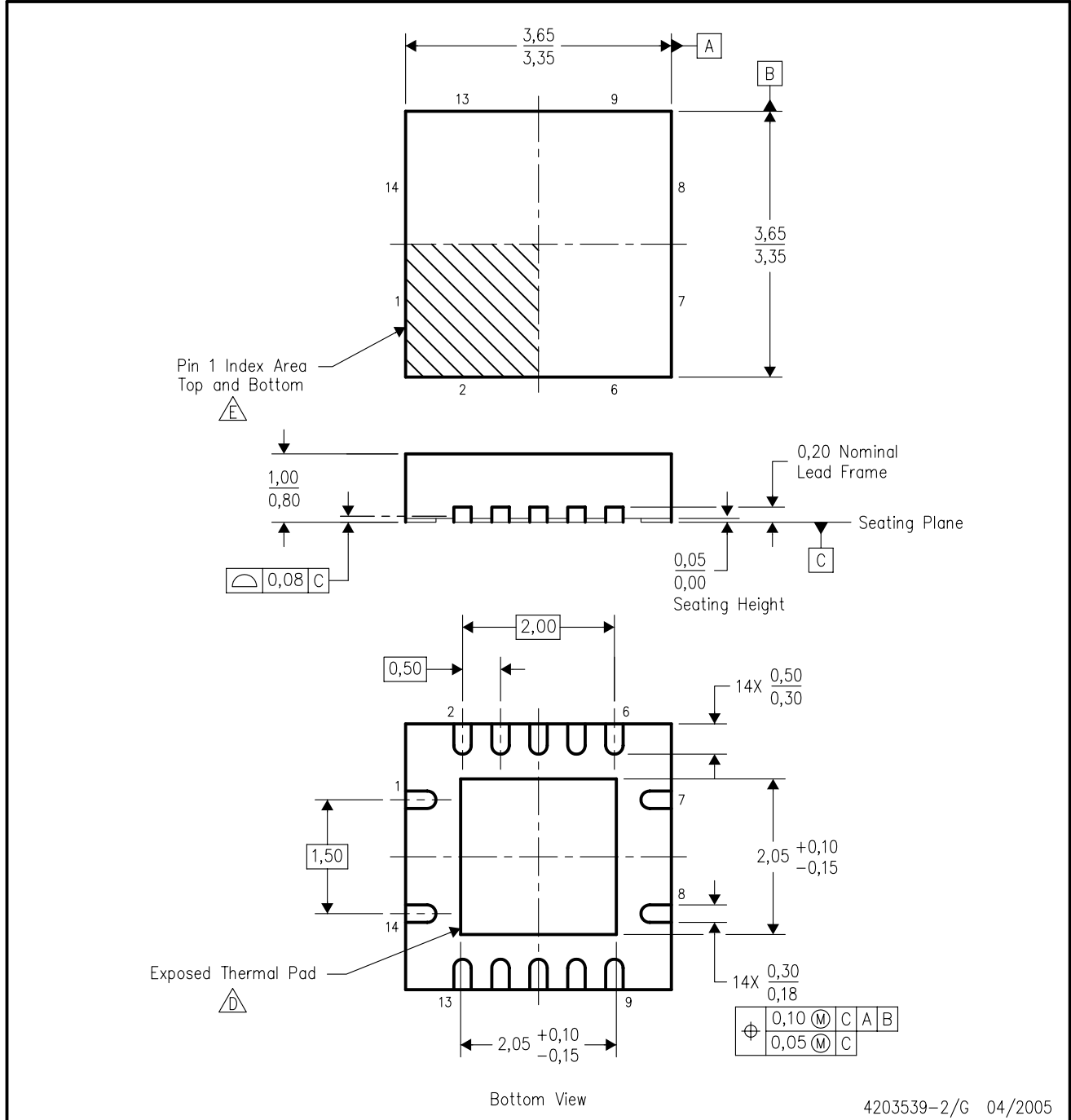
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



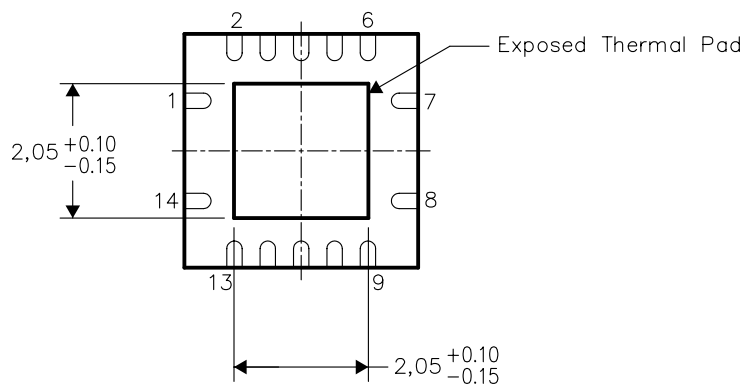
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BA.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150



PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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